

Description

This invention relates to a method of manufacturing an insulated-gate semiconductor integrated circuit having protection diodes protecting internal circuits against electrostatic breakdown.

In general, insulated-gate, e.g. MOS (metal-oxide semiconductor) semiconductor integrated circuits are provided with protection circuits in macrocells of input/output section in order to protect internal circuits from electrostatic breakdown. A prior art protection circuit is arranged as shown in Fig. 1. That is, a diode 3 is connected between a signal line 2 connected to an input/output pad 1 and a high-potential supply voltage V_{DD} node, while a diode 4 is connected between signal line 2 and a low-potential supply voltage V_{SS} node (usually ground potential node). Further, a protective resistor 5 is provided between signal line 2 and internal circuit 7 to be protected.

However, the conventional protection circuit composed of diodes 3 and 4, and resistor 5 has not yet achieved a satisfactory protection strength against electrostatic breakdown. To obtain a satisfactory strength of protection against electrostatic breakdown it is required that the constituent components of the protection circuit be made large in size. In this case, however, the macrocell is also required to be made large in size, thus provided a great difficulty in making integrated circuits small.

Prior art document Patent Abstracts of Japan 9(298), (E-361)(2021), discloses a method wherein a parasitic diode between a substrate and drain of a MOS transistor in an unused cell of a group of input-output cells is utilized as protection diode to improve the electrostatic strength thereof.

Further, prior art document GB-A-2 143 990 discloses a method wherein a semiconductor integrated circuit device which includes input and output buffers each provided in correspondence with a bonding pad is made usable for either the input buffer or the output buffer in accordance with a wiring pattern to be formed therein using the same circuit elements.

It is an object of this invention to provide a method of manufacturing an insulated-gate semiconductor integrated circuit capable of enhancing the electrostatic breakdown strength without increasing the area occupied by a protection circuit in the integrated circuit.

To solve this object the present invention provides a method as specified in claim 1.

A pull-up MOS transistor and a pull-down MOS transistor usually incorporated in an insulated-gate semiconductor integrated circuit for pulling up or down the potential of a signal line connected between a protection circuit and an internal circuit, are manufactured connecting drains of the two

MOS transistors together to the signal line, and connecting source of the pull-up or pull-down MOS transistor to pull-up or pull-down supply voltage node as needed.

The pull-up or pull-down MOS transistor functions as such when its source is connected to the pull-up or pull-down supply voltage node by the master slice wiring. On the other hand, when their sources are open, a drain junction of each of the MOS transistors serves as a protection diode. Accordingly, owing to the protection functions of the drain junction and the diodes in the protection circuit, the electrostatic breakdown strength of the internal circuit can be enhanced without the increase in the area occupied by the protection circuit in the integrated circuit.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram of a protection circuit of a prior art MOS semiconductor integrated circuit;

Fig. 2 is a circuit diagram showing a protection circuit and protection diodes formed of drain junctions of MOS transistors in an insulated-gate type semiconductor integrated circuit useful for explaining a method according to the embodiment of this invention;

Fig. 3 is a sectional view of MOS transistors in Fig. 2;

Fig. 4 shows a pattern layout of an N channel MOS transistor in Fig. 2;

Fig. 5 shows a pattern layout of a P channel MOS transistor in Fig. 2;

Fig. 6 is a circuit diagram of a protection circuit and protection diodes formed of drain junctions of MOS transistors of an insulated gate semiconductor integrated circuit useful for explaining a method according to another embodiment of this invention;

Fig. 7 shows a pattern layout of N channel MOS transistors in Fig. 6;

Fig. 8 shows a pattern layout of P channel MOS transistors in Fig. 6; and

Figs. 9 and 10 each show an MOS semiconductor integrated circuit useful for explaining a method according to a further embodiment of this invention.

Referring to Fig. 2 through Fig. 4, an embodiment of this invention will be described in detail hereinafter.

Fig. 2 shows an input/output pad 1, a protection circuit 6 provided in a macrocell of an input/output section, and MOS transistors 11 and 12 used as protection diodes in an MOS semiconductor integrated circuit. Protection circuit 6 comprises a signal line 2, a diode 3 connected between signal

line 2 and a high-potential supply voltage V_{DD} node, a diode 4 connected between signal line 2 and a low-potential supply voltage V_{SS} node, and a protective resistor 5 connected between signal line 2 and a signal line 10 connected to an internal circuit 7, which is an input gate or an output buffer though not shown in detail for simplification of the drawing. MOS transistors 11 and 12 are P and N channel transistors, respectively, with their drains connected together to signal line 10. P channel transistor 11 has its gate connected to a low potential supply voltage V_{SS} node (usually ground potential node), and its source opened instead of being connected to a high potential supply voltage V_{DD} node. On the other hand, N channel transistor 12 has its gate connected to high potential supply voltage V_{DD} node, and its source opened instead of being connected to low potential supply voltage V_{SS} node. P channel transistor 11 and N channel transistor 12 are provided for pulling up and down the potential of signal line 10, respectively, as needed.

Fig. 3 shows a sectional structure of P and N channel transistors 11 and 12. Reference numeral 21 denotes an N type semiconductor substrate, 22 and 23 P^+ diffusion regions formed in substrate 21 which serve as source and drain regions of P channel transistor 11, respectively, 24 N^+ diffusion region formed in substrate 21 for providing a substrate electrode, 25 a gate electrode for P channel transistor 11 formed over a channel between P^+ diffusion regions 22 and 23, and 26 P well region formed in the substrate. Further, reference numerals 27 and 28 denote N^+ diffusion regions formed in P well 26 which serve as drain and source regions of N channel transistor 12, 29 P^+ diffusion region adapted for an electrode of the P well, and 30 a gate electrode for N channel transistor 12 formed over a channel between N^+ diffusion regions 27 and 28. Gate electrode 30 of N channel transistor 12 and substrate electrode N^+ diffusion region 24 are connected to the V_{DD} node, while gate electrode 25 of P channel transistor 11 and P^+ diffusion region 29 adapted for P well electrode are connected to the V_{SS} node. The drain (P^+ diffusion region 23) of P channel transistor 11 and the drain (N^+ diffusion region 27) of N channel transistor 12 are connected together to signal line 10.

Fig. 4 shows a pattern layout of the N channel transistor 12. In the drawing reference numeral 31 represents an SDG region (source, drain and gate forming region) in which D stands for a drain region, G a gate region and S a source region. Reference numeral 10 represents the signal line which is in contact with drain region D. Gate electrode G is connected to a V_{DD} power supply line which is not shown. Reference numeral 32 denotes a V_{SS} power supply line which is not connected to

source region S in this example.

Though the same as that of N channel transistor 12, the pattern layout of P channel transistor 11 is shown in Fig. 5. That is, reference numeral 41 denotes SDG region (source, drain, and gate forming region) in which D represents a drain region, G a gate electrode, and S a source region. Reference numeral 10 represents a signal line which is in contact with drain region D. Gate electrode G is connected to a V_{SS} power supply line (not shown). Reference numeral 42 represents V_{DD} power supply line which is not connected to source region S in this example.

With the MOS type semicustom integrated circuit according to this embodiment the wiring is achieved by the master slice method. That is, the sources of P and N channel transistors 11 and 12 are opened instead of being connected to V_{DD} and V_{SS} nodes. To be used as a pull-up transistor P channel transistor 11 has its source connected to V_{DD} power supply node. Similarly, to act as a pull-down transistor the source of N channel transistor 12 is connected to V_{SS} power supply node.

In the circuit shown in Fig. 2, since the sources of MOS transistors 11 and 12 are open without being connected to V_{DD} and V_{SS} power supply nodes, the drain junction of each of transistors 11 and 12 acts as a protective diode. Thus, the electrostatic breakdown strength of the internal circuit can be enhanced. Further, since use is made of usually prepared transistors as MOS transistors 11 and 12 the area of protection circuit 6 does not increase. Therefore, the area of the macrocell in the input/output section does not increase either.

To use MOS transistors 11 and 12 as the pull-up and pull-down transistors it is required that the respective sources of transistors 11 and 12 be connected to the power supply nodes V_{DD} and V_{SS} using the master slice wiring technique. For example, where transistor 12 is used as the pull-down transistor the source of transistor 12 is connected to the V_{SS} power supply line as shown by a dashed-and-dotted line in Fig. 4.

Where MOS transistors 11 and 12 are each replaced with a plurality of transistors, and each transistor is used as a pull-up or pull-down transistor, the on-resistance of each transistor can be varied arbitrarily, thereby enabling the selection of resistance values of the transistors in conformity with uses for the integrated circuit.

Fig. 6 shows a circuit arrangement in which P channel transistor 11 is replaced with two transistors 11₁ and 11₂, and N channel transistor 12 is replaced with two transistors 12₁ and 12₂. A pattern layout of the transistor circuit of N channel transistors 12₁ and 12₂ is shown in Fig. 7, and a pattern layout of the transistor circuit of P channel transistors 11₁ and 11₂ is shown in Fig. 8.

In Fig. 7 reference numeral 51 denotes an SDG region, D1 a first drain region, G1 a first gate electrode, S1 (D2) a common region of a first source region and a second drain region, G2 a second gate electrode, and S2 a second source region. Drain region D1, gate electrode G1, and source region S1 form N channel transistor 12₁. Drain region D2, gate electrode G2, and source region S2 form N channel transistor 12₂. Signal line 10 is in contact with first drain region D1. First and second gate electrodes G1 and G2 are connected to V_{DD} power supply line (not shown). Reference numeral 52 represents V_{SS} power supply line. First and second source regions S1 and S2 are not connected to V_{SS} power supply line 52, and second source region S2 is opened. In this open state N channel transistor 12₁ acts as a protective diode. On the other hand, if source region S2 is connected to V_{SS} power supply line 52, then N channel transistors 12₁ and 12₂ will act as the pull-down transistors. It is to be noted that there is a difference in the on resistance of the transistor circuit formed of N channel transistors 12₁ and 12₂ between the case where second source region S2 is connected to V_{SS} power supply line 52 so that N channel transistors 12₁ and 12₂ are operated in a series connected circuit, and the case where first source region S1 is connected to V_{SS} power supply line 52 and second source region S2 is remained open so that N channel transistor 12₁ is only operated. Thus, it is made possible to select a desired on resistance value in accordance with a use for the integrated circuit.

In Fig. 8 reference numeral 61 denotes an SDG region, D1 a first drain region, G1 a first gate electrode, S1 (D2) a common region of a first source region a second drain region, G2 a second gate electrode, and S2 a second source region. Drain region D1, gate electrode G1, and source region S1 form P channel transistor 11₁. Drain region D2, gate electrode G2, and source region S2 form P channel transistor 11₂. Signal line 10 is in contact with first drain region D1. First and second gate electrodes G1 and G2 are connected to V_{SS} power supply line (not shown). Reference numeral 62 represents V_{DD} power supply line. First source region S1 and second source region S2 are not connected to V_{DD} power supply line 62, and second source region S2 is opened. In this open state P channel transistor 11₁ acts as a protective diode. On the other hand, if source region S2 is connected to V_{DD} power supply line 62, as shown by dotted-and-dashed line in Fig. 8, then P channel transistors 11₁ and 11₂ will act as the pull-up transistors. The on resistance of the transistor circuit formed of P channel transistors 11₁ and 11₂ differs between the case where second source region S2 is connected to V_{DD} supply line 62 so

that N channel transistors 11₁ and 11₂ are operated in a series connected circuit, and the case where first source region S1 is connected to V_{DD} power supply line 62 and second source region S2 is remained open so that N channel transistor 11₁ is only operated. Thus, it is made possible to select a desired on resistance value in accordance with a use for the integrated circuit.

Fig. 9 shows a MOS type semicustom integrated circuit according to still another embodiment of this invention.

In this embodiment, protection circuit 6i is connected to signal line 2i which is connected to input or output pad 1i (i stands for a pad number). Further, between signal line 10i connecting protection circuit 6i and internal circuit 7i together and power supply node V_{DD} is connected pull-up channel MOS transistor 11i, and between signal line 10i and power supply node V_{SS} is connected pull-down N channel MOS transistor 12i. In this drawing the source of pull-up transistor 11i is open, while the source of pull-down transistor 12i is connected to V_{SS} node. Thus, signal line 10i is pulled down to about V_{SS}.

Since the circuit composed of pad 1i, signal line 2i, protection circuit 6i, internal circuit 7i, P channel transistor 11i, and N channel transistor 12i is the same as the circuit shown in Fig. 2 the description thereof is omitted.

Fig. 10 shows a MOS type semicustom integrated circuit according to a further embodiment of this invention.

In this embodiment, protection circuit 6i is connected to signal line 2i which is connected to input or output pad 1i (i stands for a pad number). Further, between signal line 10i connecting protection circuit 6i and internal circuit 7i together and power supply node V_{DD} are connected pull-up P channel MOS transistors 11_{1i} and 11_{2i}, and between signal line 10i and power supply node V_{SS} are connected pull-down N channel MOS transistors 12_{1i} and 12_{2i}. In this drawing the source of pull-up transistor 11_{2i} is open, while the source of pull-down transistor 12_{2i} is connected to V_{SS} node. Thus, signal line 10i is pulled down to about V_{SS}.

Since the circuit composed of pad 1i, signal line 2i, protection circuit 6i, internal circuit 7i, P channel transistors 11_{1i} and 11_{2i}, and N channel transistors 12_{1i} and 12_{2i} is the same as the circuit shown in Fig. 6 the description thereof is omitted.

As described above, according to the above insulated-gate semicustom integrated circuit, the drain of a MOS transistor that has been previously prepared to pull up or down the signal line connected between the protection circuit and the internal circuit to be protected is connected to the signal line. Therefore, where the MOS transistor is not used for pulling up or down the signal line, by

keeping the source of the MOS transistor open instead of connecting to a power supply node, the drain junction of the transistor can be used as a protective diode. Thus, the protection strength of the internal circuit against electrostatic breakdown can be improved.

Claims

1. A method of manufacturing an insulated-gate semicustom integrated circuit having protective diodes protecting internal circuits against electrostatic breakdown, comprising:
 - an input/output pad (1) connected to a signal line (2);
 - a first protective diode (3) connected between said signal line (2) and a high-potential supply voltage (VDD);
 - a further first protective diode (4) connected between said signal line (2) and a low-potential supply voltage (VSS);
 - a protective resistor (5) connected between said signal line (2) and an internal signal line (10) connected to an internal circuit (7) of said integrated circuit;
 - an n-channel transistor (12) and a p-channel transistor (11),
 said method comprising the steps of
 - connecting the drain contacts of said transistors to said internal signal line (10),
 - connecting the gate contact of said p-channel transistor (11) to said low potential supply voltage (VSS) and connecting the gate contact of said n-channel transistor (12) to said high potential supply voltage (VDD), leaving the source contacts of said transistors open;
 - whereby in a master-slice wiring operation the source contact of said n-channel transistor (12) is either connected to said low potential supply voltage (VSS) to define a pull-down transistor, or left open to define a second protective diode; and
 - the source contact of said p-channel transistor (11) is either connected to said high potential supply voltage (VDD) to define a pull-up transistor, or left open to define a further second protective diode.
2. A method according to claim 1, characterized by further comprising the steps of
 - connecting at least one further p-channel transistor (11₂) in series to said p-channel transistor (11₁), the gate of said further p-channel transistor (11₂) being connected to said low potential supply voltage (VSS); and
 - connecting at least one further n-channel transistor (12₂) in series to said n-channel transistor (12₁), the gate of said further n-channel

transistor (12₂) being connected to said high potential voltage (VDD).

3. A method according to claim 1 or 2, characterized by further comprising a step of:
 - providing a plurality of said standard input/output cells.

Patentansprüche

1. Verfahren zur Herstellung einer halbkunden-spezifischen integrierten Schaltung mit isoliertem Gate, welche über Schutzdioden zum Schutz der internen Schaltungen gegen elektrostatischen Durchbruch verfügt, die folgendes umfaßt:
 - ein mit einer Signalleitung (2) verbundenes Eingangs-/Ausgangsglied (1);
 - eine zwischen der Signalleitung (2) und einer auf hohem Potential liegenden Versorgungsspannung (V_{DD}) eingeschaltete erste Schutzdiode (3);
 - eine weitere zwischen der Signalleitung (2) und einer auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) eingeschaltete zweite Schutzdiode (4);
 - einen zwischen der Signalleitung (2) und einer mit einer internen Schaltung (7) der integrierten Schaltung verbundenen internen Signalleitung (10) eingeschalteten Schutzwiderstand (5);
 - einen N-Kanaltransistor (12) und einen P-Kanaltransistor (11),
 wobei das Verfahren die folgenden Schritte umfaßt: Verbinden der Drainkontakte der Transistoren mit der internen Signalleitung (10); Verbinden des Gatekontaktes des P-Kanaltransistors (11) mit der auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) und Verbinden des Gatekontaktes des N-Kanaltransistors (12) mit der auf hohem Potential liegenden Versorgungsspannung (V_{DD}), wodurch die Sourcekontakte der Transistoren offen bleiben; wobei in einer Master-Slice-Verdrahtungsoperation der Sourcekontakt des N-Kanaltransistors (12) entweder mit der auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) zur Schaffung eines Pulldown-Transistors gekoppelt wird oder zur Schaffung einer zweiten Schutzdiode offen bleibt; und
 - der Sourcekontakt des P-Kanaltransistors (11) entweder mit der auf hohem Potential liegenden Versorgungsspannung (V_{DD}) zur Schaffung eines Pullup-Transistors gekoppelt wird oder zur Schaffung einer weiteren zweiten Schutzdiode offen bleibt.



keeping the source of the MOS transistor open instead of connecting to a power supply node, the drain junction of the transistor can be used as a protective diode. Thus, the protection strength of the internal circuit against electrostatic breakdown can be improved.

Claims

1. A method of manufacturing an insulated-gate semicustom integrated circuit having protective diodes protecting internal circuits against electrostatic breakdown, comprising:
an input/output pad (1) connected to a signal line (2);
a first protective diode (3) connected between said signal line (2) and a high-potential supply voltage (VDD);
a further first protective diode (4) connected between said signal line (2) and a low-potential supply voltage (VSS);
a protective resistor (5) connected between said signal line (2) and an internal signal line (10) connected to an internal circuit (7) of said integrated circuit;
an n-channel transistor (12) and a p-channel transistor (11),
said method comprising the steps of
connecting the drain contacts of said transistors to said internal signal line (10),
connecting the gate contact of said p-channel transistor (11) to said low potential supply voltage (VSS) and connecting the gate contact of said n-channel transistor (12) to said high potential supply voltage (VDD), leaving the source contacts of said transistors open;
whereby in a master-slice wiring operation the source contact of said n-channel transistor (12) is either connected to said low potential supply voltage (VSS) to define a pull-down transistor, or left open to define a second protective diode; and
the source contact of said p-channel transistor (11) is either connected to said high potential supply voltage (VDD) to define a pull-up transistor, or left open to define a further second protective diode.
2. A method according to claim 1, characterized by further comprising the steps of
connecting at least one further p-channel transistor (11₂) in series to said p-channel transistor (11₁), the gate of said further p-channel transistor (11₂) being connected to said low potential supply voltage (VSS); and
connecting at least one further n-channel transistor (12₂) in series to said n-channel transistor (12₁), the gate of said further n-channel

transistor (12₂) being connected to said high potential voltage (VDD).

3. A method according to claim 1 or 2, characterized by further comprising a step of:
providing a plurality of said standard input/output cells.

Patentansprüche

1. Verfahren zur Herstellung einer halbkunden-spezifischen integrierten Schaltung mit isoliertem Gate, welche über Schutzdioden zum Schutz der internen Schaltungen gegen elektrostatischen Durchbruch verfügt, die folgendes umfaßt:
ein mit einer Signalleitung (2) verbundenes Eingangs-/Ausgangsglied (1);
eine zwischen der Signalleitung (2) und einer auf hohem Potential liegenden Versorgungsspannung (V_{DD}) eingeschaltete erste Schutzdiode (3);
eine weitere zwischen der Signalleitung (2) und einer auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) eingeschaltete erste Schutzdiode (4);
einen zwischen der Signalleitung (2) und einer mit einer internen Schaltung (7) der integrierten Schaltung verbundenen internen Signalleitung (10) eingeschalteten Schutzwiderstand (5);
einen N-Kanaltransistor (12) und einen P-Kanaltransistor (11),
wobei das Verfahren die folgenden Schritte umfaßt: Verbinden der Drainkontakte der Transistoren mit der internen Signalleitung (10);
Verbinden des Gatekontaktes des P-Kanaltransistors (11) mit der auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) und Verbinden des Gatekontaktes des N-Kanaltransistors (12) mit der auf hohem Potential liegenden Versorgungsspannung (V_{DD}), wodurch die Sourcekontakte der Transistoren offen bleiben;
wobei in einer Master-Slice-Verdrahtungsoperation der Sourcekontakt des N-Kanaltransistors (12) entweder mit der auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) zur Schaffung eines Pulldown-Transistors gekoppelt wird oder zur Schaffung einer zweiten Schutzdiode offen bleibt; und
der Sourcekontakt des P-Kanaltransistors (11) entweder mit der auf hohem Potential liegenden Versorgungsspannung (V_{DD}) zur Schaffung eines Pullup-Transistors gekoppelt wird oder zur Schaffung einer weiteren zweiten Schutzdiode offen bleibt.



2. Verfahren gemäß Anspruch 1, dadurch gekennzeichnet, daß es des weiteren folgende Schritte umfaßt:

Schalten von mindestens einem weiteren P-Kanaltransistor (11₂) in Reihe mit dem P-Kanaltransistor (11₁), wobei das Gate des weiteren P-Kanaltransistors (11₂) mit der auf niedrigem Potential liegenden Versorgungsspannung (V_{SS}) gekoppelt wird;

Schalten von mindestens einem weiteren N-Kanaltransistor (12₂) in Reihe mit dem N-Kanaltransistor (12₁), wobei das Gate des weiteren N-Kanaltransistors (12₂) mit der auf hohem Potential liegenden Versorgungsspannung (V_{DD}) gekoppelt wird.

3. Verfahren gemäß Anspruch 1 oder 2, dadurch gekennzeichnet, daß es einen weiteren Schritt zur Bereitstellung einer Vielzahl von Standard-Eingangs-/Ausgangszellen umfaßt.

Revendications

1. Méthode de fabrication d'un circuit intégré pré-diffusé à grille isolée comportant des diodes protectrices protégeant des circuits internes contre un claquage électrostatique, comprenant : un plot d'entrée/sortie (1) connecté à une ligne de signaux (2) ; une première diode protectrice (3) connectée entre ladite ligne de signaux (2) et une borne de tension à haut potentiel d'alimentation (V_{DD}) ; une autre première diode protectrice (4) connectée entre ladite ligne de signaux (2) et une borne de tension à bas potentiel d'alimentation (V_{SS}) ; une résistance protectrice (5) connectée entre ladite ligne de signaux (2) et une ligne de signaux interne (10) connectée à un circuit interne (7) dudit circuit intégré ; un transistor à canal n (12) et un transistor à canal p (11),

ladite méthode comprenant les étapes qui consistent à :

connecter les contacts de drain desdits transistors à ladite ligne de signaux interne (10),

connecter le contact de grille dudit transistor à canal p (11) à ladite borne de tension à bas potentiel d'alimentation (V_{SS}) et connecter le contact de grille dudit transistor à canal n (12) à ladite borne de tension à haut potentiel d'alimentation (V_{DD}), en laissant les contacts de source desdits transistors ouverts ;

dans une opération de câblage de matrice standard, le contact de source dudit transistor à canal n (12) étant ainsi soit connecté à ladite borne de tension à bas potentiel d'alimentation (V_{SS}) pour définir un transistor de décharge, soit laissé ouvert pour définir une seconde

diode protectrice ; et le contact de source dudit transistor à canal p (11) étant ainsi soit connecté à ladite borne de tension à haut potentiel d'alimentation (V_{DD}) pour définir un transistor de charge, soit laissé ouvert pour définir une autre seconde diode protectrice.

2. Méthode selon la revendication 1, caractérisée en ce qu'elle comprend en outre les étapes qui consistent à :

connecter au moins au autre transistor à canal p (11₂) en série audit transistor à canal p (11₁), la grille dudit autre transistor à canal p (11₂) étant connectée à ladite borne de tension à bas potentiel d'alimentation (V_{SS}) ; et, a

connecter au moins un autre transistor à canal n (12₂) en série audit transistor à canal n (12₁), la grille dudit autre transistor à canal n (12₂) étant connectée à ladite borne de tension à haut potentiel d'alimentation (V_{DD}).

3. Méthode selon l'une quelconque des revendications 1 et 2, caractérisée en ce qu'elle comprend en outre une étape qui consiste à :

fournir une pluralité desdites cellules d'entrée/sortie standard.