ROUTER

CROSS REFERENCE TO RELATED APPLICATION

[0001] The application claims the benefit of US provisional application No. 61/753,250 filed January 16, 2013, which is hereby incorporated by reference herein in its entirety.

FIELD

[0002] Some embodiments relate to communication network elements.

BACKGROUND

[0003] A communications network may include one or more network elements to facilitate the communication of data, for example, between computing devices.

SUMMARY

[0003a] According to an aspect of the present invention, there is provided an apparatus comprising: a plurality of network interfaces including at least a first network interface, and a second network interface, wherein the first network interface is adapted to be connected to a first network, and wherein the second network interface is adapted to be connected to a second network, and a plurality of processors including at least a first processor, and a second processor, wherein the first processor is configurable to: obtain data received from the first network via the first network interface, ~~and~~ perform network address translation on the data such that the data has an address on the second network, and communicate to the second processor the data the first processor has translated from the first network to the second network, and obtain from the second processor data the second processor has received from the second network via the second network interface, perform network address translation on the data such that the data has an address on the first network, and communicate the data to the first network via the first network interface, wherein the first processor obtains data received from the first network work via the first network interface without use of the second processor, and communicates data to the first network via the first network interface without use of the second processor; and wherein the second processor is configurable to: obtain from the first processor the data the first processor has translated from the first network to the second network and communicate the data to the

second network via the second network interface; and obtain data received from the second network via the second network interface and communicate the data to the first processor for the first processor to perform network address translation on such that the data has an address on the first network, wherein the second processor obtains data received from the second network work via the second network interface without use of the first processor, and communicates data to the second network via the second network interface without use of the first processor.

BRIEF DESCRIPTION OF THE FIGURES

[0004] Figure 1A shows an example system according to some embodiments;

[0005] Figure IB shows an example configuration of the system of Figure 1 A;

[0006] Figure 2 shows another example system according to some embodiments; and

[0007] Figure 3 shows an example network element according to some embodiments.

DETAILED DESCRIPTION

[0008] Referring to Figure 1A, there is shown an example system 100. System 100 may include a plurality of entities, including entity 110 and a plurality of entities 130a-n (one of which is shown in detail in Figure 1A), one or more of which may be interconnected via network 103. Entity 110 may be, for example, a service provider that provides services, and each entity 130 may be, for example, a customer/user (e.g., such as a company, such as banks, investment funds, trading firm, etc.) of the services provided by service provider 110. For description purposes only, entity 110 will be referred to herein as a service provider and entity(s) 130 will be referred to as a user(s)/customer(s). Nonetheless, these terms are intended to be non- limiting and other example entities are possible. In addition, entity 110 being a service provider that provides services to entities 130 is also an example and other relationships between entities 110 and 130 are possible.

[0009] As one example, service provider 110 may provide one or more electronic marketplaces for the trading/buying-selling/matching of items (such as, for example, financial instruments, real-estate, bets/wagers, tangible goods, services, etc.) and as such, may provide

~~WHAT IS CLAIMED IS:~~ CLAIMS

1. An apparatus comprising:

a plurality of network interfaces including at least a first network interface, and a second network interface,

wherein the first network interface is adapted to be connected to a first network, and

wherein the second network interface is adapted to be connected to a second network, and

a plurality of processors including at least a first processor, and a second processor,

wherein the first processor is configurable to:

obtain data received from the first network via the first network interface, ~~and~~ perform network address translation on the data such that the data has an address on the second network, and communicate to the second processor the data the first processor has translated from the first network to the second network, and

obtain from the second processor data the second processor has received from the second network via the second network interface, perform network address translation on the data such that the data has an address on the first network, and communicate the data to the first network via the first network interface,

wherein the first processor obtains data received from the first network work via the first network interface without use of the second processor, and communicates data to the first network via the first network interface without use of the second processor; and

wherein the second processor is configurable to:

obtain from the first processor the data the first processor has translated from the first network to the second network and communicate the data to the second network via the second network interface; and

obtain data received from the second network via the second network interface and communicate the data to the first processor for the first processor to perform network address translation on such that the data has an address on the first network,

wherein the second processor obtains data received from the second network work via the second network interface without use of the first processor, and communicates data to the second network via the second network interface without use of the first processor.

2. The apparatus of claim 1, further comprising at least a third network interface adapted to be connected to a third network, and at least ~~a third~~ a third ~~process~~ processor,

wherein the third processor is configurable to:

obtain data received from the third network via the third network interface, ~~and~~ perform network address translation on the data such that the data has an address on the second network, and communicate to the second processor the data the third processor has translated from the third network to the second network, and

obtain from the second processor data the second processor has received from the second network via the second network interface, perform network address translation on the data such that the data has an address on the third network, and communicate the data to the third network via the third network interface,

wherein the third processor obtains data received from the third network work via the third network interface without use of the second processor, and communicates data to the third network via the third network interface without use of the second processor; and

wherein the second processor is further configurable to:

obtain from the third processor the data the third processor has translated from the third network to the second network and communicate the data to the second network via the second network interface; and

obtain data received from the second network via the second network interface and communicate the data to the third processor for the third processor to perform network address translation on such that the data has an address on the third network,

wherein the second processor obtains data received from the second network work via the second network interface without use of the third processor, and communicates data to the second network via the second network interface without use of the third processor.

3. The apparatus of claim 2, wherein the apparatus is configurable such that:

all data received by the first network interface from the first network is communicated from the first network interface only to the first processor; and

all data received by the third network interface from the third network is communicated from the third network interface only to the third processor.

4. The apparatus of claim 3, wherein the apparatus is re-configurable such that:

all data received by the first network interface from the first network is communicated from the first network interface only to the third processor; and

all data received by the third network interface from the third network is communicated from the third network interface only to the first processor.

5. The apparatus of claim 1, wherein the first processor is further configured to perform port translation on data.

6. The apparatus of claim 1,

wherein a shared memory circular queue is associated with the first processor and the second processor, the shared memory access queue having indexes associated therewith

wherein to communicate by the first processor to the second processor the data the first processor has translated from the first network to the second network incudes to place by the first processor the data into the shared memory access queue,

wherein to obtain by the second processor from the first processor the data the first processor has translated from the first network to the second network includes to read by the second processor the data from shared memory access queue, and

wherein the first and second processors update the indexes associated with the shared memory access queue to reflect data being placed into and read out of the shared memory access queue.

7. The apparatus of claim 6,

wherein another shared memory circular queue is associated with the first processor and the second processor, the another shared memory access queue having indexes associated therewith,

wherein to communicate by the second processor to the first processor the data the second processor has received from the second network via the second network interface incudes to place by the second processor the data into the another shared memory access queue,

wherein to obtain by the first processor from the second processor the data the second processor has received from the second network via the second network interface includes to read by the first processor the data from the another shared memory access queue, and

wherein the first and second processors update the indexes associated with the another shared memory access queue to reflect data being placed into and read out of the another shared memory access queue.

8. The apparatus of claim 3,

wherein for all data received by the first network interface from the first network to be communicated from the first network interface only to the first processor, and for all data received by the third network interface from the third network to be communicated from the third network interface only to the third processor includes to:

configure interrupts such that the first processor receives interrupts from the first network interface but not the third network interface, and

configure interrupts such that the third processor receives interrupts from the third network interface but not the first network interface.

9. The apparatus of claim 1, further comprising a semiconductor chip that has a plurality of cores, wherein a first of the cores comprises the first processor, and a second different one of the cores comprises the second processor.

10. The apparatus of claim 1 further comprising:

a third first network interface adapted to be connected to a third network,

a forth network interface adapted to be connected to a fourth network,

a third processor, and

a fourth processor,

wherein the third processor is configurable to:

obtain data received from the third network via the third network interface, perform network address translation on the data such that the data has an address on the fourth network, and communicate to the fourth processor the data the third processor has translated from the third network to the fourth network, and

obtain from the fourth processor data the fourth processor has received from the fourth network via the fourth network interface, perform network address translation on the data such that the data has an address on the third network, and communicate the data to the third network via the third network interface,

wherein the third processor obtains data received from the third network work via the third network interface without use of the fourth processor, and communicates data to the third network via the third network interface without use of the fourth processor; and

wherein the fourth processor is configurable to:

obtain from the third processor the data the third processor has translated from the third network to the fourth network and communicate the data to the fourth network via the fourth network interface; and

obtain data received from the fourth network via the fourth network interface and communicate the data to the third processor for the third processor to perform network address translation on such that the data has an address on the third network,

wherein the fourth processor obtains data received from the fourth network work via the fourth network interface without use of the third processor, and communicates data to the fourth network via the fourth network interface without use of the third processor.

11. The apparatus of claim 10, further comprising a first and a second semiconductor chip each of which has a plurality of cores, wherein a first of the cores of the first chip comprises the first processor, a second different one of the cores of the first chip comprises the second processor, a first of the cores of the second chip comprises the third processor, a second different one of the cores of the second chip comprises the fourth processor.