CLAIMS

1. A method, comprising:

writing data to one or more static random access memory (SRAM) cells, wherein writing data to the one or more SRAM cells comprises applying a data signal to at least one bitline electrically connected to the one or more SRAM memory cells, electrically disconnecting at least one of a first power supply terminal and a second power supply terminal of each of the one or more SRAM cells from a power supply, and applying a wordline signal to a wordline electrically connected to the one or more SRAM cells; and

thereafter, electrically connecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells to the power source.

2. A method according to claim 1, wherein electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply and applying the wordline signal to the wordline are performed substantially simultaneously.

3. A method according to claim 2, wherein the wordline signal is provided to the wordline at least until the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source

4. A method according to claim 1, wherein the wordline signal is applied to the wordline after electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply.

5. A method according to claim 4, wherein the wordline signal is provided to the wordline for a time interval, and wherein the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source before the end of the time interval.

6. A method according to claim 1, wherein the data signal is applied to the at least one bitline before electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply.

7. A method according to claim 6, wherein the data signal is provided to the at least one bitline at least until the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source.

8. A method according to claim 1, wherein writing data to the one or more SRAM cells further comprises:

applying an inverse data signal to at least one inverse bitline electrically connected to the one or more SRAM cells, the data signal and the inverse data signal being applied substantially simultaneously.

9. A method according to claim 8, further comprising reading data from the one or more SRAM cells, wherein reading data from the one or more SRAM cells comprises:

precharging the at least one bitline and the at least one inverse bitline;

applying a wordline signal to the wordline electrically connected to the one or more SRAM cells; and

for each of the one or more SRAM cells, sensing a voltage difference between one of the at least one bitline electrically connected to the SRAM cell and one of the at least one inverse bitline electrically connected to the SRAM cell;

wherein the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells remain electrically connected to the power source while the data are read

10. A method according to claim 1, wherein each SRAM cell is a six transistor SRAM cell.

11. A device, comprising:

a plurality of bitlines;

a plurality of wordlines;

a plurality of static random access memory (SRAM) cells, each SRAM cell being electrically connected to one of the bitlines and one of the wordlines, each SRAM cell having a first power supply terminal and a second power supply terminal;

a plurality of first switching devices, each first switching device being electrically connected between the first power supply terminal of at least one of the SRAM cells and a power source; and

a data writing circuit adapted for applying a data signal to each bitline electrically connected to the at least one of the SRAM cells, operating at least one of the first switching devices for electrically disconnecting the first power supply terminal of at least one of the plurality of SRAM cells from the power source, and applying a wordline signal to a wordline electrically connected to the at least one of the SRAM cells.

12. A device according to claim 11, further comprising:

a plurality of second switching devices, wherein each second switching device is electrically connected between the second power supply terminal of the at least one of the SRAM cells and the power source.

13. A device according to claim 11, wherein the plurality of SRAM cells comprises an array of SRAM cells, the array of SRAM cells comprising a plurality of rows, each row comprising two or more SRAM cells, each wordline being associated with one of the rows, each SRAM cell being electrically connected to the wordline associated with the row wherein the SRAM cell is provided.

14. A device according to claim 13, further comprising a plurality of high voltage power supply lines, each high voltage power supply line being associated with one of the rows, the first power supply terminal of each SRAM cell being electrically connected to the high voltage power supply line associated with the row wherein the SRAM cell is provided, each of the first switching devices being electrically connected between one of the high voltage power supply lines and the power source.

15. A device according to claim 14, wherein the first power supply terminals of the SRAM cells are high voltage terminals, and wherein each of the first switching devices comprises a p-channel field effect transistor.

16. A device according to claim 14, further comprising a plurality of low voltage power supply lines, each low voltage power supply line being associated with one of the rows, the second power supply terminal of each SRAM cell being electrically connected to the low voltage power supply line associated with the row wherein the SRAM cell is provided, the device further comprising a plurality of second switching devices, each of

the second switching devices being electrically connected between one of the low voltage power supply lines and the power source.

17. A device according to claim 16, wherein the second power supply terminals of the SRAM cells are low voltage terminals, and wherein each of the second switching devices comprises an n-channel field effect transistor.

18. A device according to claim 11, further comprising a plurality of inverse bitlines, each SRAM cell being electrically connected to one of the inverse bitlines, wherein the data writing circuit is adapted to apply an inverse data signal to each inverse bitline electrically connected to the at least one of the SRAM cells, wherein the data signal and the inverse data signal are applied substantially simultaneously.

19. A device according to claim 18, further comprising a read circuit adapted for precharging the bitline and the inverse bitline electrically connected to at least one of the plurality of SRAM cells, applying a wordline signal to a wordline electrically connected to the at least one of the plurality of SRAM cells, and sensing a voltage difference between the bitline and the inverse bitline for each of the at least one of the plurality of SRAM cells, wherein the first power supply terminal and the second power supply terminal of each of the at least one of the plurality of SRAM cells remain electrically connected to the power source.

20. A device according to claim 11, wherein each SRAM cell is a six transistor SRAM cell.

CLAIMS

1. A method, comprising:

writing data to one or more static random access memory (SRAM) cells, wherein writing data to the one or more SRAM cells comprises applying a data signal to at least one bit line electrically connected to the one or more SRAM memory cells, electrically disconnecting at least one of a first power supply terminal and a second power supply terminal of each of the one or more SRAM cells from a power supply, and applying a word line signal to a word line electrically connected to the one or more SRAM cells; and

thereafter electrically connecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells to the power source.

2. The method of claim 1, wherein electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply and applying the word line signal to the word line are performed substantially simultaneously.

3. The method of claim 2, wherein the word line signal is provided to the word line at least until the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source.

4. The method of claim 1, wherein the word line signal is applied to the word line after electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply.

5. The method of claim 4, wherein the word line signal is provided to the word line for a time interval, and wherein the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source before the end of the time interval.

6. The method of claim 1, wherein the data signal is applied to the at least one bit line before electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply.

7. The method of claim 6, wherein the data signal is provided to the at least one bit line at least until the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source.

8. The method of claim 1, wherein writing data to the one or more SRAM cells further comprises:

applying an inverse data signal to at least one inverse bit line electrically connected to the one or more SRAM cells, the data signal and the inverse data signal being applied substantially simultaneously.

9. The method of claim 8, further comprising reading data from the one or more SRAM cells, wherein reading data from the one or more SRAM cells comprises:

pre-charging the at least one bit line and the at least one inverse bit line;

applying a word line signal to the word line electrically connected to the one or more SRAM cells; and

for each of the one or more SRAM cells, sensing a voltage difference between one of the at least one bit line electrically connected to the SRAM cell and one of the at least one inverse bit line electrically connected to the SRAM cell;

wherein the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells remain electrically connected to the power source while the data are read.

10. The method of claim 1, wherein each SRAM cell is a six transistor SRAM cell.

11. A device, comprising:

a plurality of bit lines;

a plurality of word lines;

a plurality of static random access memory (SRAM) cells, each SRAM cell being electrically connected to one of the bit lines and one of the word lines, each SRAM cell having a first power supply terminal and a second power supply terminal;

a plurality of first switching devices, each first switching device being electrically connected between the first power supply terminal of at least one of the SRAM cells and a power source; and

a data writing circuit adapted for applying a data signal to each bit line electrically connected to the at least one of the SRAM cells, operating at least one of the first switching devices for electrically disconnecting the first power supply terminal of at least one of the plurality of SRAM cells from the power source, and applying a word line signal to a word line electrically connected to the at least one of the SRAM cells.

12. The device of claim 11, further comprising: a plurality of second switching devices, wherein each second switching device is electrically connected between the second power supply terminal of the at least one of the SRAM cells and the power source.

13. The device of claim 11, wherein the plurality of SRAM cells comprises an array of SRAM cells, the array of SRAM cells comprising a plurality of rows, each row comprising two or more SRAM cells, each word line being associated with one of the rows, each SRAM cell being electrically connected to the word line associated with the row wherein the SRAM cell is provided.

14. The device of claim 13, further comprising a plurality of high voltage power supply lines, each high voltage power supply line being associated with one of the rows, the first power supply terminal of each SRAM cell being electrically connected to the high voltage power supply line associated with the row wherein the SRAM cell is provided, each of the first switching devices being electrically connected between one of the high voltage power supply lines and the power source.

15. The device of claim 14, wherein the first power supply terminals of the SRAM cells are high voltage terminals, and wherein each of the first switching devices comprises a P-channel field effect transistor.

16. The device of claim 14, further comprising a plurality of low voltage power supply lines, each low voltage power supply line being associated with one of the rows, the second power supply terminal of each SRAM cell being electrically connected to the low voltage power supply line associated with the row wherein the SRAM cell is provided, the device further comprising a plurality of second switching devices, each of the second switching devices being electrically connected between one of the low voltage power supply lines and the power source.

17. The device of claim 16, wherein the second power supply terminals of the SRAM cells are low voltage terminals, and wherein each of the second switching devices comprises an N-channel field effect transistor.

18. The device of claim 11, further comprising a plurality of inverse bit lines, each SRAM cell being electrically connected to one of the inverse bit lines, wherein said data writing circuit is adapted to apply an inverse data signal to each inverse bit line electrically connected to the at least one of the SRAM cells, wherein the data signal and the inverse data signal are applied substantially simultaneously.

19. The device of claim 18, further comprising a read circuit adapted for precharging the bit line and the inverse bit line electrically connected to at least one of the plurality of SRAM cells, applying a word line signal to a word line electrically connected to the at least one of the plurality of SRAM cells, and sensing a voltage difference between the bit line and the inverse bit line for each of the at least one of the plurality of SRAM cells, wherein the first power supply terminal and the second power supply terminal of each of the at least one of the plurality of SRAM cells remain electrically connected to the power source.

20. The device of claim 11, wherein each SRAM cell is a six transistor SRAM cell.

21. A device having a SRAM cell, wherein data is written to the SRAM through a method of any one of claims 1-10.

22. The device of any one of claim 11-20 wherein data is written to the SRAM through a method of any one of claims 1-10.