

ABSTRACT

A memory system includes a memory controller; and a memory device configured to: during a write operation, generate a write error correction code based on write data, and store, according to a write poison signal received from the memory controller, the write data and the write error correction code, or first and second patterns in a memory cell array, and during a read operation, correct an error in read data based on a read error correction code read from the memory cell array, output a decoding status signal according to an error correction result, and generate a read poison signal according to at least one of the decoding status signal, a first comparison result between the read data and the first pattern, and a second comparison result between the read error correction code and the second pattern, to output the read poison signal to the memory controller.

FIG.1