PRE-SCREENING AND TUNING HETEROJUNCTIONS FOR TOPOLOGICAL QUANTUM COMPUTER

BACKGROUND

[0001] A quantum computer is a physical machine configured to execute logical operations based on or influenced by quantum-mechanical phenomena. Such logical operations may include, for example, mathematical computation. Current interest in quantum-computer technology is motivated by analysis suggesting that the computational efficiency of an appropriately configured quantum computer may surpass that of any practicable non-quantum computer when applied to certain types of problems. Such problems include computer modeling of natural and synthetic quantum systems, integer factorization, data searching, and function optimization as applied to systems of linear equations and machine learning. Furthermore, it has been predicted that continued miniaturization of conventional computer logic structures will ultimately lead to the development of nanoscale logic components that exhibit quantum effects, and must therefore be addressed according to quantum-computing principles.

[0002] Different types of quantum computers base their operation on different quantum-mechanical phenomena. A 'topological' quantum computer is a quantum computer whose operation is based on a non-Abelian topological phase of matter that may support 'braidable' quasiparticles. This type of quantum computer is expected to be less prone to the issue of quantum decoherence than other types of quantum computers, and may therefore serve as a relatively fault-tolerant quantum-computing platform.

SUMMARY

[0003] One aspect of this disclosure is directed to a method to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer. The method includes measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction, to obtain mapping data, and finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction. The method also includes measuring a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space, to obtain refinement data, and finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more

regions of the parameter space.

[0004] This Summary is provided to introduce in simplified form a selection of concepts that are further described in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter. The claimed subject matter is not limited to implementations that solve any or all disadvantages noted in any part of this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 shows aspects of an example quantum computer.

[0006] FIG. 2 illustrates a Bloch sphere, which graphically represents the quantum state of one qubit of a quantum computer.

[0007] FIG. 3 shows aspects of an example signal waveform for effecting a quantum-gate operation in a quantum computer.

[0008] FIG. 4 shows aspects of an example qubit architecture comprising a linear tetron array.

[0009] FIG. 5 shows aspects of an example semiconductor-superconductor heterojunction device evaluated according to the methods herein.

[0010] FIG. 6 shows aspects of an example method to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer.

[0011] FIG. 7 shows aspects of an example radio-frequency (RF) reflectometry test circuit.

[0012] FIG. 8 shows aspects of an example method to measure the RF junction admittance of a semiconductor-superconductor heterojunction.

[0013] FIG. 9 shows aspects of an example method to find, by analysis of the data from the method of FIG. 8, regions of a parameter space consistent with an unbroken topological phase of a semiconductor-superconductor heterojunction.

[0014] FIG. 10 shows aspects of analysis of mapping data according to the method of FIG. 9.

[0015] FIG. 11 shows aspects of an example sub-RF conductance test circuit.

[0016] FIG. 12 shows aspects of an example method to measure the sub-RF conductance of a semiconductor-superconductor heterojunction.

[0017] FIG. 13 shows aspects of an example method to find, by analysis of the data from the method of FIG. 12, a boundary of an unbroken topological phase in parameter space and a topological gap of a semiconductor-superconductor heterojunction.

[0018] FIG. 14 shows aspects of analysis of refinement data according to the method of

FIG. 13.

[0019] FIG. 15 shows the effect of a smooth potential at the right end of a semiconductor wire in a 1D model of a semiconductor-superconductor heterojunction.

[0020] FIG. 16 shows the effect of smooth potential at the center of a semiconductor wire in a 1D model of a semiconductor-superconductor heterojunction.

[0021] FIG. 17 shows the result of data analysis over field/plunger parameter space for a 1D model of a semiconductor-superconductor heterojunction with a potential bump in the center of the semiconductor wire.

[0022] FIG. 18 shows the result of data analysis over field/plunger parameter space of a strongly disordered 1D model of a semiconductor-superconductor heterojunction.

[0023] FIG. 19 shows aspects of an example instrument configured to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer.

[0024] FIG. 20 shows aspects of an example method for building a topological quantum computer.

DETAILED DESCRIPTION

Quantum Computer Architecture

[0025] FIG. 1 shows aspects of an example quantum computer 10 configured to execute quantum-logic operations (*vide infra*). Whereas conventional computer memory holds digital data in an array of bits and enacts bit-wise logic operations, a quantum computer holds data in an array of qubits and operates quantum-mechanically on the qubits in order to implement the desired logic. Accordingly, quantum computer 10 of FIG. 1 includes at least one qubit register 12 comprising an array of qubits 14. The illustrated qubit register is eight qubits in length; qubit registers comprising longer and shorter qubit arrays are also envisaged, as are quantum computers comprising two or more qubit registers of any length.

[0026] Qubits 14 of qubit register 12 may take various forms, depending on the desired architecture of quantum computer 10. While this disclosure relates to qubits embodied as quasiparticles in a non-Abelian topological phase, a qubit alternatively may comprise: a superconducting Josephson junction, a trapped ion, a trapped atom coupled to a high-finesse cavity, an atom or molecule confined within a fullerene, an ion or neutral dopant atom confined within a host lattice, a quantum dot exhibiting discrete spatial- or spin-electronic states, electron holes in semiconductor junctions entrained via an electrostatic trap, a coupled quantum-wire pair, an atomic nucleus addressable by magnetic resonance, a free electron in helium, a molecular magnet, or a metal-like carbon nanosphere, as non-limiting

examples. More generally, each qubit 14 may comprise any particle or system of particles that can exist in two or more discrete quantum states that can be measured and manipulated experimentally. For instance, a qubit may be implemented in the plural processing states corresponding to different modes of light propagation through linear optical elements (*e.g.*, mirrors, beam splitters and phase shifters), as well as in states accumulated within a Bose-Einstein condensate.

[0027] FIG. 2 is an illustration of a Bloch sphere 16, which provides a graphical description of some quantum mechanical aspects of an individual qubit 14. In this description, the north and south poles of the Bloch sphere correspond to the standard basis vectors $|0\rangle$ and $|1\rangle$, respectively. The set of points on the surface of the Bloch sphere comprise all possible pure states $|\psi\rangle$ of the qubit, while the interior points correspond to all possible mixed states. A mixed state of a given qubit may result from decoherence, which may occur because of undesirable coupling to external degrees of freedom.

[0028] Returning now to FIG. 1, quantum computer 10 includes a controller 18A. The controller includes at least one processor 20A and associated computer memory 22A. A processor 20A of controller 18A may be coupled operatively to peripheral componentry, such as network componentry, to enable the quantum computer to be operated remotely. A processor 20A of controller 18A may take the form of a central processing unit (CPU), a graphics processing unit (GPU), or the like. As such, the controller may comprise classical electronic componentry. The terms 'classical' and 'non-quantum' are applied herein to any component that can be modeled accurately as an ensemble of particles without considering the quantum state of any individual particle. Classical electronic components include integrated, microlithographed transistors, resistors, and capacitors, for example. Computer memory 22A may be configured to hold program instructions 24A that cause processor 20A to execute any function or process of the controller. The computer memory may also be configured to hold additional data 26A. In examples in which qubit register 12 is a low-temperature or cryogenic device, controller 18A may include control componentry operable at low or cryogenic temperatures—*e.g.*, a field-programmable gate array (FPGA) operated at 77K. In such examples, the low-temperature control componentry may be coupled operatively to interface componentry operable at normal temperatures.

[0029] Controller 18A of quantum computer 10 is configured to receive a plurality of inputs 28 and to provide a plurality of outputs 30. The inputs and outputs may each comprise digital and/or analog lines. At least some of the inputs and outputs may be data lines through which data is provided to and/or extracted from the quantum computer. Other inputs may

comprise control lines via which the operation of the quantum computer may be adjusted or otherwise controlled.

[0030] Controller 18A is operatively coupled to qubit register 12 via quantum interface 32. The quantum interface is configured to exchange data bidirectionally with the controller. The quantum interface is further configured to exchange signal corresponding to the data bidirectionally with the qubit register. Depending on the architecture of quantum computer 10, such signal may include electrical, magnetic, and/or optical signal. Via signal conveyed through the quantum interface, the controller may interrogate and otherwise influence the quantum state held in the qubit register, as defined by the collective quantum state of the array of qubits 14. To this end, the quantum interface includes at least one modulator 34 and at least one demodulator 36, each coupled operatively to one or more qubits of the qubit register. Each modulator is configured to output a signal to the qubit register based on modulation data received from the controller. Each demodulator is configured to sense a signal from the qubit register and to output data to the controller based on the signal. The data received from the demodulator may, in some examples, be an estimate of an observable to the measurement of the quantum state held in the qubit register.

[0031] In some examples, suitably configured signal from modulator 34 may interact physically with one or more qubits 14 of qubit register 12 to trigger measurement of the quantum state held in one or more qubits. Demodulator 36 may then sense a resulting signal released by the one or more qubits pursuant to the measurement, and may furnish the data corresponding to the resulting signal to controller 18A. Stated another way, the demodulator may be configured to output, based on the signal received, an estimate of one or more observables reflecting the quantum state of one or more qubits of the qubit register, and to furnish the estimate to the controller. In one non-limiting example, the modulator may provide, based on data from the controller, an appropriate voltage pulse or pulse train to an electrode of one or more qubits, to initiate a measurement. In short order, the demodulator may sense photon emission from the one or more qubits and may assert a corresponding digital voltage level on a quantum-interface line into the controller. Generally speaking, any measurement of a quantum-mechanical state is defined by the operator O corresponding to the observable to be measured; the result R of the measurement is guaranteed to be one of the allowed eigenvalues of O. In quantum computer 10, R is statistically related to the qubit-register state prior to the measurement, but is not uniquely determined by the qubit-register state.

[0032] Pursuant to appropriate input from controller 18A, quantum interface 32 may be

configured to implement one or more quantum-logic gates to operate on the quantum state held in qubit register 12. Whereas the function of each type of logic gate of a classical computer system is described according to a corresponding truth table, the function of each type of quantum gate is described by a corresponding operator matrix. The operator matrix operates on (*i.e.*, multiplies) the complex vector representing the qubit register state and effects a specified rotation of that vector in Hilbert space.

[0033] For example, the Hadamard gate HAD is defined by

$$\mathrm{HAD} = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}. \qquad (1)$$

[0034] The HAD gate acts on a single qubit; it maps the basis state $|0\rangle$ to $(|0\rangle + |1\rangle)/\sqrt{2}$, and maps $|1\rangle$ to $(|0\rangle - |1\rangle)/\sqrt{2}$. Accordingly, the HAD gate creates a superposition of states that, when measured, have equal probability of revealing $|0\rangle$ or $|1\rangle$.

[0035] The phase gate *S* is defined by

$$S = \begin{bmatrix} 1 & 0 \\ 0 & e^{i\pi/2} \end{bmatrix}. \qquad (2)$$

[0036] The *S* gate leaves the basis state $|0\rangle$ unchanged but maps $|1\rangle$ to $e^{i\pi/2}|1\rangle$. Accordingly, the probability of measuring either $|0\rangle$ or $|1\rangle$ is unchanged by this gate, but the phase of the quantum state of the qubit is shifted. This is equivalent to rotating ψ by 90 degrees along a circle of latitude on the Bloch sphere of FIG. 2.

[0037] Some quantum gates operate on two or more qubits. The SWAP gate, for example, acts on two distinct qubits and swaps their values. This gate is defined by

$$\mathrm{SWAP} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}. \qquad (3)$$

[0038] The foregoing list of quantum gates and associated operator matrices is non-exhaustive, but is provided for ease of illustration. Other quantum gates include *Pauli-X*, *-Y, and -Z* gates, the $\sqrt{\mathrm{NOT}}$ gate, additional phase-shift gates, the $\sqrt{\mathrm{SWAP}}$ gate, controlled *cX*, *cY*, and *cZ* gates, and the Toffoli, Fredkin, Ising, and Deutsch gates, as non-limiting examples.

[0039] Continuing in FIG. 1, suitably configured signal from modulators 34 of quantum interface 32 may interact physically with one or more qubits 14 of qubit register 12 so as to assert any desired quantum-gate operation. As noted above, the desired quantum-gate operations are specifically defined rotations of a complex vector representing the qubit register state. In order to effect a desired rotation *O*, one or more modulators of quantum

interface 32 may apply a predetermined signal level S_i for a predetermined duration T_i. In some examples, plural signal levels may be applied for plural sequenced or otherwise associated durations, as shown in FIG. 3, to assert a quantum-gate operation on one or more qubits of the qubit register. In general, each signal level S_i and each duration T_i is a control parameter adjustable by appropriate programming of controller 18A.

[0040] The term 'oracle' is used herein to describe a predetermined sequence of elementary quantum-gate and/or measurement operations executable by quantum computer 10. An oracle may be used to transform the quantum state of qubit register 12 to effect a classical or non-elementary quantum-gate operation or to apply a density operator, for example. In some examples, an oracle may be used to enact a predefined 'black-box' operation $f(x)$, which may be incorporated in a complex sequence of operations. To ensure adjoint operation, an oracle mapping n input qubits $|x\rangle$ to m output or ancilla qubits $|y\rangle = f(x)$ may be defined as a quantum gate $O(|x\rangle \otimes |y\rangle)$ operating on the $n + m$ qubits. In this case, O may be configured to pass the n input qubits unchanged but combine the result of the operation $f(x)$ with the ancillary qubits via an XOR operation, such that $O(|x\rangle \otimes |y\rangle) = |x\rangle \otimes |y + f(x)\rangle$. As described further below, a state-preparation oracle is an oracle configured to generate a quantum state of specified qubit length.

[0041] Implicit in the description herein is that each qubit 14 of qubit register 12 may be interrogated via quantum interface 32 so as to reveal with confidence the standard basis vector $|0\rangle$ or $|1\rangle$ that characterizes the quantum state of that qubit. In some implementations, however, measurement of the quantum state of a physical qubit may be subject to error. Accordingly, any qubit 14 may be implemented as a logical qubit, which includes a grouping of physical qubits measured according to an error-correcting oracle that reveals the quantum state of the logical qubit with confidence.

Topological Quantum Computer

[0042] In a topological quantum computer, the quantum state held in each qubit is a state of two or more braidable quasiparticles, or 'anyons', observed within a non-Abelian topological phase of matter. The world lines of different anyons are quantum mechanically forbidden from intersecting or merging. This feature forces their paths to form stable braids that pass around each other in space-time. Relative to trapped particles used in other types of quantum computers, anyon braids are more resistant to quantum decoherence, which is a source of error in quantum computation. However, the realization of a topological quantum computer requires the ability to engineer a suitable topological phase and to manipulate the

anyons therein.

[0043] Early experiments in topological quantum computing focused on the two-dimensional 'electron gas' of a supercooled, thin layer of gallium arsenide (GaAs) sandwiched between layers of aluminum gallium arsenide (AlGaAs) and manipulated in a strong magnetic field. Implementation of a quantum computer using that architecture would require the braiding of individual quasiparticle excitations combined with anyonic interferometry-based measurement, involving coherent quasiparticle transport over significant distances.

[0044] Proposed more recently is a one-dimensional topological qubit architecture that appears to be more amenable to practical implementation. The proposed system uses a semiconductor-superconductor heterostructure wherein superconductivity, strong spin-orbit coupling, and magnetic fields cooperate to form a topological, superconducting state that supports Majorana zero modes (MZMs). This new architecture obviates the need to move quasiparticles by employing a 'measurement-only' method wherein a sequence of measurements has the same effect as a braiding operation. This architecture does not require quasiparticles to be moved through an interferometry loop, but rather exploits a distinction between a 'fermion parity-protected topological phase' (the actual genus of the proposed heterostructure) and a true topological phase. Advantageously, topological charge in a fermion parity-protected topological phase can be manipulated by the process of electron tunneling into a MZM. Transport through a pair of MZMs can provide a measurement of their combined topological charge in the presence of a large charging energy.

[0045] In view of these and other useful properties, MZMs may be used as a basis for the qubits of a topological quantum computer. The MZMs are created at the ends of semiconductor-superconductor heterostructures tuned into a topological regime by the appropriate magnetic field and gate voltages. A series of practical implementations are described in Karzig et al., *Scalable Designs for Quasiparticle-Poisoning-Protected Topological Quantum Computation with Majorana Zero Modes*, arXiv:1610.05289v4 [cond-mat.mes-hall] 21 Jun 2017. Suitable heterostructure materials and material properties are described in Lutchyn et al., *Majorana Fermions and a Topological Phase Transition in Semiconductor-Superconductor Heterostructures*, arXiv:1002.4033v2 [cond-mat.supr-con] 13 Aug 2010.

[0046] Example implementations include at least two topological superconducting segments in a qubit, totaling at least four Majorana zero modes per qubit. The states used for quantum computation will be the degenerate ground states of the qubit, in contrast to

non-degenerate quantum-computing architectures where the two states of the qubit have different energies. The degeneracy of the qubit states and the spatial separation of the Majorana zero modes ensure long coherence times and feasibility of precise application of a set of Clifford gates.

[0047] FIG. 4 illustrates an example of a topological qubit architecture comprising a linear tetron array 38. The linear tetron array includes segments 40 and 42 comprising a classical superconductor, such as aluminum (Al), segments 44 comprising a semiconductor, such as indium arsenide (InAs) or indium antimonide (InSb), and a plurality of MZMs 46. The length ℓ_c of the non-topological segments is much larger than the corresponding coherence length ξ_c of the non-topological regions, and the length ℓ_t of the topological segments is much larger than the coherence length ξ of the topological regions. The dashed box in FIG. 4 represents a single qubit in the form of a linear tetron. Additional topological superconducting links and semiconducting structures allow appropriate measurements to manipulate and entangle the linear tetrons.

[0048] Qubit structures as shown in FIG. 4 are difficult to fabricate with the degree of reproducibility required for practical quantum computing. Due to material or fabrication defects, some candidate structures may fail to operate in the desired topologic regime. Even for candidate structures that do operate in the desired topologic regime, the appropriate terminal-bias and magnetic-field levels required for qubit operation cannot always be predicted *a priori*. Accordingly, candidate semiconductor-superconductor heterojunctions must be 'pre-screened' for appropriate topologic behavior, and successful heterojunctions must be 'tuned' to discover the appropriate operating parameters, before being incorporated into a qubit register.

Method Overview

[0049] This disclosure provides a method for pre-screening and tuning a candidate semiconductor-superconductor heterojunction for a topological qubit. The method includes a procedure for extracting the 'topological gap' of the candidate heterojunction (*vide infra*) using at least two stages of measurement followed by analysis. The measurement is enacted on a device having three current-carrying contacts, one of which is superconducting (a 'three-terminal device' herein). The 'mapping' phase of this method includes a fast RF measurement that roughly identifies promising regions. The subsequent 'refinement' phase includes a slower sub-RF (*e.g.*, DC) measurement performed on each of the promising regions identified in the mapping phase. In some examples, the method uses density-based clustering algorithms on two-sided zero-bias peak (ZBP) data to extract predicted

topological regions and classification of bias traces using peak finding or machine learning. It improves the accuracy of previous methods by checking the stability of the ZBP to variations in cutter gate voltage and by checking for gap closing at the boundary of the suspected topological region. Meta-analysis of the ZBP data is used to extract the probability of finding a topological region across many devices of the same preparation. This feature can be used for characterizing the growth and/or fabrication method for topological qubit structures.

[0050] As used herein, a 'false positive' identifies a trivial system as topological, whereas a 'false negative' identifies a topological system as trivial. The technique herein improves over the basic ZBP search by including a separate ZBP search on both sides of the three-terminal device, thereby reducing the probability of false positives. It also includes non-local measurements to extract the energy gap in the candidate system, providing additional information for detection of a topological gap. Lastly, it includes non-discriminant measurement within regions of the parameter space that have pre-defined boundaries, thereby excluding false-positives deriving from confirmation and selection biases (which could occur if the measurement region were human-selected).

[0051] FIG. 5 shows aspects of an example semiconductor-superconductor heterojunction device 48 evaluated according to the methods herein. Generally speaking, a semiconductor-superconductor heterojunction suitable for testing comprises at least three terminals supporting electronic admittance and conductance measurements, in addition to a plurality of electrostatic control terminals. Device 48 of FIG. 5 is a three-terminal device comprising a topological middle segment 50 coupled to ground probe 52 through a trivial superconductor, and two normal probes, 54R and 54L coupled to the two ends of a semiconductor wire. This geometry allows simultaneous measurement of the tunneling signatures of the topological phase at the two ends of middle segment 50, for correlation to the zero-bias features on the two sides. Further, the non-local signal between the two normal probes provides information about the lowest energy of the extended states of the topological segment, which may be used as a proxy for the topological gap (*e.g.*, in a sufficiently long semiconductor wire, the non-local signal sets in at bias values corresponding to the lowest energy extended mode in the wire.). Accordingly, the method herein does not *directly* measure the topological character of a system but instead measures a set of surrogate variables, which, from analytical calculations and numerical simulations, are known to correlate well to the topological invariant. The surrogate criteria for identifying a topologically non-trivial region are as follows:

[0052] 1. Correlated zero-bias differential conductance peaks occur on both sides of the device throughout a topological region with well-separated Majoranas.

[0053] 2. For low values of the magnetic field, the bulk of the system is gapped. As the magnetic field is increased, the bulk gap should close and reopen in the topological region. The value of the energy gap in the bulk of the wire can be detected in a three-terminal device via a non-local conductance measurement.

[0054] Within a region in parameter space that fulfills the criteria for being topological, the magnitude of the bulk gap varies. The operational meaning of the term 'topological gap' in the context of this disclosure is the magnitude of the maximum bulk gap in such a topological region.

[0055] To be able to distinguish between topological and non-topological systems, the method must correctly identify topological regions in idealized numerical test data sets. Accordingly, the methods herein show high overlap between the topologically identified region and the numerically determined topological index (as demonstrated in FIG. 10, for example). Further, the method must correctly label currently known candidates for false positive signatures as non-topological. These include:

[0056] 1. Trivial local bound states induced by cutters, impurities or smooth potentials (*e.g.*, pairs of quasi-Majorana modes at the ends of the device), which are examples of non-topological zero-bias peaks;

[0057] 2. Disorder-induced low energy subgap states (non-topological zero-bias peaks and possible accidental gap-closing/reopening features);

[0058] 3. Trivial gap closing without proper reopening in finite-size systems (*e.g.*, a Coulomb-blockaded system) where a finite-size gap closes at small fields and gives rise to oscillations of low-energy states (false gap closing/reopening feature); and

[0059] 4. Trivial accidental closing-like features caused by a set of discrete states crossing zero energy (false gap-closing/reopening feature).

[0060] The way that the method reduces such false positives is by using data collected over a large range of parameter values. Accidental or fine-tuned points should not persist under change of parameter values, as a topological phase does. Moreover, the method correlates different indicators of the topological phase, as both of the above criteria are to be verified—*viz.*, zero-bias conductance peaks have to be present simultaneously at both ends, and the

system needs to show a gap closing and reopening feature in the non-local conductance. Given those criteria, the above false positives can be correctly identified, since:

[0061] 1. False positives 1 and 2 in the enumeration above lack a gap-closing/reopening feature in the non-local conductance; and

[0062] 2. False positives 3 and 4 lack correlated and stable zero-bias peaks at both ends of the semiconductor wire.

[0063] Simultaneous occurrence of different types of false positives is not expected to be stable to variations across the parameter space.

[0064] A remaining concern of the method is to prevent false negatives, which are addressed further below. In particular, a specifically constructed example combining features 1 and 4 with false-positive regions is addressed, along with an example relating to a strongly disordered system. While disorder can lead to zero-bias peaks, it will in general not lead to extended regions of correlated ZBPs. Similar stability requirements rule out the potential false positive 3 in the above enumeration.

[0065] The method is guided by the following principles:

[0066] 1. The method must guarantee that both criteria enumerated above can be verified.

[0067] 2. Measuring as wide a range as possible of the parameter space of the device is required because:

[0068] a. The initial uncertainty over the presence and position of the topological phases can be high.

[0069] b. Checking the stability of zero-bias peaks in parameter space helps to rule out possible false positives.

[0070] c. It reduces unwanted selection bias.

[0071] 3. The method should be completed in a reasonable amount of time (days at most), and require minimal human decision making during its implementation.

[0072] 4. Non-local conductance measurements are currently much slower than local measurements, and therefore should be limited to promising candidate regions, so that the method can be completed in a reasonable time.

[0073] 5. For a given execution of the method, the sequence of measurements should be pre-determined and have a finite length, in order to prevent open-ended searches which, especially given the large parameter space, can take a long time and may introduce selection bias. It is still possible to allow for the

measurement sequence to be improved over time, for instance, by applying lessons learned in previous runs.

[0074] 6. For a given execution of the method, the data analysis procedure should be determined before the data is collected and inspected, and should have pre-determined outputs, in order to avoid over-fitting and confirmation bias, and to guarantee that the method has an outcome. Again, it is still possible to allow for the data analysis code to improve over time, for instance, by using improved algorithms and applying lessons learned in previous runs.

[0075] In view of the above considerations, FIG. 6 shows aspects of an example method 56 to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer. Method 56 includes a mapping phase 58 and a refinement phase 60. In some examples, the mapping and refinement phases may be enacted separately—*e.g.*, to evaluate a new experimental setup or a change in implementation.

[0076] Mapping phase 58 and refinement phase 60 each include measurement followed by analysis. The mapping phase includes fast RF measurement 62 of normal-superconductor (NS) junction admittances to provide mapping data. Measured quantities include the local conductance at each end of the semiconductor wire over a wide parameter space in bias, field, plunger and left/right cutter gate voltages. In some examples, the 'mapping data' from measurement 62 includes two 5D datasets of RF signal versus field, left cutter, right cutter, plunger, and left or right bias. The associated data analysis 64 then looks for extended regions in the parameter space where correlated ZBPs are present. In some examples, the output of analysis 64 includes a list of 'promising' regions in 4D parameter space (field, left cutter, right cutter, plunger), ranked by the likelihood that there is an unbroken topological phase with a finite topological gap within that region.

[0077] Each promising region identified in this manner is then further investigated, iteratively, in refinement phase 60. The refinement phase includes a slower sub-RF measurement 66 of the full conductance matrix within each promising region, using lock-in amplifiers and including local and non-local conductance. In some examples, the 'refinement data' from measurement 66 includes the full conductance matrix for each promising region as a function of bias. Associated data analysis 68 on the full conductance matrix, and in particular of the non-local conductance, yields information about the behavior of the bulk gap for identifying a region as topological according to the above criteria. It also allows quantitative assessment of the magnitude of the gap within each topological region.

In some examples, analysis 68 includes determination of the boundary of the topological phase within each measured region (or the absence of a topological phase) based on joint analysis of local and non-local conductance. Further, the value of the topological gap (if any) is determined for each region. In refinement phase 60, measurements over the promising regions may be repeated with adjusted ranges and resolution—*e.g.*, not indefinitely but only under appropriate circumstances. Accordingly, refinement phase 60 may include a heavily regulated feedback loop that adjusts the bias range and/or resolution in parameter space. The feedback loop may include a maximum of two iterations, for example.

[0078] On completion of refinement phase 60, a region having optimal properties of topological phase is identified. The region may be defined, for instance, by a combination of a large gap and high confidence of topological character. To further increase the confidence, an additional validation phase 70 may be enacted optionally, where the stability of the optimal region is put to additional testing. In some examples, validation phase 70 includes validating a ZBP in regions identified in refinement phase 60, by checking the stability of the ZBP to variations in cutter-gate voltage. Such variations may be of any desirable magnitude, including large variations. Furthermore, in examples in which the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, the validation phase may include meta-analysis of ZBP data across the series. The meta-analysis may be conducted in order to compute a probability of finding a topological region in other, analogously prepared semiconductor-superconductor heterojunctions.

[0079] As noted previously, the measurements in method 56 are made on three-terminal devices, as shown in FIG. 5. Some constraints on the device to be measured will now be discussed, with continued reference to that drawing. Device 48 of FIG. 5 includes a semiconductor wire 72, which is typically a nanowire. In some implementations, the semiconductor wire may comprise a selective-area grown (SAG) nanowire. In device 48, semiconductor nanowire 72 is proximitized by superconductor 74. The superconductor extends to the side, away from the hybrid wire. FIG. 5 shows representative locations of MZMs 75 in the scenario in which device 48 is operating in a topological regime. The 'T' shape of the superconductor is not necessarily required, and the width of the vertical superconducting section can extend over the entire length L of the device. The normal contacts 54R and 54L contact the semiconductor wire on each end of the device. Contact 52 is coupled to superconductor 74, making a device with three terminals, suitable for electrical

transport measurements. The entire device is covered in a dielectric layer (not shown in the drawing). Electrostatic cutter gates 76R and 76L are used to form tunnel barriers at each end of semiconductor wire 72. Electrostatic plunger gate 78 tunes the chemical potential inside the device.

[0080] In the illustrated example, important dimensions include:

[0081] L: the maximal length of the topological region,

[0082] L_S: the length of the superconducting segment connecting the topological region to the lead grounding superconductor 74,

[0083] W: the width W of semiconductor wire 72 (or more generally the cross section),

[0084] L_C: the distance between the cutter gates 76 and superconductor 74,

[0085] W_C: the width of each cutter gate 76,

[0086] L_N: the spacing between each cutter gate 76 and the associated normal lead 54.

[0087] The distance of plunger gate 78 from semiconductor wire 72 can be important for the lever arm and the potential profile within the semiconductor wire, also depending on the dielectric material used. Another variable is the geometry of plunger gate 78 with respect to the semiconductor wire (wrap gate versus side gate). If the plunger gate wraps around the semiconductor (wrap gate), then the lever arm will be larger, which allows the chemical potential inside the semiconductor wire to be changed by a larger amount. In turn, if the coupling of the plunger gate to the semiconductor wire is too strong, a small voltage noise on the plunger gate will have a larger effect, potentially artificially broadening the chemical potential inside semiconductor wire 72.

[0088] One of the most important parameters is the length L of the proximitized semiconductor wire. Here, two effects are competing against each other. On the one hand, the semiconductor wire needs to have a sufficient length to avoid finite-size effects and make the signatures of the topological phase transition and correlated ZBPs clear. On the other hand, longer wires will increase the practical difficulty of growing or fabricating a working device and may reduce the non-local signal. In particular, it will be more difficult to ensure sufficient homogeneity in the semiconductor wire and the absence of strong defects (like a bad contact to the superconductor suppressing the proximity effect) when the semiconductor wire length is increased. Little data is currently available for devices longer than 2 μm. From a theoretical point of view, 5ξ, where ξ is the topological coherence length, presents a minimal length scale where the finite-size effects are sufficiently suppressed.

Even in clean wires the non-local signal will be suppressed with increasing length of the semiconductor wire. The issues above will lead to a device-quality dependent upper bound on L for a successful extraction of non-local information.

[0089] The length L_S is chosen such that leakage of quasiparticles to the center lead is suppressed. A working estimate is $L_S > 10\xi_S$, where ξ_S is the coherence length of superconductor 74 (L_S = 200 nm for disordered Al). In typical experiments L_S can be up to the scale of millimeters, thus exceeding the minimum by several orders of magnitude.

[0090] Experimental evidence indicates that the distance L_C to cutter gate 76 must be well below 100 nm to avoid spurious end states and enable high-resolution tunneling spectroscopy. An optimal choice for L_C and the design of the cutter gate may be determined by combining simulations from electrostatics, realistic transport, and fabrication capabilities. As a place holder, the requirement $L_C < 40$ nm may be used. It should be noted that the cutter design may be varied in terms of width of the cutter W_C and distance between the cutter and the normal lead. For InSb wires, a reduced spacing between the cutter and the normal lead may be desired, since these wires are normally-off and the cutter has to open up this segment of the wire too.

[0091] Note that the parameter of wire width W is not necessarily important for the viability of the disclosed method but will influence the likelihood of getting a positive result from the method. For example, the width controls the number of channels, and numerical simulations show that fewer channels are beneficial to reach the topological phase.

[0092] Table 1 summarizes current estimates for the various requirements on device geometry in terms of the materials currently used, giving estimated material-specific requirements for device dimensions. For these values, the following estimates for the coherence length at the point of the maximal gap were used: ξ(InSb/Al) = 400 nm, ξ(InAs/Al) = 300 nm and ξ_S = 200 nm.

Quantity	InSb/Al	InAs/Al
L	> 2.0 μm	> 1.5 μm
L_S	> 2 μm	> 2 μm
L_C	< 40 nm	< 40 nm

[0093] An appropriate choice of materials is necessary to obtain a system with a sufficiently large topological gap. Method 56 is agnostic, however, to the semiconductor-wire material. While the material stack is still under investigation (both theoretically and

experimentally), current results indicate that InAs with a barrier material and InSb without a barrier are promising choices for obtaining a topological gap within a suitable range of energy. In some examples, a topological gap within a range of 25 to 200 μeV may be suitable to support the operation of a topological quantum computer. Narrower and broader ranges are also envisaged.

[0094] The current choice of superconductor is aluminum since it creates a hard induced gap in heterostructures with no subgap states at zero field. Again, the method is in large part agnostic to the choice of superconductor, as long as measurement parameters are adapted accordingly, for example, by extending the bias scan range for larger-gap superconductors or adjusting the dimensions of the device based on the values shown in Table 1.

[0095] The choice of the dielectric is very much dependent on the SAG material stack used. The hybrid system places limits on the temperature that a given material stack can be exposed to. The maximal gate voltage that can be applied to the electrostatic gates before the dielectric breaks down (breakdown voltage V_{break}) is an important material quantity, which preferably is known for a given dielectric layer and SAG material system, as it sets fundamental limits on device operation. Breakdown voltages can either be measured on a test device or determined by standard electrical characterization (SEC) measurements. If experimentally feasible, one recommendation is to fabricate, nearby on the same chip, an identical device to the device under test, to allow for a measurement of a realistic V_{break}.

[0096] Returning now to FIG. 6, before a device is subjected to detailed measurement, the device may be qualified in order to determine that it meets a set of criteria. Accordingly, method 56 includes an initial qualification phase 80. The initial qualification phase may include preliminary assessment of conductance, tunnel spectroscopy, and time stability, as described below.

[0097] With regard to device conductance, the device is considered conducting if the resistance through the device is < 25 kΩ between all three terminals, measured at high bias voltage $V_{bias,high} > 2\Delta$, where Δ is the superconducting gap. For InSb-based devices, this may require initially opening the channel by applying positive voltages to the cutter gates. With regard to gate pinch-off, all gate resistances should be > 500 MΩ to ground. All gates used to form a tunnel barrier (cutters) have to pinch off the device individually. To test the gate pinch-off, conductance between the superconducting terminal and the corresponding normal terminal is measured as a function of cutter gate voltage at high bias. The device is considered pinched off when a conductance < 0.005 e^2/h is reached. The plunger gate, used to tune the chemical potential in the topological segment should be able to tune the

conductance through the device, to some extent. The effect of the plunger gate can be most easily tested in the tunneling regime, using tunnel spectroscopy as described further below. Hysteresis on both cutter gates and plunger gates may be acceptable, since all measurements can be performed in the same sweep direction. However, it is required that after a hysteresis loop on either gate, states do not measurably shift in gate space, as detailed hereinafter.

[0098] With regard to tunnel spectroscopy, once the cutter gates have been tuned to a regime where the high-bias conductance is on the order of 0.1 e^2/h, conductance as a function of bias and a gate voltage (either plunger or tunnel gate) is measured at zero magnetic field. Peaks in the differential conductance versus bias should be clearly identifiable at a bias around the expected induced superconducting gap and should not change position for small gate voltage changes (given that the high-bias conductance does not change by a large amount). At zero field and at energies below the superconducting gap, the number of finite conductance features should be low, to reduce the probability of false positives. Ideally, the zero-field conductance traces should be devoid of discrete subgap state features. This can be quantified by requiring average subgap conductance to be below 1/4 of the high-bias conductance.

[0099] With regard to time stability, in the tunneling regime the high-bias conductance should be stable. This means the conductance should not jump or drift by more than $\Delta g \sim 0.2$ e^2/h on a timescale of $t = 10$ minutes. With regard to RF response, the resonances used for the fast RF measurements should be identified for a specific device, for example, by comparing the resonances in the open versus the pinched-off regime. For all terminals where fast measurements are needed, a clear response of one resonance as a function of the corresponding tunnel gate should be visible. Effective impedance matching is necessary in order to obtain optimal sensitivity to changes in conductance. Based on typical device resistances of $\gtrsim$ 100 kΩ and resonator inductance values on the order of 200 nH, the parasitic capacitance of the devices should be less than 1 pF to allow for high sensitivity.

[00100] Returning briefly to FIG. 6, measurement 62 of mapping phase 58 may include benchmarking of electrical noise and energy broadening. This step is valuable because energy broadening due to the measurement setup will provide a lower bound on the detectable topological gap. To ensure that broadening due to electrical noise is negligible, the integrated voltage noise RMS amplitude between 1 Hz and 500 Hz should be smaller than 3 μV.

[00101] FIG. 7 shows aspects of an example measurement setup for RF reflectometry. In RF reflectometry measurements, the sample is bonded via a resonator to a transmission line.

The sample resistance alters the impedance matching of the resonator to the transmission line, changing the reflection coefficient of RF signals sent into the line. Each of the two normal conducting leads of the device are bonded to a resonator for RF reflectometry measurements, which have resonant frequencies $f_{l,res}$ and $f_{r,res}$ for the left and right side, respectively. The frequency difference between these resonators on the left and the right sides should be greater than the line width of each resonator. The intermediate-frequency (IF) source generates RF pulses within the frequency bandwidth of the readout system. These pulses are up-converted to the frequency range of the resonators bonded to the device. For this, a mixer with high (> 30 dB) carrier suppression mixes the IF signal with a local oscillator (LO) signal. The LO frequency must bridge the frequency difference between the bandwidth of the acquisition system f_{ADC} and both resonator frequencies $f_{l,res}$ and $f_{r,res}$.

[00102] If the RF source does not have separate I and Q outputs, one of the up-converted sidebands must be filtered away. This can be done by choosing $f_{LO} > \max f_{l,res}, f_{r,res}$ and installing a low-pass filter with cutoff frequency $= f_{LO}$ between the up-conversion mixer and the input port of the fridge. After the signal gets reflected from the sample, it goes through a low-noise amplifier. Then it gets down-converted with a mixer using the original LO signal, low-pass filtered to the bandwidth of the acquisition system, and sent to the input of the acquisition system.

[00103] In order to measure local conductance with RF reflectometry, the reflected RF signal values must be calibrated against the directly measured differential conductance, for instance with lock-in amplifiers at low frequency. Since this is a sample-dependent procedure that can be performed in parallel with the actual measurement, it is described hereinafter, together with the measurement operations.

[00104] In order to benefit from fast acquisition rates, the gate and bias voltage scans on the device are triggered by hardware, to minimize the time spent on software communication (typically on the order of 10 ms). This can be done in a hardware-triggered two-dimensional scan synchronized with the acquisition system. One voltage is ramped with a saw-tooth function and sampled N times during each ramp, while a second voltage is at a slower rate during M cycles of the faster ramps, resulting in a $N \times M$ points scan. In order to be compatible with DC values of voltages applied on the contacts and gates, these voltage scans are applied on low-pass filtered DC lines. The fastest ramping rate must be below the cutoff frequency of the low-pass filters in the fridge lines, typically 1 kHz.

Mapping phase 58 in detail

[00105] FIG. 8 shows additional aspects of measuring the radio-frequency (RF) junction

admittance of the semiconductor-superconductor heterojunction to obtain mapping data. Method 62A of FIG. 8 illustrates fast measurement of local conductances by RF reflectometry, enacted in order to satisfy the first of the two topological gap criteria specified hereinabove, as it allows rapid characterization of a device and identification of candidates for topological regions based on correlations of ZBPs. The identification of these regions sets the stage for the non-local measurements of refinement phase 60. The fast local measurement for the three-terminal device is closely related to the fast measurement of a conventional NS junction.

[00106] At 82 of method 62A, the magnetic field is set to 0 T. At 84, for each side of the three-terminal device, the reflected RF signal is measured at a large bias voltage (for instance, 1 mV) as a function of frequency around the estimated resonance frequency (100 MHz to each side) and the corresponding cutter voltage from the open-channel setpoint (*i.e.*, typically 0 V for InAs and 1 V for InSb) to 100 mV beyond full pinch-off voltage. The resonance frequency f_{res} is identified as the frequency with the steepest change in signal as a function of cutter gate voltage, and the cutter voltage $V_{tunn,res}$ where the dip in the reflected signal as a function of frequency has the minimum absolute value.

[00107] At 86 the frequency is fixed at f_{res}, and the cutter voltage range, $V_{c,min}$ to $V_{c,max}$, that satisfies the following three conditions is determined:

[00108] a. The range is hysteresis-free as measured by reproducibility of measurements after a hysteresis loop.

[00109] b. The local conductance measured well above the superconducting gap (*e.g.*, at 1 mV for Al) is between 0.05 e^2/h and 0.2 e^2/h.

[00110] c. The non-local conductance signal measured via standard low-frequency lock-in amplifier techniques is above the noise level.

[00111] For significant electrostatic cross-talk between plunger and cutter (geometry and material specific), this step may be repeated for different values of the plunger-gate voltage.

[00112] At 88 the RF readout power is optimized. In some examples, this action includes finding a region in cutter space that shows a clear gap with well-defined coherence peaks. To that end, the RF readout power on each side is scanned, measured at the sample (bottom of the fridge), from -80 dBm to -130 dBm in 1 dB steps. For each RF power, a fast scan of the bias voltage is made on the respective side from $-1.5\Delta_0$ to $1.5\Delta_0$ (Δ_0 being the gap of the parent superconductor leading to a bias range -350 μV to 350 μV for Al), with a maximum step size of 5 μV and measure the reflected RF signal. For each side, the maximum RF power that does not broaden the features in the measurement is found, *e.g.*, the coherence

peaks, and set as the working RF power.

[00113] At 90 the magnetic field angle is calibrated so as to be parallel to the semiconductor wire. To this end, the magnetic field is set to a value at which the superconducting gap is not closed for a field parallel to the semiconductor wire, but is greatly reduced in size for a field perpendicular to the semiconductor wire, *e.g.*, 500 mT for InAs and InSb SAG. The magnetic field angle is scanned around the expected value from the wire geometry, and for each value of the angle, the bias on one side of the device is scanned from $-1.5\Delta_0$ to $+1.5\Delta_0$ (-350 μV to $+350$ μV for Al) with a maximum step size of 5 μV. The reflected RF signal is then measured. The field angle is set to the one that yields the maximum gap size. Here the aim is for an alignment accuracy of better than 2° in both azimuthal and polar angles.

[00114] At 92 the maximum magnetic field B_{max} where the superconductor bulk gap closes is determined. At 94 the magnetic field is scanned from 0 T to B_{max} in steps of 100 mT to perform the RF-DC calibration. For each field value, the following additional calibration is performed.

[00115] At 96 the optimal RF readout frequency is measured. This can be done as a repetition of step 84. However, once the readout frequency has been identified, a quicker method can be followed. In one example, the cutter gate voltage is set to $V_{c,res}$ where the dip in the reflected RF signal as a function of frequency had the minimum absolute value at zero field. The RF reflected signal is measured as a function of RF frequency, from 50 MHz to each side of the resonance frequency found for the latest field value. The dip in magnitude of the RF signal closest to the previously found dip is found and set as the RF readout frequency. The result of this measurement may be saved to the database.

[00116] At 98 an RF-DC calibration curve is measured. On each side, the bias voltage is set to high bias (*e.g.*, 1 mV for Al), to be above the superconducting gap. The respective cutter gate voltage is scanned from the open-channel setpoint (*i.e.*, typically 0 V for InAs and 1 V for InSb) to 100 mV beyond pinch-off voltage. For each cutter voltage, the local conductance is measured with a lock-in amplifier on the respective side as well as the reflected RF signal. The result of this measurement is saved to the database to later establish the calibration function between reflected RF signal and conductance.

[00117] At 100 the magnetic field is set to 0 T again. At 102 the magnetic field is ramped from 0 T to B_{max} in steps of ΔB. The field step ΔB depends on the g factor and is such that states moving with field can be tracked. A reasonable range for InAs or InSb SAG is 10 mT $\leq \Delta B \leq$ 50 mT. For each value of the field, the following additional steps are performed.

[00118] At 104 the cutter gate potentials are scanned from $V_{c,min}$ to $V_{c,max}$ in $N_c = 15$ steps on each side independently, to yield a total of $2N_c$ configurations. Such an independent scan is justified for local conductance measurements when the lever arm for cutter-plunger cross talk and the range of the cutter gate scan is small enough to not change the effective plunger voltage by more than the size of a plunger voltage step. For each cutter gate configuration, the following measurement is performed. The voltage limits $V_{c,min}$ and $V_{c,max}$ are as determined at 86.

[00119] At 106 a fast scan of plunger voltage and bias voltage on each side is performed. The plunger voltage is scanned from $V_{p,max}$ to $V_{p,min}$. The plunger bounds are material specific and are limited by the upper and lower breakdown voltage (stop at 80% of breakdown voltage V_{break}) and by the possible range of interesting regions. The latter ranges from the fully gapless regime to full depletion and requires theory input. The resolution of the plunger scan needs to be sufficient to resolve individual subgap states crossing the gap (lever arm dependent). For each value of the plunger gate, the bias voltage at that terminal is scanned from $-1.5\Delta_0$ to $+1.5\Delta_0$ (-350 μV to $+350$ μV for Al)) with a resolution no larger than 5 μV. The reflected RF signal is measured as a function of plunger and bias voltage. The resulting two-dimensional scan is saved into the database.

[00120] The mapping data generated as an output of method 62A includes the following:

[00121] 1. A calibration dataset consisting of two 2D cutter-field scans, on the left and right sides. For each point of this scan, three parameters are measured: RF in-phase component, RF out-of-phase component, and conductance of the respective side.

[00122] 2. A measurement dataset including two 5D field-left-cutter-right cutter-plunger-bias scans, where the bias scan is taken on the left and on the right. For each point of this scan, two parameters are measured: RF in-phase component and RF out-of-phase component.

[00123] The goal of data analysis at this stage is to identify the promising regions in the parameter space that are likely to contain an unbroken topological phase. FIG. 9 shows additional aspects of finding, by analysis of the mapping data, one or more regions of a parameter space consistent with an unbroken topological phase of a semiconductor-superconductor heterojunction.

[00124] At 108 of method 64A, the RF signal input is converted into conductance using the calibration dataset to define a transfer function. At 110 each point in the (field, plunger, cutter) parameter space is classified as (potentially) topological or trivial, using as inputthe

local conductances of the respective left and right terminals, G_{ll}, G_{rr}, from bias traces measured at that point. In one example, the classification may check for the presence of ZBPs in both conductance traces.

[00125] Analysis of the mapping data includes density-based clustering on two-sided ZBP data. At 112 clusters of points that have been classified as topological are found, and clusters whose volume or shapes in parameter space are deemed incompatible with a topological phase are filtered out. In some examples, the cluster volume must be larger than 0.03 V × T in the plunger voltage-magnetic field space. The clusters that survive the filtering are promising regions for the presence of topological phases. In some examples, this step may be implemented using density-based clustering for every 2D plunger-field scan, and may exclude regions that extend to zero magnetic field. At 114 the promising regions are ranked by the likelihood that they contain a topological phase. In some examples, the ranking score is determined by the average plunger gate voltage of each cluster, with priority being associated with more negative gate voltages.

[00126] FIG. 10 shows aspects of analysis of mapping data according to method 64A. The analysis is illustrated and verified using a simulated dataset of an InSb/Al nanowire with length L = 3 μm and a mean free path of 3 μm. From left to right as functions of plunger gate (in V) and magnetic field (in T) the figure shows: topological index Q as calculated from scattering matrix; a binary array where 1 corresponds to the ZBP present on both sides of the device; and clustered ZBP Boolean data with the cluster color corresponding to the score of the corresponding cluster (smaller corresponding to better). With such data, it is possible to find regions that include a true topological region, for further analysis.

[00127] The results of the data analysis performed in mapping phase 58 of method 56 determine the measurements to be taken in the subsequent refinement phase 60. For each promising region in the above ranking, ranges in field, plunger and cutter values that enclose the region are specified as input for the refinement phase. In some examples, the refinement phase may be performed on the various identified regions in the ranking order. It is necessary to minimize the wait time between the end of the measurements in the mapping phase and the beginning of the measurements in the refinement phase, in order to minimize the effect of gate drifts, gate jumps and other problems that may occur while the device is idle. For this reason, it is important for the data analysis outlined above to be executed in a time-efficient manner. Note that the raw data generated in the RF measurement phase can be quite large: existing RF datasets of this kind exceed 100 GB in total size, with reduction and analysis spanning a few hours. Therefore, it is important that a data pipeline is in place

to make the data quickly available for analysis on a computational cluster, in order to avoid bottlenecks in the execution of the method. Note that the implementation of the pipeline may require different solutions for measurements done at different sites. The acquisition, transfer, and analysis of data should also be parallelized as much as possible. For instance, the first step in the data analysis outlined above can occur in parallel with the data acquisition, as it requires individual bias traces as input.

Refinement phase 60 in detail

[00128] The differential conductance of the device being evaluated can be measured using standard, low-frequency lock-in amplifier techniques, as represented in FIG. 11. The full conductance matrix is measured by applying a DC bias voltage $V_{bias,l/r}$ and an AC voltage $\delta V_{l/r}$ at the left and right terminals 54, respectively, with two different AC excitation frequencies, f_l and f_r. These frequencies must be lower than the low-pass filter cutoff values in the system and low enough to minimize parasitic capacitance effects. To ensure this, the phase shift of the current with respect to the voltage excitation must be less than 10°. The in-phase AC current $\delta I_{l/r}$ flowing to the left or right side is measured with the middle superconducting lead grounded. It is necessary that the connection to ground is low-ohmic (*i.e.*, typically less than a few kΩ) compared to the resistance of the other two lines, in order to suppress spurious voltage divider effects. To that end, either the low-pass filters may be designed accordingly or the superconducting lead may be grounded at the PCB level (cold ground).

[00129] This three-terminal setup allows measurement of all four elements of the conductance matrix G between the left (l) and right (r) terminals:

$$G = \begin{pmatrix} dI_l/dV_l & dI_l/dV_r \\ dI_r/dV_l & dI_r/dV_r \end{pmatrix}. \qquad (4)$$

[00130] The conductance matrix elements $G_{ll} = dI_l/dV_l$ and $G_{rr} = dI_r/dV_r$ are referred to as 'local conductance' and the elements $G_{lr} = dI_l/dV_r$ and $G_{rl} = dI_l/dV_r$ as 'non-local conductance'.

[00131] The input for refinement measurement 66 includes a region in (cutter gate, plunger gate, field) space that is a candidate for further investigation. The size of the regions in plunger gate/field space may be increased by a 20%, in some examples, to ensure that the refinement measurements fully capture the topological phase transition surrounding each region.

[00132] FIG. 12 shows additional aspects of measuring a sub-RF conductance of the semiconductor-superconductor heterojunction in each of the one or more mapped regions

of the parameter space, to obtain refinement data. In particular, method 66A describes local and non-local conductance measurements suitable for extracting an energy gap of the semiconductor-superconductor heterojunction.

[00133] At 116 of method 66A, the magnetic field is set to the minimum field value in the candidate region. This field should be low enough that the induced gap is still open, for the purpose of observing whether it closes in the candidate region. At 118 the cutter gate is set to its median value, for instance, in the candidate region. At 120 a correction is applied for small bias voltage offsets of V_L and V_R (*cf.* FIG. 11), to ensure that the extraction of the antisymmetric component of the local and non-local signals is straightforward. This can be achieved by finding the minimum of the summed absolute currents ($|I_L| + |I_R|$) in the V_L-V_R parameter space. At 122 the magnetic field is ramped in the candidate region in steps of ΔB. For each value of the field, the bias-plunger scan is performed as described immediately below.

[00134] At 124 the plunger voltage is set to the maximum plunger voltage in the region to be explored ($V_{p,max}$). The plunger voltage is scanned from V_{max} to the minimum plunger voltage in the region to be explored, $V_{p,min}$, in steps of ΔV_p. In other examples, the plunger voltage may be scanned in the opposite direction. For each plunger voltage value, the bias voltage on the left terminal is scanned from –50 μV to +50 μV in steps of 5 μV. If the data indicates that the topological gap is outside of this window, then the scan is repeated with larger window size. The resulting two-dimensional scan is saved into the database.

[00135] The refinement data generated by the slower full-conductance matrix measurement is a dataset per candidate region. Each dataset consists of two 3D field-plunger-bias scans, where the bias is scanned separately on the left and the right sides. For each point in the scan, two parameters are measured: conductance on the left and on the right sides. In some examples, each conductance may comprise the full conductance matrix for the corresponding side of the device.

[00136] FIG. 13 shows additional aspects of finding, by analysis of the refinement data, a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space interrogated in method 66A. In some examples, the illustrated method is performed iteratively for each promising region.

[00137] At 126 of method 68A, step 110 of method 64A is repeated in order to verify that the measured region is still promising, and potentially to adjust the boundaries of the candidate topological region. At this point, analysis of the refinement data includes

verifying gap closure at the boundary of each of the one or more regions of the parameter space. At 128 a check is performed to determine what fraction of the boundary of the promising region is gapless, based on the non-local conductance signal. At 130 the size of the gap $\Delta^{(j)}$ for each point i within the region j is extracted by thresholding the non-local conductance. At 132, based on the extent of a gapless boundary, and on the value of the gap within the candidate topological region, a score is assigned to the region. The score reflects the likelihood that the promising region is indeed topological and gapped. In some examples, the score S is defined by $S_i = X \cdot \text{median}_i(\Delta^{(j)})$. At 134 the largest gap inside each topological region is obtained, together with an estimate of the error. In some examples, the error bar is dictated by the uncertainty in the thresholding of non-local conductance at the point of the largest gap.

[00138] The output of this analysis includes a set of probabilities corresponding to the regions identified in mapping phase 58 of method 56—*viz.*, the probability of hosting an unbroken topological phase. Associated with each probability is the maximal (topological) gap inside each of the (non-trivial) regions. FIG. 14 shows aspects of analysis of refinement data according to method 68A, using the same simulation as in FIG. 10. From left to right: gap extracted from the non-local data; score of the ZBP clusters as defined by average gap within the region times the percentage of the boundary that is gapless; and score of the ZBP clusters, same as the middle figure, but with average gap replaced by the median gap in the region. The maximal gap within the region is 175 μeV. Accordingly, the output of the overall method 56 is an estimate for the value of the topological gap in each promising region and its position in the explored parameter space.

Detailed examples of false positives and false negatives

[00139] One possible issue of quasi-Majoranas is that they can occur as precursors of a true topological regime. This means a topological region could be directly adjacent (in parameter space) to a non-topological quasi-Majorana regime. In that case, the current algorithm that clusters regions of correlated ZBPs could identify a region that is too large in the mapping phase. In other words, while containing the topological region, the identified region could extend much farther, including some of the quasi-Majorana regime. In that case, the current analysis in the refinement phase is set up to fail by either identifying too much of parameter space as topological or not recognizing the topological regions because of the absence of gap closing/reopening in the quasi-Majorana regime.

[00140] A solution to this problem is to implement another clustering algorithm in the refinement phase that identifies lines of gap-closing/reopening features in parameter space

(specifically in field-plunger space), and then determine intersections of these lines with the regions of correlated ZBPs to find topological phases. Note that this is mostly a problem of data analysis in the refinement phase. The mapping phase is still suitable for identifying promising regions of data that are examined more closely in the refinement phase.

[00141] Unstable behavior in data analysis may result from cuts of the data for a fixed cutter voltage. Stability can be improved by using one or both cutter-gate potentials as additional dimensions in refinement data analysis 68. This should improve clustering and make better use of the available dataset.

[00142] The following example addresses smooth potentials at the ends of the semiconductor wire, which are associated with quasi-Majoranas and false negatives. The presence of long-range inhomogeneities (smooth potential variations) can make it more difficult to observe the gap-closing/reopening features, thus leading to false negatives. Interestingly, smooth potential variations are also the regime in which one would expect quasi-Majorana modes. Here the interplay between the two effects is discussed.

[00143] A typical scenario where quasi-Majorana modes appear is when a system is tuned close-to but outside of the topological phase. For concreteness, consider an example where at a fixed magnetic field the chemical potential μ is smaller than the critical chemical potential μ_C required to enter the topological phase. A smooth potential variation can be interpreted as a spatially varying chemical potential $\mu(x) = \mu_0 V(x)$, where $V(x)$ is the potential. In the above scenario, it is possible for a potential dip close to the (here right) end of the semiconductor wire, as shown in FIG. 15, to locally tune the system into the topological regime $\mu(x) > \mu_C$, which leads to a local pair of Majorana modes. The latter manifest in the local conductance at the right end at much lower fields as the topological phase transition in the bulk of the semiconductor wire (which can be read off via the local conductance at the other (left) end where no smooth potential variation is present).

[00144] FIG. 15 shows the effect of a smooth potential at the right end of the semiconductor wire in a 1D model. Left: Spatial dependence of the potential (lower panel) and position of the superconducting shell implemented via self-energy (orange, upper panel) of the semiconductor wire. Right: Conductance matrix including the antisymmetric part of the non-local conductance. Note that there is no gap-reopening feature in the non-local conductance. The only feature of the phase transition is the onset of weak Majorana oscillations.

[00145] Specifically, in the example in FIG. 15, the phase transition at fixed chemical potential is at $B_C \approx 2.7$ T. The ZBPs due to quasi-Majorana modes appearing around $B \approx 1$

T would correctly be labeled as non-topological in method 56 since there is no gap closing and reopening feature in the non-local conductance. However, even at the topological phase transition there is no gap-closing/reopening feature visible. The reason is that the part of the system under the smooth potential at the right side already went through the phase transition and is therefore gapped when B crosses B_C. This suppresses the signal of the bulk modes at the phase transition since they couple only evanescently to the right lead. Note that in this particular model the topological gap is 100 μeV and thus larger than we would expect in realistic systems. For a smaller gap, the non-local signal becomes larger thus increasing the strength of the gap-closing/reopening feature. Nevertheless, since the signal of the finite-size oscillations will also become stronger, it can remain difficult to observe the gap-closing/reopening.

[00146] In conclusion, while quasi-Majorana modes at the end of the semiconductor wire do not lead to false positive features in the non-local conductance, the presence of quasi-Majorana modes increases the chance of false negatives once the system is tuned into the topological phase.

[00147] A second example addresses smooth potentials in the center of the semiconductor wire, associated with false positives. Here we discuss the only example identified that can have ZBPs at both ends of the semiconductor wire and a non-trivial feature in the non-local conductance that could be interpreted as a gap closing (and potentially a reopening), while the bulk of the system is non-topological.

[00148] The setup is depicted in FIG. 16. The bulk of the semiconductor wire is tuned to be non-topological while a smooth potential bump in the center of the semiconductor wire reaches the topological regime of the potential. One can therefore think of a pair of Majorana zero modes nucleating in the center of the semiconductor wire. While the center region is chosen too small for well-separated Majorana modes, the smoothness of the potential could lead to close-by but weakly-coupled quasi Majorana modes in the center of the semiconductor wire.

[00149] Due to finite-size effects, the corresponding zero modes can be probed as correlated ZBPs in the conductance at each end, as shown in FIG. 16. Moreover, since the low-energy modes at the center overlap with both sides they also contribute to the non-local conductance, which could be misinterpreted as a gap closing.

[00150] FIG. 16 shows the effect of smooth potential at the center of the semiconductor wire in a 1D model. Left: Spatial dependence of the potential (lower panel) and position of the superconducting shell implemented via self-energy (orange, upper panel) of the

semiconductor wire. Right: Conductance matrix including the antisymmetric part of the non-local conductance. Note that due to finite-size effects the quasi-Majorana modes nucleated in the center regions are visible as correlated ZBPs and also contribute to the non-local conductance.

[00151] FIG. 17 illustrates data analysis over field/plunger parameter space of the gap method for a 1D model with a potential bump in the center of the semiconductor wire. Left: Detected ZBPs. Right: Gap determined from the data. In this case, the ZBP finder detects two overlapping regions: one centered around plunger = 0 (bulk topological region) and one centered around plunger = 0.0025 (center bump topological). It is unclear whether this case represents a false positive (outside of the bulk topological region) because there is a small topological region in the center, and finite-size effects are significant. In fact, finite-size effects lead to features in the gap-closing of each of the regions (center and bulk) in the estimated gap extracted from the data.

[00152] This problematic example illustrates the value of continued development of the data analysis used in the methods herein. Note that the ZBP clustering algorithm has identified both regions (center and bulk) as a single region. This example illustrates how non-topological regions adjacent to topological regions may be comparatively difficult to separate and may require further refinement in data analysis.

[00153] A third example relates to non-topological ZBPs due to strong disorder. Represented here is an example of a one-dimensional model with strong disorder. To illustrate, FIG. 18 shows data analysis over field/plunger parameter space of a strongly disordered 1D model. Left: points of correlated ZBPs (red) Right: extracted gap at each point in parameter space. While ZBPs are present, the data in FIG. 18 indicates that the regions of correlated ZBPs are sparse and largely disconnected. Strongly disordered region can thus be ruled out by the gap method by adding requirements for the size and continuity of the identified regions.

Instrumentation and Additional Methods

[00154] While the features and examples disclosed herein relate to methods for evaluating a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer, such features and examples are also applicable to related instrumentation. FIG. 19 shows aspects of an example instrument 136 configured to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer. Instrument comprises a controller 18B. The controller includes at least one processor 20B and computer memory 22B coupled operatively to the processor. The

computer memory is configured to hold instructions 24B that cause the processor to enact the various measurement and analysis methods described herein. To that end, the processor may be coupled operatively to RF admittance-measurement device 138 and to a sub-RF conductance-measurement device 140. The RF admittance-measurement device may include features as illustrated in FIG. 7; the sub-RF conductance-measurement device may include features as illustrated in FIG. 11. In the illustrated example, instrument 136 includes an interface 142 that couples the processor to the measurement devices and also provides control signals to the electrostatic gates of device 48 and to magnet 144.

[00155] The features and examples disclosed herein relate equally to methods for building a topological quantum computer. FIG. 20 shows aspects of an example method 146 for building a topological quantum computer.

[00156] Fabricated at 148 of method 146 is a semiconductor-superconductor heterojunction having at least three terminals configured to support electronic admittance testing. At 62 RF junction admittance of the semiconductor-superconductor heterojunction is measured to obtain mapping data. At 64, by analysis of the mapping data, one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction is found. At 66 a sub-RF conductance of the semiconductor-superconductor heterojunction is measured in each of the one or more regions of the parameter space, to obtain refinement data. At 68, by analysis of the refinement data, a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction are found for at least one of the one or more regions of the parameter space. At 150 the semiconductor-superconductor heterojunction is incorporated into a qubit register of the topological quantum computer, provided that the found boundary and topological gap are within respective, predefined ranges. In operation of the topological quantum computer built in this manner, one or more values characterizing the boundary in the parameter space may be used as tuning parameters for addressing the semiconductor-superconductor heterojunction in the qubit register.

[00157] For additional context, the following references are provided.

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[00162] MITEQ AFS4-00100800-14-10P-4.

Conclusion

[00163] In conclusion, one aspect of this disclosure is directed to method to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer. The method comprises: measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data; finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction; measuring a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; and finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space.

[00164] In some implementations, the analysis of the mapping data includes density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction. In some implementations, the method further comprises validating a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage. In some implementations, the analysis of the refinement data includes verifying gap closure at the boundary of each of the one or more regions of the parameter space. In some implementations, the semiconductor-superconductor

heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, the method further comprising meta-analysis of zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction. In some implementations, measuring the sub-RF conductance includes enacting local and non-local conductance measurement suitable for extracting an energy gap of the semiconductor-superconductor heterojunction. In some implementations, the semiconductor-superconductor heterojunction comprises a semiconductor wire and at least three terminals supporting admittance and conductance measurement at opposite ends of the semiconductor wire. In some implementations, the semiconductor-superconductor heterojunction comprises a plurality of electrostatic control terminals.

[00165] Another aspect of this disclosure is directed to an instrument configured to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer. The instrument comprises: a controller having a processor and computer memory coupled operatively to the processor, the controller being configured to: measure a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data; find by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction; measure a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; and find by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space.

[00166] In some implementations, the controller is configured to analyze the mapping data using density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction. In some implementations, the controller is further configured to validate a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage. In some implementations, the controller is configured to analyze the refinement data by verifying gap closure at the boundary of each of the one or more regions of the parameter space. In some implementations, the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, wherein the controller is configured to meta-analyze zero-bias peak data across the series to compute a

probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction. In some implementations, the instrument is coupled operatively to an RF admittance-measurement device and to a sub-RF conductance-measurement device.

[00167] Another aspect of this disclosure is directed to a method for building a topological quantum computer. The method comprises: fabricating a semiconductor-superconductor heterojunction having at least three terminals configured to support electronic admittance testing; measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data; finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction; measuring a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space; and incorporating the semiconductor-superconductor heterojunction in a qubit register of the topological quantum computer provided that the found boundary and topological gap are within respective, predefined ranges.

[00168] In some implementations, the analysis of the mapping data includes density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction. In some implementations, the method further comprises validating a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage. In some implementations, the analysis of the refinement data includes verifying gap closure at the boundary of each of the one or more regions of the parameter space. In some implementations, the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, the method further comprising meta-analysis of zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction. In some implementations, one or more values characterizing the boundary in the parameter space are used as tuning parameters for addressing the semiconductor-superconductor heterojunction in the qubit register.

[00169] Another aspect of this disclosure is directed to a two-stage approach to the

extraction of the topological phase. Significantly, this includes separation by stages whereupon a mapping phase allows for extensive search of the parameter space while still producing false positives, and a refinement stage allows for weeding out false positives slowly scanning the regions of interest from the mapping phase. Another aspect of this disclosure is directed to using density-based clustering algorithms on the two-sided ZBP data to extract predicted topological regions. Significantly, this includes clustering algorithms used for this purpose. It is believed to be the first systematic approach for finding promising regions. Another aspect of this disclosure is directed to mapping between the RF and DC conductance for the purpose of the fast conductance extraction in the RF measurement. Significantly, this includes usage of the mapping to bypass DC conductance measurement and still extract the same data but much faster due to the faster RF technique. Another aspect of this disclosure is directed to classification of bias traces using peak finding or machine learning. Significantly, this includes machine learning of topological traces and statistical characterization of how good peak finding is. Another aspect of this disclosure is directed to extraction of the gap from non-local conductance traces, specifically using bias traces together with experimental noise or filtering and smoothening of bias/field scans. Significantly, this includes the automatic gap extraction. Another aspect of this disclosure is directed to improvement of the accuracy of previous methods by checking for gap closing at the boundary of the suspect topological region. Significantly, this includes application of the extraction of the gap from the data to classify the regions into topological/trivial ones. Another aspect of this disclosure is directed to meta-analysis of the ZBP data to extract the probability of finding topological regions across many devices of the same preparation. This can be used in order to characterize the growth/fabrication method via a topological phase diagram. Another aspect of this disclosure is directed to using any of the above to tune up a qubit of a topological quantum computer.

[00170] It will be understood that the configurations and/or approaches described herein are exemplary in nature, and that these specific embodiments or examples are not to be considered in a limiting sense, because numerous variations are possible. The specific routines or methods described herein may represent one or more of any number of processing strategies. As such, various acts illustrated and/or described may be performed in the sequence illustrated and/or described, in other sequences, in parallel, or omitted. Likewise, the order of the above-described processes may be changed.

[00171] The subject matter of the present disclosure includes all novel and non-obvious combinations and sub-combinations of the various processes, systems and configurations,

and other features, functions, acts, and/or properties disclosed herein, as well as any and all equivalents thereof.

The invention claimed is :

1. A method to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer, the method comprising:

measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data;

finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction;

measuring a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; and

finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space.

2. The method of claim 1 wherein the analysis of the mapping data includes density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction.

3. The method of claim 1 further comprising validating a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage.

4. The method of claim 1 wherein the analysis of the refinement data includes verifying gap closure at the boundary of each of the one or more regions of the parameter space.

5. The method of claim 1 wherein the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, the method further comprising meta-analysis of zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction.

6. The method of claim 1 wherein measuring the sub-RF conductance includes enacting local and non-local conductance measurement suitable for extracting an energy gap of the

semiconductor-superconductor heterojunction.

7. The method of claim 1 wherein the semiconductor-superconductor heterojunction comprises a semiconductor wire and at least three terminals supporting admittance and conductance measurement at opposite ends of the semiconductor wire.

8. The method of claim 1 wherein the semiconductor-superconductor heterojunction comprises a plurality of electrostatic control terminals.

9. An instrument configured to evaluate a semiconductor-superconductor heterojunction for use in a qubit register of a topological quantum computer, the instrument comprising:

a controller having a processor and computer memory coupled operatively to the processor,

the controller being configured to:

measure a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data;

find by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor-superconductor heterojunction;

measure a sub-RF conductance including a non-local conductance of the semiconductor-superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data; and

find by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space.

10. The instrument of claim 9 wherein the controller is configured to analyze the mapping data using density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction.

11. The instrument of claim 9 wherein the controller is further configured to validate a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZBP to variations in cutter-gate voltage.

12. The instrument of claim 9 wherein the controller is configured to analyze the refinement data by verifying gap closure at the boundary of each of the one or more regions of the parameter space.

13. The instrument of claim 9 wherein the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunctions, wherein the controller is configured to meta-analyze zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction.

14. The instrument of claim 9 wherein the instrument is coupled operatively to an RF admittance-measurement device and to a sub-RF conductance-measurement device.

15. A method for building a topological quantum computer, the method comprising : fabricating a semiconductor-superconductor heterojunction having at least three terminals configured to support electronic admittance testing ;

measuring a radio-frequency (RF) junction admittance of the semiconductor-superconductor heterojunction to obtain mapping data;

finding by analysis of the mapping data one or more regions of a parameter space consistent with an unbroken topological phase of the semiconductor superconductor heterojunction;

measuring a sub-RF conductance including a non-local conductance of the semiconductor -superconductor heterojunction in each of the one or more regions of the parameter space to obtain refinement data;

finding by analysis of the refinement data a boundary of the unbroken topological phase in the parameter space and a topological gap of the semiconductor-superconductor heterojunction for at least one of the one or more regions of the parameter space; and

incorporating the semiconductor-superconductor heterojunction in a qubit register of the topological quantum computer provided that the found boundary and topological gap are within respective predefined ranges.

16. The method of claim 15 wherein the analysis of the mapping data includes density-based clustering on zero-bias peak data from opposite ends of the semiconductor-superconductor heterojunction.

17. The method of claim 15 further comprising validating a zero-bias peak (ZBP) in each of the one or more regions by checking stability of the ZEP to variations in cutter-gate voltage.

18. The method of claim 15 wherein the analysis of the refinement data includes verifying gap closure at the boundary of each of the one or more regions of the parameter space.

19. The method of claim 15 wherein the semiconductor-superconductor heterojunction is one of a series of analogously prepared semiconductor-superconductor heterojunction, the method further comprising meta-analysis of zero-bias peak data across the series to compute a probability of finding a topological region in another analogously prepared semiconductor-superconductor heterojunction.

20. The method of claim 15 wherein one or more values characterizing the boundary in the parameter space are used as tuning parameters for addressing the semiconductor-superconductor heterojunction in the qubit register.