(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 June 2011 (16.06.2011)

PCT

(10) International Publication Number
WO 2011/071966 A2

(51) International Patent Classification:
H01L 21/8247 (2006.01) *H01L 27/115* (2006.01)

(21) International Application Number:
PCT/US2010/059362

(22) International Filing Date:
8 December 2010 (08.12.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/635,005 10 December 2009 (10.12.2009) US

(71) Applicant *(for all designated States except US)*: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 S. Federal Way, Boise, ID 83707-0006 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ZAHURAK, John** [US/US]; 2633 W. Sugarberry Drive, Eagle, ID 83616 (US). **TANG, Sanh, D.** [US/US]; 1273 N. Jullion Avenue, Boise, ID 83704 (US). **SANDHU, Gurtej, S.** [US/US]; 2964 E. Parkriver Drive, Boise, ID 83706 (US).

(74) Agents: **PARKER, Paul, T.** et al.; Perkins Coie LLP, P.O. Box 1247, Seattle, WA 98111-1247 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: CROSS-POINT DIODE ARRAYS AND METHODS OF MANUFACTURING CROSS-POINT DIODE ARRAYS

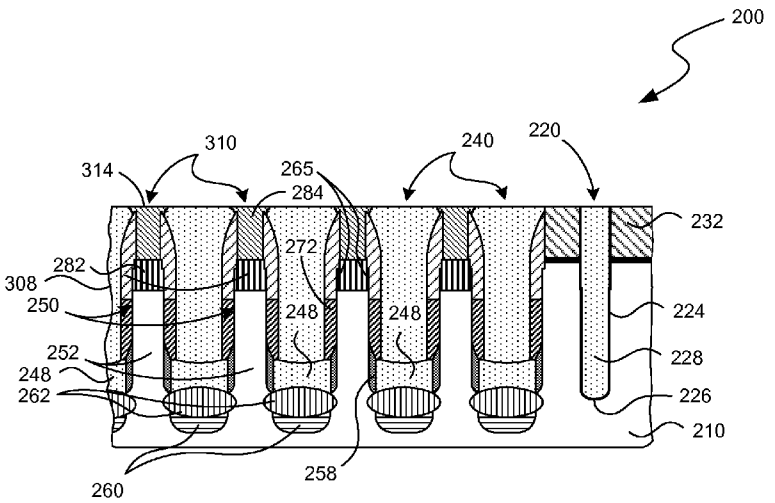


FIG. 22

(57) **Abstract**: Methods of forming an array of memory cells and memory cells that have pillars. Individual pillars can have a semiconductor post formed of a bulk semiconductor material and a sacrificial cap on the semiconductor post. Source regions can be between columns of the pillars, and gate lines extend along a column of pillars and are spaced apart from corresponding source regions. Each gate line surrounds a portion of the semiconductor posts along a column of pillars. The sacrificial cap structure can be selectively removed to thereby form self-aligned openings that expose a top portion of corresponding semiconductor posts. Individual drain contacts formed in the self-aligned openings are electrically connected to corresponding semiconductor posts.

WO 2011/071966 A2