WHAT IS CLAIMED IS:

1. An electronic device including a semiconductor memory, the semiconductor memory comprising:

a plurality of memory cells having a pillar structure extending vertically from a surface of a substrate, each memory cell including a lower portion and an upper portion over the lower portion,

wherein the plurality of memory cells comprise:

a first memory cell including an upper portion that has a first protruding portion protruding laterally beyond a sidewall of a lower portion; and

a second memory cell including an upper portion that has a second protruding portion protruding laterally beyond a sidewall of a lower portion; and

a liner layer disposed along the surface of the substrate and an entire side surface of each of the plurality of memory cells without fully filling a space between the lower portions of the plurality of memory cells, the liner layer having a first portion disposed over the first protruding portion and a second portion disposed over the second protruding portion, the first and second portions of the liner layer directly contacting each other at a contact portion so as to provide spaces located under and over the contact portion,

wherein the upper portion of each memory cell has an inclined sidewall shape,

wherein the semiconductor memory further comprises an insulating material filling the spaces located under and over the contact portion, the insulating material having a lower thermal conductivity than the liner layer, and

wherein a portion of the insulating material located under the contact portion is surrounded by the liner layer.

2. The electronic device according to claim 1, wherein the insulating material comprises a flowable insulating material including SiOC, and

wherein the lower portion of each memory cell includes a variable resistance pattern.

3. The electronic device according to claim 1, wherein a width of the upper portion increases from top to bottom so that a side surface of the upper portion forms an acute angle with the surface of the substrate.

4. The electronic device according to claim 3, wherein the acute angle is in a range of 45° to 89°.

5. The electronic device according to claim 1, wherein the lower portion includes a variable resistance pattern that includes a phase change material.

6. The electronic device according to claim 1, wherein the plurality of memory cells further comprise:

a third memory cell including an upper portion that has a third protruding portion protruding laterally beyond a sidewall of a lower portion, the third memory cell being adjacent to the first memory cell in a diagonal direction with respect to a direction in which the first and second memory cells are arranged,

wherein the liner layer has a third portion disposed over the third protruding portion, the third portion of the liner layer being spaced apart from the first portion of the liner layer.

7. The electronic device according to claim 1, wherein the liner layer has a multi-layered structure including a first liner layer and a second liner layer,

wherein the first liner layer encapsulates the plurality of memory cells, and the second liner layer is disposed over the first liner layer, and

wherein the first liner layer and the second liner layer are alternately stacked along a profile of the plurality of memory cells one or more times.

8. The electronic device according to claim 7, wherein the first liner layer includes a nitride.

9. The electronic device according to claim 7, wherein the second liner layer includes an oxide.

10. An electronic device including a semiconductor memory, the semiconductor memory comprising:

first to fourth memory cells arranged in a matrix form along a first direction and a second direction crossing the first direction, each memory cell having a pillar structure extending vertically from a surface of a substrate and including a lower portion and an upper portion over the lower portion, the upper portion having a protruding portion that protrudes laterally beyond a sidewall of the lower portion; and

a liner layer disposed along the surface of the substrate and an entire side surface of each of the first to fourth memory cells without fully filling spaces between the lower portions of the plurality of memory cells, the liner layer having a first liner portion disposed over a first protruding portion of the first memory cell, a second liner portion disposed over a second protruding portion of the second memory cell, a third liner portion disposed over a third protruding portion of the third memory cell, and a fourth liner portion disposed over a fourth protruding portion of the fourth memory cell,

wherein among the first to fourth memory cells, two neighboring memory cells in the first direction or the second direction contact each other at a contact portion through corresponding liner portions among the first to fourth liner portions so as to provide spaces located under and over the contact portion,

wherein an opening space is defined by the first to fourth liner portions in a plan view and surrounded by the first to fourth memory cells,

wherein the upper portion of each memory cell has an inclined sidewall shape,

wherein the semiconductor memory further comprises an insulating material filling the spaces located under and over the contact portion and the opening space, the insulating material having a lower thermal conductivity than the liner layer, and

wherein a portion of the insulating material located under the contact portion is surrounded by the liner layer.

11. The electronic device according to claim 10, wherein the insulating material comprises a flowable insulating material including SiOC, and wherein the lower portion of each memory cell includes a variable resistance pattern.

12. The electronic device according to claim 10, wherein a width of the upper portion increases from top to bottom so that a side surface of the upper portion forms an acute angle with the surface of the substrate.

13. The electronic device according to claim 12, wherein the acute angle is in a range of 45° to 89°.

14. The electronic device according to claim 10, wherein the lower portion includes a variable resistance pattern that includes a phase change material.

15. The electronic device according to claim 10, wherein the liner layer has a multi-layered structure including a first liner layer and a second liner layer,

wherein the first liner layer encapsulates the first to fourth memory cells, and the second liner layer is disposed over the first liner layer, and

wherein the first liner layer and the second liner layer are alternately stacked along a profile of the first to fourth memory cells one or more times.

16. The electronic device according to claim 15, wherein the first liner layer includes a nitride.

17. The electronic device according to claim 15, wherein the second liner layer includes an oxide.