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(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **JACOBSON, Quinn** [US/US]; 598 Sunnymount Ave, Sunnyvale, California 94087 (US). **WANG, Hong** [US/US]; 2200 Mission College Blvd, Santa Clara, California 95052 (US). **SHEN, John** [US/US]; 2303 Quail Bluff Place, San Jose, California 95121 (US). **CHINYA, Gautham** [IN/US]; 125, SE 49th Ct., Hillsboro, Oregon 97123 (US). **HAMMERLUND, Per** [SE/US]; 2601 NE 2nd Drive, Hillsboro, Oregon 97124 (US). **ZOU, Xiang** [CN/US]; 92 SW Horton Way, Beaverton, Oregon 97006 (US). **BIGBEE, Bryant** [US/US]; 10886 East Palomino Road, Scottsdale, Arizona 85259 (US). **KAUSHKI, Shivnandan** [IN/US]; 14116 NW Harbor LN, Portland, Oregon 97229 (US).

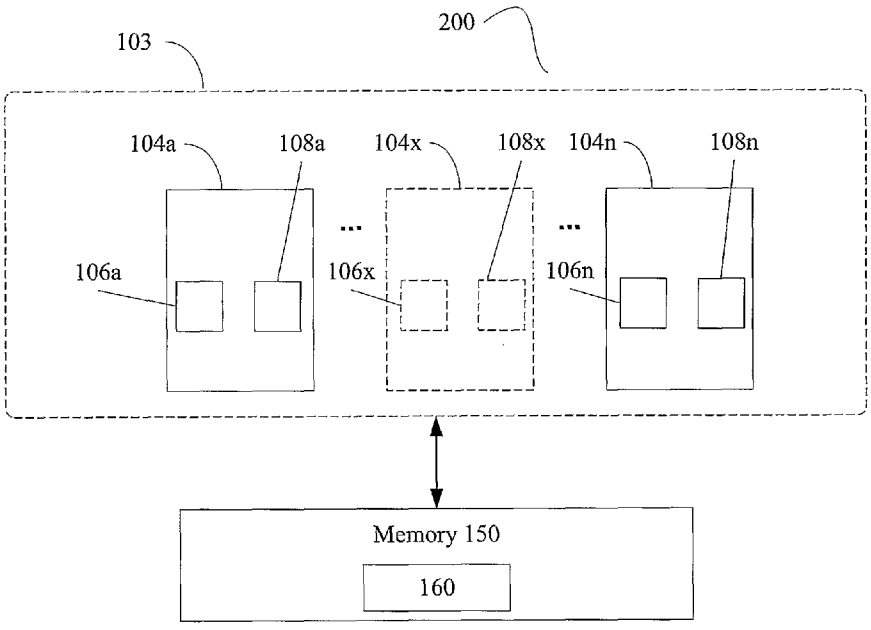
(74) Agents: **VINCENT, Lester J.** et al.; BLAKELY SOKOLOFF TAYLOR & ZAFMAN, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 (US).

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(54) Title: PRIMITIVES TO ENHANCE THREAD-LEVEL SPECULATION



(57) Abstract: A processor may include an address monitor table and an atomic update table to support speculative threading. The processor may also include one or more registers to maintain state associated with execution of speculative threads. The processor may support one or more of the following primitives: an instruction to write to a register of the state, an instruction to trigger the committing of buffered memory updates, an instruction to read the a status register of the state, and/or an instruction to clear one of the state bits associated with trap/exception/interrupt handling. Other embodiments are also described and claimed.

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