

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN AND RELATING TO ELECTRONICALLY CONTROLLED SHUTTERS FOR PHOTOGRAPHIC CAMERAS

(71) We, AGFA-GEVAERT AKTIEN-
GESELLSCHAFT, a body corporate organised
according to the laws of the Federal
Republic of Germany, of Leverkusen,
5 Federal Republic of Germany, do hereby
declare the invention for which we pray
that a patent may be granted to us, and
the method by which it is to be performed,
to be particularly described in and by the
10 following statement:—

The invention relates to an electronically
controlled shutter for a photographic
camera.

A photographic camera adapted for
15 operation with an electronically controlled
shutter will include a shutter opening mem-
ber which is subject to the action of a retard
mechanism during its operation and which
opens the shutter, and a shutter closing
20 member which can be released after the
appropriate delay to provide the required
exposure time. The photographic camera
may also include a photo-sensitive device
which is arranged to receive light from the
25 region of the object to be photographed,
and to provide a signal which controls the
exposure time according to the diaphragm
aperture. It may be advantageous to use
more than one photo-sensitive device, each
30 photo-sensitive device then being restricted
to a particular range of light intensities to
provide good performance over a wide
range of conditions. It will be appreciated
that when more than one photo-sensitive
35 device is used, care must be taken to ensure
that there are no discontinuities in the
overall light intensity — exposure time
relationship, and that the changeover from
one photo-sensitive device to the other must
40 be effected precisely.

In a photographic camera having two
photo-sensitive devices the arrangement may
be such that one photo-sensitive device is
used at higher ambient light levels where
45 the diaphragm aperture is less than maxi-

mum, and the other photo-sensitive device
is used at lower ambient light levels where
the diaphragm aperture is at its maximum.

It is an object of the present invention
to provide for a photographic camera, an 50
electronic shutter control system employing
two photo-sensitive devices.

According to the invention, an electronic
shutter control system comprises,

- (i) first and second photo-resistors having 55
differing characteristics,
- (ii) a timing network arranged to control
exposure time,
- (iii) a resistor network arranged as part of
an impedance bridge, 60
- (iv) a switching network arranged to con-
nect the photo-resistors in circuit with
the resistor network and the timing
network, respectively,
- (v) a bistable flip-flop having data input 65
terminals, a clock input terminal, a
presetting input terminal and output
terminals, and arranged to accept data
from its data input terminals only in
the presence of a pulse at its clock 70
input terminal, the output terminals of
the bistable flip-flop being connected
to the switching network to permit the
control of the connection in circuit of
one of the photo-resistors at a time, 75
- (vi) a clock pulse generator arranged to
provide one clock pulse when triggered,
having an input terminal connected to
the switching network and which is
arranged to be triggered when the 80
switching network is operated to con-
nect the photo-resistors to the timing
network, and an output terminal con-
nected to the clock input terminal of
the bistable flip flop, 85
- (vii) a comparator having input terminals
connected to the resistor network, and
an output terminal,
- (viii) a delay circuit connected between the
output terminal of the comparator and 90

the data input terminals of the bistable flip-flop and arranged to provide a time delay which exceeds the duration of the clock pulse, and (ix) a set pulse generator arranged to provide a voltage step when energised and having an output terminal connected to the presetting input terminal of the bistable flip-flop, the switching network and the timing of the pulse generator being such that, on energisation of the control system, the set pulse generator presets the bistable flip-flop to select the first photo-resistor for connection in circuit, operation of the switching network to connect the photo-resistors to the resistor network is effective to provide data to the bistable flip-flop for the selection of one of the photo-resistors for operation, and operation of the switching network to connect the photo-resistors to the timing network effects connection to the photo-resistor selected according to the state of the bistable flip-flop and initiates exposure timing.

In a preferred embodiment, the bistable circuit is a clocked RS master-slave flip-flop, the presetting input terminal being the PRESET input to the flip-flop, the data input terminals being the respective R and S input terminals of the flip-flop.

A differential amplifier may be used as the comparator, and the resistor network may function as the biasing components for the differential amplifier in addition to being part of the impedance bridge. The resistor network may consist of two resistors connected in series across the voltage supply terminals of the differential amplifier with the inverting input terminal of the amplifier connected to the junction of the resistors, and a third resistor connected to the lower voltage supply terminal and to the non-inverting input terminal of the amplifier. The third resistor may be a variable resistor. The first and second photo-resistors may be connected in series with respective first and second switches, and the series combination of the first photo-resistor and the first switch arranged in parallel with the series combination of the second photo-resistor and the second switch, the parallel arrangement being connected on one side of the upper voltage supply terminal, and on the other side, to a third switch through which the parallel arrangement is connectable to the non-inverting terminal of the differential amplifiers.

The timing network may include a capacitor and a threshold detector connected to the capacitor and arranged to trigger at some set voltage input level, triggering resulting in a rapid change of the voltage output level of the threshold detector. The capacitor may be connected in parallel with

the third switch, and a fourth switch may be connected from the non-inverting terminal of the differential amplifier to the lower voltage supply terminal.

Preferably, a variable resistor is included in series with the second photo-transistor to permit adjustment of the resistance-light intensity characteristic for the second photo-resistor in order to provide means for obtaining a smooth transition from the first to the second photo-resistor and vice-versa.

In a preferred embodiment, the delay circuit includes an inverter, and the data input terminals of the bistable flip-flop are connected to the inverter output terminal and the inverter input terminal, respectively. Light-emitting diodes may be included in the input and output circuits of the inverter as indicators of the relative polarities of the bistable circuit inputs.

The bistable flip-flop may be provided with a stabilised supply voltage in order to isolate it from the remainder of the circuit and thereby to avoid false triggering. The stabilised supply voltage is preferably derived from the supply for the remainder of the circuit by means of a stabilizing diode and a smoothing capacitor.

An electronic shutter control system in accordance with the invention will now be described by way of example only and with reference to the accompanying drawing, which illustrates a preferred form of the invention.

Referring now to the Figure, there is shown a battery 1 which may be connected to the circuit by means of a switch 2. The switch 2 could be arranged for closure when the shutter cocking mechanism is operated. Shown also is a shutter control magnet 4 which does not form part of the invention.

In this Figure is shown a first photo-resistor 5 having a characteristic constant of 0.5 to be used at higher levels of light intensity where the diaphragm aperture is less than maximum, which permits alteration of both the diaphragm aperture and the exposure time for optimum results. A second photo-resistor 8, having a characteristic constant 1 is to be used at lower levels of light intensity where the diaphragm aperture has reached the maximum value and only the exposure time may be altered to give optimum results. The photo-resistor 8 has in series with it a variable resistor 9 which may be adjusted to give a smooth transition at the changeover of the photo-resistors. Associated with the photo-resistor 5 is a PNP transistor 6 which becomes conductive when its base potential voltage is low and non-conductive when its base voltage is high, the emitter of the transistor being connected to the positive terminal of the battery 1 and the collector electrode to the photo-resistor 5. A similar

transistor 7 is similarly connected to the photo-resistor 8. The series combination of the transistor 6 and the photo-resistor 5 is arranged in parallel with the series combination of the transistor 7, the photo-resistor 8 and the variable resistor 9, and in series with this parallel arrangement are a capacitor 10 and a variable resistor 11. Connected across the capacitor 10 is an NPN transistor 12 and across the variable resistor 11 is an NPN transistor 13. Therefore the transistor 12, when conductive, short-circuits the capacitor 10, and the transistor 13 when conductive, short-circuits the variable resistor 11.

The base terminal of the transistor 12 is connected to the junction of two resistors 15 and 16. The terminal of the resistor 16 which is remote from the resistor 15 is connected to the negative terminal of the power supply line for the circuit and the terminal of the resistor 15 which is remote from the resistor 16 is connected to the positive terminal of the power supply line for the circuit by way of a single pole single throw switch 17 and a diode 19. The junction of the two resistors 15 and 16 is connected also to the base terminal of an NPN transistor 14 and the triggering input terminal of a clock pulse generator 41. The emitter terminal of the NPN transistor 14 is connected to the negative terminal of the power supply line and the collector terminal of the said transistor is connected to the positive terminal of the power supply line through a resistor 42. The collector terminal of the NPN transistor 14 is connected also to the base terminal of the NPN transistor 13 which has its collector terminal connected to the junction of the capacitor 10 and the variable resistor 11.

The base terminal of the NPN transistor 14 is connected to the positive voltage supply line by way of the resistor 15 when the switch 17 is closed, and the said base terminal is connected only to the negative voltage supply line by way of the resistor 16 when the switch 17 is open. Therefore the transistor 14 is switched on by the closure of the switch 17, and switched off when the switch is open. Because the base terminal of the transistor 12 is connected to the base terminal of the transistor 14 and the base terminal of the transistor 13 is connected to the collector terminal of the transistor 14, the transistor 12 is switched on when the transistor 14 is switched on, and switched off when the transistor 14 is switched off. In addition, the transistor 13 is always held in the state opposite that of the transistor 12. Furthermore, the clock pulse generator 41 is triggered on when the transistor 14 is switched on by the operation of the switch 17.

When the transistor 12 is conductive and

the transistor 13 is non-conductive the capacitor 10 is short-circuited, and the photo-resistors 5 and 8 with their series components, transistors 6 and 7 and the resistors 9 form one arm of an impedance bridge, of which a resistor 38, a resistor 39 and the resistor 11 form the other arms. A selected one of the photo-resistors 5 and 8 may be switched operationally into the impedance bridge by making one of the transistors 6 and 7 conductive.

An RS flip-flop 20 performs the function of making one of the transistors 6 and 7 conductive, to select one of the photo-resistors 5 and 8 for operation, by causing the appropriate transistor to switch on. The flip-flop outputs are designated Q and $\bar{Q}$, these being logical complements of each

other, as is well known. Because $\bar{Q}$ is the inverse of Q , it follows that only one of the transistors 6 and 7 can be conductive at any time and they can never both be non-conductive. The flip-flop 20 is of the master-slave type, NAND gates 23 and 24 acting as the "master" and NAND gates 25 and 26 acting as the "slave". NAND gates 21 and 22 act as switches to permit data from the inputs S and R to be fed to the "master" under the control of a clock pulse that is to be applied to the input terminal T , and transistors 27 and 28 act as transmission gates to allow data to pass from the "master" to the "slave", again under the control of the clock pulse to be applied to the input terminal T . The flip-flop 20 will therefore respond to input signals on the terminals S and R only when a clock pulse is present at the input terminal

T . The input terminal designated $\bar{R}$ is used to set the flip-flop 20 to a predetermined logical state, this terminal going directly to the "master" section, and to the "slave" section, of the flip-flop 20. Therefore

an input signal on the terminal $\bar{R}$ acts on the flip-flop 20 independently of a clock pulse on the terminal T . Initially the flip-flop 20 is set to a logical state $Q \equiv 1$, $\bar{Q} \equiv 0$ by an input pulse on the terminal $\bar{R}$, this pulse being provided by a set pulse generator 40. The power supply to the flip-flop 20 is provided from the battery 1 via a forward biased diode 19, and the cathode side of the diode 19 is decoupled by means of a capacitor 18. This arrangement acts as a voltage stabiliser and provides some isolation of the flip-flop supply from disturbances appearing on the main supply rail. This reduces the risk of false triggering of the flip-flop 20.

The input terminals S and R to the flip-flop 20 are connected to the collector and base terminals, respectively, of an NPN transistor 31, the collector circuit of which includes a light-emitting diode 32 and a resistor 33 in series, the base terminal of

which is connected to the positive power supply line via a light-emitting diode 34 and a resistor 35 in series, and the emitter of which is connected to the negative voltage supply line. The signal on the input terminal S of the flip-flop 20 is therefore always the inverse of the signal on the input terminal R of the said flip-flop. The transistor 31 and its associated components, the resistors 33 and 35 and the light-emitting diodes 32 and 34 along with a delay stage 36 form a delay circuit which is energised by a differential amplifier 37. The inverting input terminal of the differential amplifier 37 is connected to the junction of the resistors 38 and 39, the resistors 38 and 39 being connected between the inverting input terminal of the differential amplifier 37 and the positive and negative voltage supply lines, respectively, which are also the voltage supply lines to the amplifier 37. Therefore the resistors 38 and 39 establish a reference voltage level for the inverting input terminal of the differential amplifier 37. The non-inverting input terminal of the differential amplifier 37 is connected to the junction of the variable resistor 11, the capacitor 10 and the transistors 12 and 13. The differential amplifier 37 functions as a comparator providing either a constant high or low output level according to the relative levels of the voltages present at its input terminals. When the transistor 12 is conductive it short-circuits the capacitor 10 thereby making the impedance bridge circuit operative, when illumination of the light-emitting diode 32 indicates that the output voltage of the differential amplifier 37 is at the high voltage level and illumination of the light-emitting diode 34 indicates that the output voltage of the amplifier 37 is at the low voltage level. Therefore the light-emitting diodes 32 and 34 are indicators of the relative resistance of the photo-resistor which is operational.

The set pulse generator 40 operates when power is applied to the supply rails on closure of the switch 2 to generate a voltage step which is applied to the input terminal R of the flip-flop 20 to set the flip-flop output Q to a logic 1 and the output $\bar{Q}$ to a logic 0, thereby holding transistor 6 on, and holding transistor 7 off. The voltage step consists of an initial period at the low logic level followed by an abrupt change to the high logic level.

The transistor 12 and the transistors 13 and 14 act with the clock pulse generator 41, under the control of the switch 17, which may be actuated by the shutter release button of a camera. When the switch 17 is closed, the potential at the junction of the resistors 15 and 16 is positive which makes transistors 12 and 14 conductive,

and transistor 13 non-conductive, since transistor 14 acts as an inverter. This represents the impedance bridge arrangement where the capacitor 10 is short-circuited by the transistor 12. When the switch 17 is opened, the potential at the junction of the resistors 15 and 16 drops to zero, the transistors 12 and 14 become non-conductive and the transistor 13 becomes conductive. A negative-going step is applied to the clock pulse generator 41 which then produces a positive pulse with its leading edge corresponding to the negative-going step. The capacitor 10 is no longer short-circuited and is charged from the positive rail through whichever photo-resistor is operational, the voltage rise across the capacitor being monitored by a threshold detector 3 which triggers at some predetermined level to close the camera shutter by energising a relay 4. When the switch 17 is opened, the output of the amplifier 37 may change, but this is prevented from reaching the flip-flop inputs S and R by the delay stage 36 until the pulse from the clock pulse generator 41 has disappeared. The delay provided by the delay stage 36 exceeds the duration of the clock pulse from the clock pulse generator 41.

The electronic shutter control system of Figure 1 operates as follows:—

If the ambient lighting level is such that a short exposure time is appropriate, the required diaphragm aperture is smaller than the maximum possible aperture. After closure of the switch 2 the supply lines are energised by the battery 1 and the set pulse generator 40 operates. Operation of the set pulse generator 40 consists of maintaining a low level output voltage for some predetermined time and then providing an output voltage step which is recognisable by the bistable flip-flop 20 as a change from a low logic level to a high logic level. The output signal waveform from the set pulse generator 40 is illustrated within the area representing the set pulse generator 40. The output signal from the set pulse generator

40 energises the R or PRESET input terminal of the bistable flip-flop 20 in which, as is generally known in the electronics art, a low level voltage on the PRESET terminal overrides all other input signals and holds the Q output at logic 1. The change of the flip-flop 20 from a low to a high logic level is effective to free the flip-flop for operation in response to signals arriving at its other input terminals but leaves the flip-flop in the Q=logic 1 state. As is the normal arrangement for flip-flops and several other digital circuits, there is

also a $\bar{Q}$ output which is always the logical inverse of Q. Therefore the flip-flop 20 is set initially to the state Q=logic 1 and $\bar{Q}$ =logic 0, and the transistor 6 is switched

on while the transistor 7 is switched off. During this time the switch 17 is closed, so that the transistor 12 is conductive and the transistor 13 is non-conductive, and the resistors 38 and 39 along with the variable resistor 11 and the photo-resistor 5 form an impedance bridge. Because the ambient lighting level is high the resistance of photo-resistor 5 is relatively low and the potential at the non-inverting terminal of the amplifier 37 is positive with respect to the potential at the inverting terminal of the amplifier 37, which gives a positive output from the amplifier 37. This positive output at the base terminal of transistor 31 makes it conductive so that the collector potential is low and the light-emitting diode 32 is illuminated. The input to the terminal S is therefore a logic 0 and the input to the terminal R is a logic 1.

These input signals are ignored by the flip-flop 20 in the absence of a clock pulse on its clock input terminal T. The clock pulse provided by the clock pulse generator 41 is illustrated within the area representing the clock pulse generator 41. The illustrated clock pulse is of the form generally required for operation of a master-slave flip-flop, the event P1 corresponding to isolation of the slave section of the flip-flop from its master section, the event P2 corresponding to the entry of data from the S and R inputs to the master section, the event P3 corresponding to the isolation of the master section from the S and R inputs, and the event P4 corresponding to the transfer of data from the master section to the slave section and its appearance at the output terminals Q and $\bar{Q}$. The construction and method of operation of the flip-flop are well known in the digital electronics art.

With the switch 17 closed, therefore, data representing the result of assessment of the lighting level as determined by the impedance bridge with the photo-resistor 5 as the light-sensitive measuring element is maintained at the S and R input terminals of the flip-flop 20, but the flip-flop 20 maintains the Q=logic 1 state in the absence of a clock pulse from the clock pulse generator 41. The system can remain in this state indefinitely. This would correspond to the state of a camera with its shutter cocked and in which the camera continues to monitor the ambient lighting level.

Exposure is initiated by the opening of the switch 17, which causes an abrupt change in the voltage level at the junction of the resistors 16 and 17, and results in the generation of a clock pulse by the clock pulse generator 41. The application of the clock pulse to the T input terminal of the flip-flop 20 allows the flip-flop 20 to respond to the data present at its S and R input

terminals, and the flip-flop 20 then provides output signals corresponding to that data which in this case is Q=logic 1, selecting the photo-resistor 5. The flip-flop 20 will ignore any data presented to its S and R input terminals after the disappearance of the clock pulse. The opening of the switch 17 also causes the transistor 12 to switch off and the transistor 13 to switch on, thereby connecting the capacitor 10 to the lower voltage supply line and leaving the capacitor connected to the upper voltage supply line via the photo-resistor 5. The switching on of the transistor 13 has the additional effect of connecting the non-inverting terminal of the amplifier 37 to the lower voltage supply line which may have the effect of changing the amplifier output voltage level which output level is now unrelated to the ambient lighting level. This incorrect data as to lighting level still finds its way to the S and R input terminals of the flip-flop 20, but the delay element 36 is effective to hold this incorrect data back until the clock pulse has disappeared from the T input terminal of the flip-flop 20, and when the incorrect data eventually reaches the flip-flop it is ignored. The capacitor 10 becomes charged by way of the photo-resistor 5, delaying shutter closure until the capacitor voltage reaches the triggering level for the threshold stage 33, when the exposure is terminated.

When the ambient lighting level is low, the situation with the switch 17 closed is the same as for high ambient lighting, but the output from the amplifier 37 will be reversed, and consequently the inputs to the terminals S and R of the flip-flop 20 will be reversed. The light-emitting diode 34 will be alight. When the switch 17 is operated, the flip-flop outputs Q and $\bar{Q}$ will be reversed, and the charging circuit will be formed by the photo-resistor 8, the variable resistor 9 and the capacitor 10. The variable resistor 9 is adjustable to make the composite resistance/light intensity curve for the two photo-resistors 5 and 8, a smooth and continuous curve.

WHAT WE CLAIM IS:—

1. An electronic shutter control system, comprising
 - (i) first and second photo-resistors having differing characteristics,
 - (ii) a timing network arranged to control exposure time,
 - (iii) a resistor network arranged as part of an impedance bridge,
 - (iv) a switching network arranged to connect the photo-resistors in circuit with the resistor network and the timing network, respectively,
 - (v) a bistable flip-flop having data input terminals, a clock input terminal, a presetting input terminal, and output



(14)

on while the transistor 7 is switched off. During this time the switch 17 is closed, so that the transistor 12 is conductive and the transistor 13 is non-conductive, and the resistors 38 and 39 along with the variable resistor 11 and the photo-resistor 5 form an impedance bridge. Because the ambient lighting level is high the resistance of photo-resistor 5 is relatively low and the potential at the non-inverting terminal of the amplifier 37 is positive with respect to the potential at the inverting terminal of the amplifier 37, which gives a positive output from the base terminal of transistor 31 makes it conductive so that the collector potential is low and the light-emitting diode 32 is illuminated. The input to the terminal S is therefore a logic 0 and the input to the terminal R is a logic 1.

These input signals are ignored by the flip-flop 20 in the absence of a clock pulse on its clock input terminal T. The clock pulse provided by the clock pulse generator 41 is illustrated within the area representing the clock pulse generator 41. The illustrated clock pulse is of the form generally required for operation of a master-slave flip-flop, the event P1 corresponding to isolation of the slave section of the flip-flop from its master section, the event P2 corresponding to the entry of data from the S and R inputs to the master section, the event P3 corresponding to the isolation of the master section from the S and R inputs, and the event P4 corresponding to the transfer of data from the master section to the slave section and its appearance at the

output terminals Q and $\bar{Q}$. The construction and method of operation of the flip-flop are well known in the digital electronics art.

With the switch 17 closed, therefore, data representing the result of assessment of the lighting level as determined by the impedance bridge with the photo-resistor 5 as the light-sensitive measuring element is maintained at the S and R input terminals of the flip-flop 20, but the flip-flop 20 maintains the Q=logic 1 state in the absence of a clock pulse from the clock pulse generator 41. The system can remain in this state indefinitely. This would correspond to the state of a camera with its shutter cocked and in which the camera continues to monitor the ambient lighting level.

Exposure is initiated by the opening of the switch 17, which causes an abrupt change in the voltage level at the junction of the resistors 16 and 17, and results in the generation of a clock pulse by the clock pulse generator 41. The application of the clock pulse to the T input terminal of the flip-flop 20 allows the flip-flop 20 to respond to the data present at its S and R input

terminals, and the flip-flop 20 then provides output signals corresponding to that data which in this case is Q=logic 1, selecting the photo-resistor 5. The flip-flop 20 will ignore any data presented to its S and R input terminals after the disappearance of the clock pulse. The opening of the switch 17 also causes the transistor 12 to switch off and the transistor 13 to switch on, thereby connecting the capacitor 10 to the lower voltage supply line and leaving the capacitor connected to the upper voltage supply line via the photo-resistor 5. The switching on of the transistor 13 has the additional effect of connecting the non-inverting terminal of the amplifier 37 to the lower voltage supply line which may have the effect of changing the amplifier output voltage level which output level is now unrelated to the ambient lighting level. This incorrect data as to lighting level still finds its way to the S and R input terminals of the flip-flop 20, but the delay element 36 is effective to hold this incorrect data back until the clock pulse has disappeared from the T input terminal of the flip-flop 20, and when the incorrect data eventually reaches the flip-flop it is ignored. The capacitor 10 becomes charged by way of the photo-resistor 5, delaying shutter closure until the capacitor voltage reaches the triggering level for the threshold stage 33, when the exposure is terminated.

When the ambient lighting level is low, the situation with the switch 17 closed is the same as for high ambient lighting, but the output from the amplifier 37 will be reversed, and consequently the inputs to the terminals S and R of the flip-flop 20 will be reversed. The light-emitting diode 34 will be alight. When the switch 17 is

operated, the flip-flop outputs Q and $\bar{Q}$ will be reversed, and the charging circuit will be formed by the photo-resistor 8, the variable resistor 9 and the capacitor 10. The variable resistor 9 is adjustable to make the composite resistance/light intensity curve for the two photo-resistors 5 and 8, a smooth and continuous curve.

WHAT WE CLAIM IS:—

1. An electronic shutter control system, comprising
 - (i) first and second photo-resistors having differing characteristics,
 - (ii) a timing network arranged to control exposure time,
 - (iii) a resistor network arranged as part of an impedance bridge,
 - (iv) a switching network arranged to connect the photo-resistors in circuit with the resistor network and the timing network, respectively,
 - (v) a bistable flip-flop having data input terminals, a clock input terminal, a presetting input terminal, and output

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- terminals, and arranged to accept data from its data input terminals only in the presence of a pulse at its clock input terminal, the output terminals of the bistable flip-flop being connected to the switching network to permit the control of the connection in circuit of one of the photo-resistors at a time,
- (vi) a clock pulse generator arranged to provide one clock pulse when triggered, having an input terminal connected to the switching network which is arranged to be triggered when the switching network is operated to connect the photo-resistors to the timing network, and an output terminal connected to the clock input terminal of the bistable flip-flop.
- (vii) a comparator having input terminals connected to the resistor network, and an output terminal,
- (viii) a delay circuit connected between the output terminal of the comparator and the data input terminals of the bistable flip-flop, and arranged to provide a time delay which exceeds the duration of the clock pulse, and
- (ix) a set pulse generator arranged to provide a voltage step when energised and having an output terminal connected to the presetting input terminal of the bistable flip-flop,
- the switching network and the timing of the pulse generators being such that, on energisation of the control system, the set pulse generator presets the bistable flip-flop to select the first photo-resistor for connection in circuit, operation of the switching network to connect the photo-resistors to the resistor network is effective to provide data to the bistable flip-flop for the selection of one of the photo-resistors for operation, and operation of the switching network to connect the photo-resistors to the timing network effects connection to the photo-resistor selected according to the state of the bistable flip-flop and initiates exposure timing.
2. An electronic shutter control system as claimed in claim 1, wherein the bistable flip-flop is a clocked RS master-slave flip-flop, the presetting input terminal being the

PRESET input terminal of the flip-flop and the data input terminals the respective R and S input terminals of the flip-flop.

3. An electronic shutter control system as claimed in claim 1 or claim 2, wherein the comparator is a differential amplifier having one input terminal connected to the junction of two resistors of the resistor network, the other terminal of the differential amplifier being connectable to the first and second photo-resistors by way of a switch, the said first and second photo-resistors being connected to respective first and second switches by means of which one or other of the photo-resistors is connectable into circuit.

4. An electronic shutter control system as claimed in any one of claims 1 to 3, wherein the timing network includes a capacitor, and a threshold detector connected to the capacitor, the capacitor being connected to the said first and second photo-resistors.

5. An electronic shutter control system as claimed in claim 3, wherein the switches are transistors.

6. An electronic shutter control system as claimed in any one of claims 1 to 5, wherein a variable resistor is included in series with the second photo-resistor.

7. An electronic shutter control system as claimed in any one of claims 1 to 6, wherein the delay circuit includes a delay stage and an inverter, and means arranged to indicate the relative polarities of the output and input signals of the inverter.

8. An electronic shutter control system as claimed in any one of claims 1 to 7, wherein a voltage stabilising circuit is included in the power supply arrangement for the bistable flip-flop.

9. An electronic shutter control system substantially as herein described with reference to and as illustrated by the accompanying drawing.

10. A camera including an electronic shutter control system as claimed in any one of the preceding claims.

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