

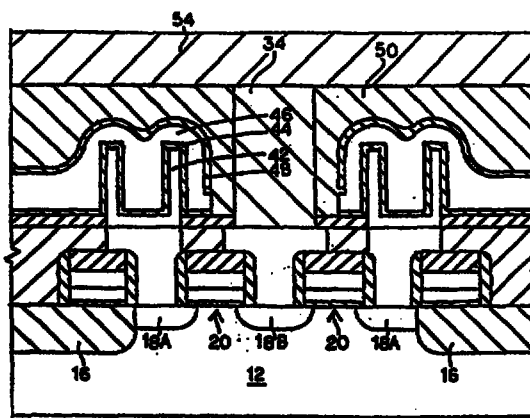
PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/92, 21/3205, 21/8242	A1	(11) International Publication Number: WO 96/14663 (43) International Publication Date: 17 May 1996 (17.05.96)
(21) International Application Number: PCT/US95/14568 (22) International Filing Date: 7 November 1995 (07.11.95) (30) Priority Data: 08/336,426 8 November 1994 (08.11.94) US (71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 S. Federal Way, Boise, ID 83706-9632 (US) (72) Inventors: FIGURA, Thomas, A.; 4313 Douglas Street, Boise, ID 83706 (US). PRALL, Kirk, D.; 2548 S. Harmony, Boise, ID 83706 (US). (74) Agent: FLETCHER, Michael, G.; P.O. Box 4433, Houston, TX 77210 (US).		(81) Designated States: AL, AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

SG 9701953-3

(54) Title: METHOD OF FORMING BIT LINE CONTACTS IN STACKED CAPACITOR DRAMS //**(57) Abstract**

A method of forming a contact area between two vertical structures. A first layer of material conforming to and extending between vertical sidewalls is covered with a mask layer. The mask layer is patterned and etched to remove the horizontal region of the mask layer between the vertical sidewalls, thereby exposing the first layer of material at the desired location of the contact area, while retaining at least a portion of the vertical regions of the mask layer. Using the remaining vertical regions of the mask layer as an etch mask, the exposed portions of the first layer are then etched away to form the contact area. Another aspect of the invention provides a method of making a DRAM that utilizes a capacitor insulating layer over the capacitor second conductor (or cell poly) to self-align the bit line contact to the capacitor second conductor. In accordance with this aspect of the invention, a capacitor is formed over a semiconductor wafer. The capacitor includes a first conductor, a dielectric layer on the first conductor and a second conductor on the dielectric layer. A capacitor insulating layer is formed on the second conductor. The capacitor insulating layer is patterned and etched to expose portions of the second conductor at the desired location of the bit line contact. Then, using the capacitor insulating layer as a hard mask, the exposed portions of the second conductor are etched away in the area in which the bit line contact will subsequently be formed.