



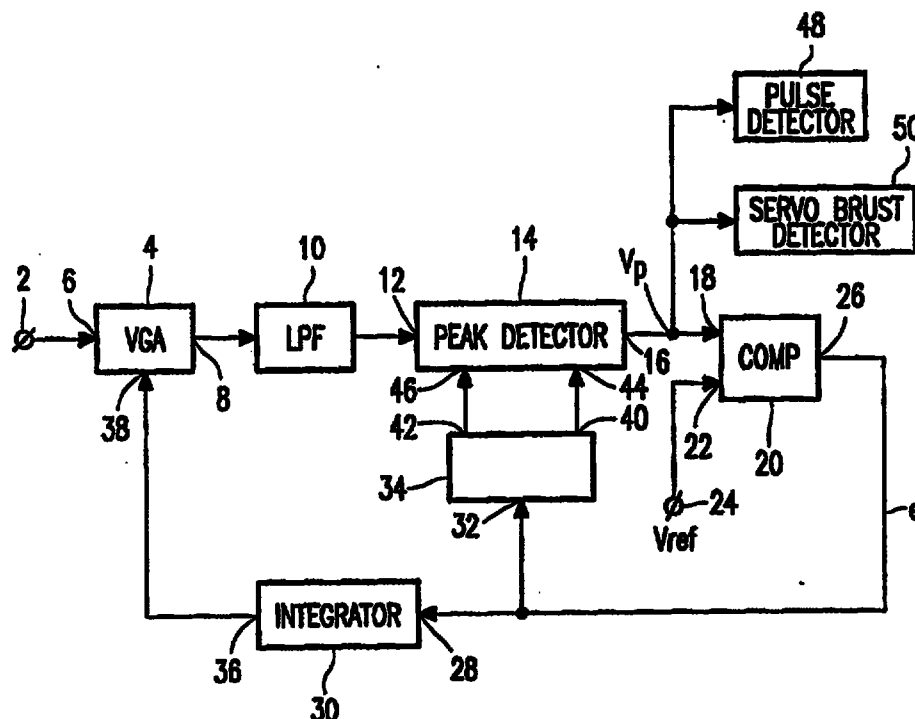
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(21) International Application Number: PCT/IB98/00675 (22) International Filing Date: 7 May 1998 (07.05.98) (30) Priority Data: 97201659.6 3 June 1997 (03.06.97) EP (34) Countries for which the regional or international application was filed: NL et al. (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). (71) Applicant (for SE only): PHILIPS AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE). (72) Inventors: VOORMAN, Johannes, Otto; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). RAMALHO, Joao, Nuno, Vila, Lobos; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). (74) Agent: VAN DER KRUK, Willem, L.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).		(81) Designated States: CN, JP, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published Without international search report and to be republished upon receipt of that report.

(54) Title: AUTOMATIC GAIN CONTROL CIRCUIT, E.G. FOR USE IN A HARD DISK DRIVE

(57) Abstract

An automatic gain control circuit is disclosed for amplifying an input signal so that it has a specific correspondence with a reference value (V_{ref}). The circuit comprises an input terminal (2) for receiving the input signal, a variable gain amplifier unit (4) for amplifying said input signal in response to a gain control signal. A peak detector unit (14) is provided for detecting peaks in said amplified input signal. The peak detector unit (14) has an attack time constant (T_a) and a decay time constant (T_d), so as to supply a peak detector output signal (V_p) which is representative of the amplitude of the peaks in said amplified input signal. Further, a comparator unit (20) is provided for comparing the peak detector output signal (V_p) with said reference value (V_{ref}) so as to derive an error signal (e) therefrom. An integrator unit (30) is further present for integrating the error signal (e) so as to obtain said gain control signal. The peak detector circuit comprises means for controlling said decay time constant in response to said error signal, said means for controlling said decay time constant being adapted to decrease said decay time constant for increasing error signals, in a situation when the peak detector output signal (V_p) is larger than said reference value (V_{ref}). Further, the following relationship is maintained between the attack time constant T_a and the decay time constant T_d of the peak detector means: $T_d = c \cdot T_a^p$, where c is a positive constant and p is a constant larger than 1. p is preferably equal to 2 and for c holds $20 \leq c \leq 200$.



The peak detector circuit comprises means for controlling said decay time constant in response to said error signal, said means for controlling said decay time constant being adapted to decrease said decay time constant for increasing error signals, in a situation when the peak detector output signal (V_p) is larger than said reference value (V_{ref}). Further, the following relationship is maintained between the attack time constant T_a and the decay time constant T_d of the peak detector means: $T_d = c \cdot T_a^p$, where c is a positive constant and p is a constant larger than 1. p is preferably equal to 2 and for c holds $20 \leq c \leq 200$.