

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
18 December 2008 (18.12.2008)

PCT

(10) International Publication Number
WO 2008/151429 A1

(51) International Patent Classification:

H01L 29/66 (2006.01) *H01L 21/336* (2006.01)
G11C 11/40 (2006.01) *H01L 29/78* (2006.01)
G11C 17/16 (2006.01) *H03K 19/177* (2006.01)

(21) International Application Number:

PCT/CA2008/001122

(22) International Filing Date: 11 June 2008 (11.06.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

11/762,552 13 June 2007 (13.06.2007) US

(71) Applicant (for all designated States except US): **SIDENSE CORP.** [CA/CA]; 84 Hines Road, Suite 260, Ottawa, Ontario K2K 3G3 (CA).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KURJANOWICZ, Wlodek** [CA/CA]; 56 Sherring Crescent, Ottawa, Ontario K2K 2T1 (CA). **SMITH, Steven** [CA/CA]; 38 Pine Ridge Road, Wakefield, Québec J0X 3G0 (CA).

(74) Agents: **HUNG, Shin** et al.; Borden Ladner Gervais LLP, World Exchange Plaza, 100 Queen Street, Suite 1100, Ottawa, Ontario K1P 1J9 (CA).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL,

[Continued on next page]

(54) Title: ANTI-FUSE MEMORY CELL

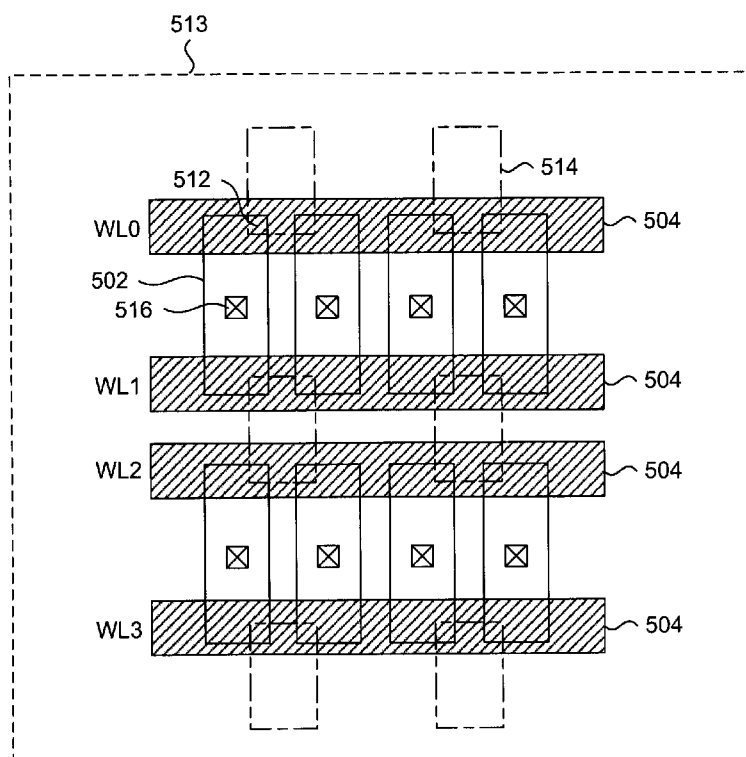


Figure 10

(57) Abstract: An anti-fuse memory cell having a variable thickness gate oxide. The variable thickness gate oxide has a thick gate oxide portion and a thin gate oxide portion, where the thin gate oxide portion has at least one dimension less than a minimum feature size of a process technology. The thin gate oxide can be rectangular in shape or triangular in shape. The anti-fuse transistor can be used in a two-transistor memory cell having an access transistor with a gate oxide substantially identical in thickness to the thick gate oxide of the variable thickness gate oxide of the anti-fuse transistor.



NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG,
CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a
patent (Rule 4.17(ii))*

Published:

- *with international search report*