

Claims

What is claimed is:

1. A package assembly comprising:
a substrate comprising a plurality of build-up layers;
electrical routing features disposed on an outer surface of the substrate;
a primary logic die embedded in the plurality of build-up layers;
a second die or capacitor embedded in the plurality of build-up layers; and
an electrical path defined in the plurality of build-up layers to route electrical power or a ground signal between the second die or capacitor and the electrical routing features, the electrical path bypassing the primary logic die.
2. The package assembly of claim 1, wherein the second die or capacitor comprises a secondary logic die or a memory die.
3. The package assembly of claim 2, wherein the primary logic die includes one or more vias between a first surface of the primary logic die and a second, opposing surface of the primary logic die.
4. The package assembly of claim 3, wherein the electrical path is a first electrical path, the package assembly further comprising a second electrical path defined in the plurality of build-up layers from an active surface of the secondary logic die or memory die to the one or more vias, to route input/output ("I/O") signals between the primary logic die and the secondary logic die or memory die.
5. The package assembly of any one of claims 1-4, wherein the second die or capacitor comprises a power management die.
6. The package assembly of any one of claims 1-4, wherein the primary logic die and the second die or capacitor are approximately coplanar.

7. The package assembly of any one of claims 1-4, wherein the primary logic die is embedded in the plurality of build-up layers in-between the second die or capacitor and the electrical routing features.

8. The package assembly of claim 7, wherein the electrical path includes a conductive layer between two of the plurality of build-up layers to route the electrical power or ground signal that passes between the second die and the electrical routing features away from the primary logic die.

9. The package assembly of claim 8, wherein the conductive layer is a first conductive layer, and the electrical path includes a second conductive layer between two of the plurality of build-up layers, wherein the second conductive layer is parallel to the first conductive layer and closer to the electrical routing features than the first conductive layer.

10. The package assembly of any one of claims 1-4, wherein the first die and the second die or capacitor are fully embedded within the plurality of build-up layers.

11. The package assembly of any one of claims 1-4, wherein the outer surface of the substrate is a first outer surface, the first die is fully embedded within the plurality of build-up layers, and a surface of the second die is flush with a second outer surface of the substrate opposite the first outer surface.

12. The package assembly of any one of claims 1-4, wherein the electrical routing features comprise solder interconnect structures.

13. A method of forming a package assembly, comprising:
forming a substrate comprising a plurality of build-up layers;
forming electrical routing features on an outer surface of the substrate;
embedding a primary logic die in the plurality of build-up layers;
embedding a second die or capacitor in the plurality of build-up layers; and

forming an electrical path in the plurality of build-up layers to route electrical power or a ground signal between the second die or capacitor and the electrical routing features, the electrical path bypassing the primary logic die.

14. The method of claim 13, wherein the second die or capacitor comprises a secondary logic die or a memory die.

15. The method of claim 14, further comprising forming one or more vias between a first surface of the primary logic die and a second, opposing surface of the primary logic die.

16. The method of claim 15, wherein the electrical path is a first electrical path, the method further comprising forming a second electrical path in the plurality of build-up layers from an active surface of the secondary logic die or memory die to the one or more vias, to route input/output ("I/O") signals between the primary logic die and the secondary logic die or memory die.

17. The method of any one of claims 13-16, wherein embedding the primary logic die further comprises embedding the primary logic die in the plurality of build-up layers to be approximately coplanar with the second die or capacitor.

18. The method of any one of claims 13-16, wherein embedding the primary logic die further comprises embedding the primary logic die in the plurality of build-up layers in-between the second die or capacitor and the electrical routing features.

19. The method of any one of claims 13-16, further comprising forming, as part of the electrical path, a conductive layer between two of the plurality of build-up layers to route the electrical power or ground signal that passes between the second die and the electrical routing features away from the primary logic die.

20. The method of any one of claims 13-16, wherein the conductive layer is a first conductive layer, and the method further comprises forming, as part of the electrical path, a second conductive layer between two of the plurality of build-up layers, wherein the second conductive layer is parallel to the first conductive layer and closer to the electrical routing features than the first conductive layer.

21. The method of any one of claims 13-16, wherein embedding the first primary logic die comprises fully embedding the primary logic die within the plurality of build-up layers, and wherein embedding the second die or capacitor comprises fully embedding the second die or capacitor within the plurality of build-up layers.

22. The method of any one of claims 13-16, wherein the outer surface of the substrate is a first outer surface, and embedding the second die or capacitor comprises embedding the second die or capacitor in the plurality of build-up layers so that a surface of the second die or capacitor is flush with a second outer surface of the substrate opposite the first outer surface.

23. The method of any one of claims 13-16, wherein forming the electrical routing features comprises forming solder interconnect structures.

24. A system, comprising:
a printed circuit board (PCB); and
a package assembly coupled with the PCB via electrical routing features disposed on an outer surface of the package assembly, the package assembly comprising
a substrate comprising a plurality of build-up layers;
a primary logic die embedded in the plurality of build-up layers;
a second die or capacitor embedded in the plurality of build-up layers; and
an electrical path defined in the plurality of build-up layers to route electrical power or a ground signal between the second die or capacitor and the electrical routing features, the electrical path bypassing the primary logic die.

25. The system of claim 24, further comprising a touch screen display.

Claims

What is claimed is:

1. A package assembly comprising:
a substrate comprising a plurality of build-up layers;
electrical routing features disposed on an outer surface of the substrate;
a primary logic die embedded in the plurality of build-up layers;
a second die or capacitor embedded in the plurality of build-up layers; and
an electrical path defined in the plurality of build-up layers to route electrical power or a ground signal between the second die or capacitor and the electrical routing features, the electrical path bypassing the primary logic die,
wherein the primary logic die includes one or more vias between a first surface of the primary logic die and a second, opposing surface of the primary logic die.
2. The package assembly of claim 1, wherein the second die or capacitor comprises a secondary logic die or a memory die.
3. The package assembly of claim 2, wherein the electrical path is a first electrical path, the package assembly further comprising a second electrical path defined in the plurality of build-up layers from an active surface of the secondary logic die or memory die to the one or more vias, to route input/output ("I/O") signals between the primary logic die and the secondary logic die or memory die.
4. The package assembly of any one of claims 1-3, wherein the second die or capacitor comprises a power management die.
5. The package assembly of any one of claims 1-3, wherein the primary logic die and the second die or capacitor are approximately coplanar.
6. The package assembly of any one of claims 1-3, wherein the primary logic die is embedded in the plurality of build-up layers in-between the second die or capacitor and the electrical routing features.

7. The package assembly of claim 6, wherein the electrical path includes a conductive layer between two of the plurality of build-up layers to route the electrical power or ground signal that passes between the second die and the electrical routing features away from the primary logic die.

8. The package assembly of claim 7, wherein the conductive layer is a first conductive layer, and the electrical path includes a second conductive layer between two of the plurality of build-up layers, wherein the second conductive layer is parallel to the first conductive layer and closer to the electrical routing features than the first conductive layer.

9. The package assembly of any one of claims 1-3, wherein the first die and the second die or capacitor are fully embedded within the plurality of build-up layers.

10. The package assembly of any one of claims 1-3, wherein the outer surface of the substrate is a first outer surface, the first die is fully embedded within the plurality of build-up layers, and a surface of the second die is flush with a second outer surface of the substrate opposite the first outer surface.

11. A method, comprising:
forming a substrate comprising a plurality of build-up layers;
forming electrical routing features on an outer surface of the substrate;
embedding a primary logic die in the plurality of build-up layers;
embedding a second die or capacitor in the plurality of build-up layers; and
forming an electrical path in the plurality of build-up layers to route electrical power or a ground signal between the second die or capacitor and the electrical routing features, the electrical path bypassing the primary logic die,
wherein the primary logic die includes one or more vias between a first surface of the primary logic die and a second, opposing surface of the primary logic die.

12. The method of claim 11, wherein the second die or capacitor comprises a secondary logic die or a memory die.

13. A system, comprising:
a printed circuit board (PCB); and
a package assembly coupled with the PCB via electrical routing features disposed on an outer surface of the package assembly, the package assembly comprising
a substrate comprising a plurality of build-up layers;
a primary logic die embedded in the plurality of build-up layers;
a second die or capacitor embedded in the plurality of build-up layers; and
an electrical path defined in the plurality of build-up layers to route electrical power or a ground signal between the second die or capacitor and the electrical routing features, the electrical path bypassing the primary logic die,
wherein the primary logic die includes one or more vias between a first surface of the primary logic die and a second, opposing surface of the primary logic die.

14. The system of claim 13, wherein:
the second die or capacitor comprises a secondary logic die or a memory die;
the electrical path is a first electrical path; and
a second electrical path is defined in the plurality of build-up layers from an active surface of the secondary logic die or memory die to the one or more vias, to route input/output ("I/O") signals between the primary logic die and the secondary logic die or memory die.