CLAIMS

1. A device comprising:

a plurality of groups of gallium nitride (GaN) epitaxial layers, a combined thickness of the plurality of groups of GaN epitaxial layers greater than ten microns;

mesas etched within at least some groups of the plurality of groups of GaN epitaxial layers;

internal interconnects formed within the mesas;

electrodes formed on at least one of the internal interconnects or the GaN epitaxial layers, the electrodes configuring each group of GaN epitaxial layers of the plurality of groups of GaN epitaxial layers into a GaN device of a plurality of GaN devices; and

external interconnects formed over at least some of the electrodes for connecting the plurality of GaN devices into an integrated circuit.

2. The device of claim 1 wherein the plurality of groups of GaN epitaxial layers is formed on an engineered substrate with a diameter of at least 150 millimeters.

3. The device of claim 2 wherein a coefficient of thermal expansion (CTE) of the plurality of groups of GaN epitaxial layers matches a CTE of the engineered substrate.

4. The device of claim 1 wherein:

a first group of GaN epitaxial layers of the plurality of groups of GaN epitaxial layers forms a transistor;

a second group of GaN epitaxial layers of the plurality of groups of GaN epitaxial layers located on top of the first group of GaN epitaxial layers forms a light emitting diode (LED); and

the external interconnects connect an electrode formed on the transistor with an electrode formed on the LED.

5. The device of claim 4 wherein:

the second group of GaN epitaxial layers forms multiple quantum wells (MQWs) that emit light; and

the first group of GaN epitaxial layers is substantially transparent to the light emitted from the MQWs.

6. A gallium nitride (GaN) integrated circuit comprising:

a first set of GaN layers;

a first set of mesas, interconnects, and first electrodes for configuring the first set of GaN layers into a first GaN device;

a second set of GaN layers formed on top of the first set of GaN layers;

a second set of mesas, interconnects, and second electrodes for configuring the second set of GaN layers into a second GaN device; and

a third set of interconnects formed on at least an electrode of the first electrodes and at least an electrode of the second electrodes for connecting the first GaN device to the second GaN device.

7. The GaN integrated circuit of claim 6 wherein the first set of GaN layers and the second set of GaN layers have a combined thickness of at least 10 microns.

8. The GaN integrated circuit of claim 6 wherein the first set of GaN layers and the second set of GaN layers are formed on an engineered substrate with a diameter of at least six inches and have a coefficient of thermal expansion (CTE) substantially matching a CTE of the engineered substrate.

9. The GaN integrated circuit of claim 8 further comprising a buffer layer is disposed between the GaN integrated circuit and the engineered substrate.

10. The GaN integrated circuit of claim 8 wherein the engineered substrate may include one or more outer engineered layers encapsulating a polycrystalline layer.

11. The GaN integrated circuit of claim 10 wherein the polycrystalline layer comprises an aluminum nitride (AlN) substrate and the one or more outer engineered layers comprise at least one of oxide, nitride, or polysilicon.

12. The GaN integrated circuit of claim 6 further comprising an electrically isolating wide bandgap layer disposed between the first set of GaN layers and the second set of GaN layers.