ABSTRACT

A three-dimensional (3D) semiconductor device may include a stack structure and a vertical channel structure. The stack structure may include a first insulation pattern, a conductive pattern and a second insulation pattern. The conductive pattern may be arranged on the first insulation pattern. The second insulation pattern may be configured to physically contact an upper surface of the conductive pattern. The second insulation pattern may have a property different from a property of the first insulation pattern. The vertical channel structure may be formed through the stack structure.

FIG. 1B