Description

Title of Invention: DIRECT-POWER-CONVERTER CONTROL DEVICE

Technical Field

[0001] This invention relates to a technique for controlling a direct power converter including a converter, an inverter, and a power buffer circuit that are mutually connected through a DC link.

Background Art

[0002] Generally, full-wave rectifying circuits are used as converters to obtain a DC voltage from a single-phase AC voltage input from a single-phase AC power source. However, the output of the full-wave rectifying circuits contains power ripple having a frequency twice that of the single-phase AC voltage. Thus, reduction in this power ripple requires a power buffer circuit that buffers the power between an output of the full-wave rectifying circuit and a load.

[0003] Non-Patent Documents 1 to 3 and Patent Documents 1 to 4 listed below disclose a technique for connecting a capacitor to a DC link through a switching element. In the proposed technique, the capacitor (hereinafter also referred to as a "buffer capacitor"), which functions as a voltage source, drives a load together with a power supply voltage to compensate for the power ripple as well as reduce the electrostatic capacity required for the buffer capacitor.

[0004] Particularly, Non-Patent Documents 1 to 2 and Patent Documents 1 to 4 also propose a technique that achieves a function of a boost chopper using a reactor and a switch to boost a voltage across a buffer capacitor (hereinafter referred to as a "both-end voltage").

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Summary of Invention

Problems to be Solved by the Invention

[0009] However, use of film capacitors as the buffer capacitors is undesirable in consideration of downsizing the buffer capacitors. Here, options for capacitors to be used as the buffer capacitors include ceramic capacitors and electrolytic capacitors.

[0010] The tolerance range of the electrostatic capacity of the electrolytic capacitors largely varies from ±20% to ±30%. Moreover, the electrostatic capacity tends to decrease according to degradation of the capacitors. When the voltage of the buffer capacitor varies according to change in the electrostatic capacity, an error increases in estimating an input current. This induces variations in the both-end voltage. When the variations are prominent, a direct power converter may not be operable.

[0011] Thus, embodiments of the present invention seek to provide a technique for making variations in the both-end voltage less prominent even when the electrostatic capacity of the buffer capacitor varies.

Means to Solve the Problems

[0012] The direct-power-converter control device according to this invention is a control device (10) that controls a direct power converter.

[0013] The direct power converter includes: a DC link (7) including a first power supply line (LH) and a second power supply line; a converter (3) that receives a single-phase AC voltage (Vin), and outputs ripple power (Pin) to the DC link in which the first power supply line is higher in potential than the second power supply line; a power buffer circuit (4) provided between the first and second power supply lines, the power buffer circuit buffering power by buffered power (Pbuf) obtained by multiplying an AC component ($\hat{Pin}$) of the ripple power (Pin) by a distribution factor (k); and an inverter (5)

that converts a DC voltage (Vdc) between the first and second power supply lines into an AC voltage.

[0014] The power buffer circuit includes: a discharge circuit (4a) including a capacitor (C4) and a switch (Sc, D42) connected in series with the capacitor between the first and second power supply lines, the switch being closer to the first power supply line relative to the capacitor; and a charge circuit (4b) that charges the capacitor.

[0015] The control device includes an inverter controller (101), a discharge controller (102), and a charge controller (103).

[0016] The inverter controller outputs an inverter control signal (SSup, SSvp, SSwp, SSun, SSvn, SSwn) for controlling an operation of the inverter on the basis of a rectifying duty (drec), a discharge duty (dc), and a command value (Vu*, Vv*, Vw*) of a voltage to be output by the inverter, the rectifying duty being a duty at which the converter is brought into conduction with the DC link, the discharge duty being a duty at which the switch is conducting.

[0017] The discharge controller outputs a discharge switch signal (SSc) for bringing the switch into conduction on the basis of the discharge duty.

[0018] The charge controller includes: an amplitude determining unit (103a) that determines an amplitude (Im) of an input current (Iin) to be input to the converter by performing at least proportional-integral control on a deviation (ΔVc) between a voltage across the capacitor and an average voltage command value (Vc*) that is a command value of an average of the voltage across the capacitor; a charge command generating unit (103b) that determines a charge command (iL*) on a current (il) flowing through the charge circuit by multiplying by the amplitude a function (F1 (ωt), F2 (ωt), F3 (ωt)) of a phase (ωt) of the single-phase AC voltage, the function being determined according to the discharge duty, the rectifying duty, and the distribution factor; and a charging operation

controller (103c) that controls a charging operation of the charge circuit on the basis of the charge command.

[0019] For example, the discharge duty and the rectifying duty are set so that the power buffer circuit (4) receives power from the DC link during a period during which a cosine value (cos (2ωt)) is negative and provides power to the DC link during a period during which the cosine value is positive, the cosine value being a cosine of a value twice the phase (ωt).

[0020] Alternatively, power (Pl) received by the power buffer circuit (4) from the DC link (7) and power (Pc) provided by the power buffer circuit (4) to the DC link (7) are set to vary at a frequency twice a frequency of the single-phase AC voltage (Vin) as a fundamental frequency.

[0021] Preferably, the function is determined with the input current (Iin) having a sinusoidal waveform.

[0022] Preferably, responsiveness of the charge controller (103) is less than or equal to one tenth of a value twice a frequency of the single-phase AC voltage (Vin).

Effects of the Invention

[0023] Even when an electrostatic capacity of a capacitor (buffer capacitor) included in a discharge circuit of a power buffer circuit varies, variations in both-end voltage of the capacitor are made less prominent.

[0024] The objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0025] FIG. 1 is a block diagram illustrating a structure of a direct power converter according to embodiments;

FIG. 2 is a block diagram exemplifying a structure of a control device according to the embodiments;

FIG. 3 is a block diagram schematically illustrating the balance of power in the direct power converter illustrated in FIG. 1;

FIG. 4 is a diagram illustrating an equivalent circuit of the direct power converter illustrated in FIG. 1;

FIG. 5 is a graph indicating relationships between an average, the maximum value, the minimum value, and fluctuation of a both-end voltage of a buffer capacitor;.

FIG. 6 is a graph indicating behaviors of various quantities in a technique corresponding to a technique of Patent Document 2 when an electrostatic capacity of the buffer capacitor decreases;

FIG. 7 is a graph indicating behaviors of various quantities in the technique corresponding to the technique of Patent Document 2 when the electrostatic capacity of the buffer capacitor increases;

FIG. 8 is a graph indicating behaviors of various quantities in a first embodiment when the electrostatic capacity of the buffer capacitor decreases;

FIG. 9 is a graph indicating behaviors of various quantities in the first embodiment when the electrostatic capacity of the buffer capacitor increases;

FIG. 10 is a graph indicating operations of a direct power converter according to a second embodiment;

FIG. 11 is a graph indicating the operations of the direct power converter according to the second embodiment;

FIG. 12 is a block diagram illustrating an example of a structure for performing control with a DC current;

FIGS. 13 and 14 are graphs indicating operations of a direct power converter according

to a third embodiment;

FIG. 15 is a graph indicating behaviors of various quantities in the third embodiment when the electrostatic capacity of the buffer capacitor decreases;

FIG. 16 is a graph indicating behaviors of various quantities in the third embodiment when the electrostatic capacity of the buffer capacitor increases; and

FIG. 17 is a circuit diagram illustrating a modification of the direct power converter illustrated in FIG. 1.

Description of Embodiments

[0026] A. Analysis of problems with conventional techniques

Before describing embodiments in detail, problems with the conventional techniques will be analyzed to facilitate understanding of the present invention.

[0027] (i) First conventional technique: In Non-Patent Document 2, the minimum value of the both-end voltage is detected and the maximum value of the both-end voltage is used as a voltage command to control the both-end voltage. However, an average of the both-end voltage is high even when a load of an inverter is low because the maximum value of the both-end voltage is used as the voltage command (see, for example, FIG. 7 of Patent Document 2). The high average induces increase in switching loss of a power buffer circuit.

[0028] (ii) Second conventional technique: Apparently, Patent Document 1 suggests a method for obtaining a reactor current command on the basis of the maximum value and the minimum value of a detected both-end voltage to control an average of the both-end voltage. However, since such a control is significantly influenced by the ripple of a voltage output by a full-wave rectifying circuit, the responsiveness of a control system is

inferior (see, for example, FIG. 10 of Patent Document 2).

[0029] (iii) Third conventional technique: In Patent Document 2, a reactor current command is obtained using an average of a both-end voltage as a voltage command to control the both-end voltage. Accordingly, an average voltage is held constant, thus improving the responsiveness (see, for example, FIG. 6 of Patent Document 2).

[0030] However, in the first to third conventional techniques, an input current is estimated not from the both-end voltage themselves but from an average, the maximum value, and the minimum value of the both-end voltage. Thus, variations in electrostatic capacity of a buffer capacitor increase an error of the input current, which may cause variations in operating point of the both-end voltage.

[0031] This is expressed by an equation. According to the various documents above, it is known that the following Equation (1) holds by introducing an amplitude Im of an input current Iin to be input to a full-wave rectifying circuit, an amplitude Vm and an angular velocity ω of a single-phase AC voltage Vin (= Vm·sin(ωt), where t denotes a time) to be rectified by the full-wave rectifying circuit, an electrostatic capacity C of a buffer capacitor, and the maximum value Vcmax and the minimum value Vcmin of a both-end voltage.

[0032]

$$Im = \frac{\omega \cdot C}{Vm}(Vcmax^2 - Vcmin^2) \qquad (1)$$

[0033] Furthermore, the following Equation (2) holds by introducing an average Vavg (= (Vcmax + Vcmin) / 2) of the both-end voltage (see, for example, Patent Document 2).

[0034]

$$Im = \frac{\omega \cdot C}{Vm}\{2 \cdot Vavg \cdot (Vcmax - Vcmin)\} \qquad (2)$$

[0035] Furthermore, a reactor current command il* is determined according to the following Equation (3) so that the input current Iin has a sinusoidal waveform and a power factor is 1 (that is, Iin = Im·sin(ωt)). Since the amplitude Im can be obtained from Equations (1) and (2) as described above, the reactor current command il* depends on the maximum value Vcmax and the minimum value Vcmin of the both-end voltage.

[0036]

$$il^* = Im \cdot |\sin(\omega t)| - \frac{Im}{2 \cdot |\sin(\omega t)|} \qquad (3)$$

[0037] When a buffer capacitor is provided, it is known that the following Equation (4) holds by introducing a power Pout to be output by an inverter 5 and an both-end voltage Vc (see, for example, Non-Patent Document 3).

[0038]

$$Vc = \sqrt{Vavg^2 - \frac{Pout}{\omega \cdot C} \cdot \sin(2\omega t)} \qquad (4)$$

[0039] When the maximum value Vcmax of the both-end voltage Vc is fixed as a command value as according to the first conventional technique, the average Vavg of the both-end voltage Vc also varies according to variations in the power Pout subject to variations in a load. In contrast, when the average Vavg is fixed as a command value as according to the third conventional technique, a fluctuation (Vcmax – Vcmin) of the both-end voltage Vc varies.

[0040] For example, FIG. 5 indicates relationships between the average Vavg, the maximum value Vcmax, the minimum value Vcmin, and the fluctuation (Vcmax – Vcmin) of the both-end voltage Vc when Vm = 230√2 (V), Im = 16√2 (A), Pout = 3680 (W). When the amplitude Im indicated by Equations (1) and (2) is fixed, an operating point of the both-end voltage Vc is determined by the average Vavg, and the maximum

necessary to generate this charge switch signal SSl, it is input to the charging operation controller 103c.

[0082] The charging operation controller 103c functions as, for example, a critical mode modulator that generates the charge switch signal SSl so that the reactor current il flows in the critical mode. In Non-Patent Document 2, the value of the inductance of the reactor L4 is limited on the premise that the reactor current il flows in the discontinuous mode. However, according to the technique proposed by the present application, even when the inductance varies from the limits and influences the both-end voltage Vc, the operation of the amplitude determining unit 103a accommodates the influence of variations.

[0083] With such structures, the technique described in "B. Basic ideas of technique to be proposed" can be embodied.

[0084] D. Outline of operations of power buffer circuit 4

Instantaneous input power Pin to be input to the converter 3 is expressed by the following Equation (5) with an input power factor 1.

[0085]

$$\begin{aligned} Pin &= Vm \cdot Im \cdot \sin^2(\omega t) \\ &= \frac{Vm \cdot Im}{2} - \frac{Vm \cdot Im}{2} \cdot \cos(2\omega t) \end{aligned} \qquad (5)$$

[0086] The instantaneous input power Pin has an AC component $(-1/2)\cdot Vm\cdot Im\cdot\cos(2\omega t)$ (hereinafter may be referred to as an "AC component Pin^") indicated by the second term in the right side of Equation (5). Thus, the instantaneous input power Pin may be hereinafter referred to as ripple power Pin.

[0087] The power converter illustrated in FIG. 1 can be understood as follows.

[0088] The converter 3 receives the single-phase AC voltage Vin, and outputs the ripple power Pin. The power buffer circuit 4 receives receiving power Pl from the DC

link 7, and outputs providing power Pc to the DC link 7. The inverter 5 receives input power Pdc (= Pin + Pc – Pl) obtained by subtracting the receiving power Pl from a sum of the ripple power Pin and the providing power Pc, and outputs the load currents iu, iv, and iw. If the loss of the inverter 5 is disregarded, the input power Pdc is equal to the power Pout (see Equation (4)).

[0089] FIG. 3 is a block diagram schematically illustrating the balance of power in the direct power converter illustrated in FIG. 1. The power subjected to buffering (hereinafter referred to as "buffering power Pbuf") is equal to a power difference (Pc – Pl) obtained by subtracting the receiving power Pl from the providing power Pc. Furthermore, power Prec transferred from the converter 3 to the inverter 5 is equal to (Pin – Pl). Thus, Pdc = Prec + Pc holds.

[0090] A distribution factor k is introduced into the next Equation (6).

[0091]

$$Pdc = \frac{Vm \cdot Im}{2} - (1-k) \cdot \frac{Vm \cdot Im}{2} \cdot \cos(2\omega t) \qquad (6)$$

[0092] In other words, when k = 0, the inverter 5 receives the ripple power Pin as it is in as the input power Pdc from the DC link 7. This means Pbuf = 0 which corresponds to a case where no power is distributed to the power buffer circuit 4. When k=1, Pdc = Pin – $\hat{Pin}$ holds. This corresponds to a case where the power buffer circuit 4 provides and receives to and from the DC link 7 powers of the absolute value $|\hat{Pin}|$ of the AC component $\hat{Pin}$.

[0093] In other words, the distribution factor k indicates a level of the absolute value $|\hat{Pin}|$ of the AC component $\hat{Pin}$ to be distributed to the power buffer circuit 4 as the buffering power Pbuf.

[0094] E. Equivalent circuit of direct power converter and various duties

irec1, ic, and iz are averages in switching periods of the switches Srec, Sc, and Sz, respectively. Thus, the duties drec, dc, and dz can be regarded as current distribution factors of the DC current Idc relative to the currents irec1, ic, and iz, respectively.

[0102] When a diode bridge is used as the converter 3, the converter 3 cannot actively perform a switching operation in the rectifying duty drec. Thus, the inverter 5 and the switch Sc perform a switching operation at the zero duty dz and the discharge duty dc, respectively, thus obtaining the current irec1.

[0103] During a period in which the zero current iz flows, the inverter 5 cannot use a DC voltage in the DC link 7. Thus, the DC voltage in the DC link 7 to be used in supplying power to the inverter 5 is significant in converting power. In other words, the instantaneous DC voltage that is not used by the inverter 5 for power conversion is meaningless even in considering a voltage utilization factor. The DC voltage Vdc significant in converting power can be expressed by Equation (7) below.

[0104]

$$Vdc = Vrec \cdot drec + Vc \cdot dc + 0 \cdot dz \qquad (7)$$

[0105] In contrast, the DC voltage Vdc can be understood as a voltage to be applied to the DC link 7 as an average of the maximum values of the voltage that the inverter 5 can output in a period during which switching of the switches Sc and Sl and the inverter 5 is controlled. This is because the inverter 5 is insulated from one of the DC power lines LL and LH during a period corresponding to the zero duty dz, though the inverter 5 may contribute to the voltage at the DC link 7 at a ratio indicated by the zero duty dz.

[0106] In FIG. 4, the DC voltage Vdc is shown as a voltage across a current source Idc (that supplies the DC current Idc) representing the inverter 5 and a load of the inverter 5.

[0107] Hereinafter, the various modes in which the direct power converter is operated will be specifically described.

[0108] F. First embodiment

The first embodiment will be described in comparison with the operations of the direct power converter introduced by Patent Document 2.

[0109] In the technique disclosed by Patent Document 2, different controls have been alternately performed per quarter period (1/4 period) of the single-phase AC voltage Vin (hereinafter, such a control will be also referred to as "quarter period control" for convenience) to cancel out the AC component $\hat{Pin}$. Specifically, a control where Pl = $\hat{Pin}$ and Pc = 0 and a control where Pl = 0 and Pc = $-\hat{Pin}$ have been alternately performed per quarter period of the single-phase AC voltage Vin. Accordingly, Pdc = Pin + Pc – Pl = Pin – $\hat{Pin}$ = (1/2)·Vm·Im holds during all the periods, and the power ripple has been avoided. This holds when k = 1 in Equation (6).

[0110] In the present application, a period during which the receiving power Pl is received from the DC link 7 (a period during which a cosine value cos (2ωt) that is a cosine of a value twice a phase ωt is negative) is called a receiving period, and a period during which the providing power Pc is provided to the DC link 7 (a period during which the cosine value cos (2ωt) is positive) is called a providing period, similarly as Patent Document 2.

[0111] (f-1) Setting of duty

In Patent Document 2, the discharge duty dc is set by the next Equation (8), and the reactor current command il* is determined by Equation (3) using this discharge duty dc and on the premise that the input current Iin has a sinusoidal waveform. Here, the DC current Idc can be set as a command value.

[0112]

$$dc = \begin{cases} 0 \,(\text{receivingperiod}) \\ \dfrac{Vm \cdot Im}{2 \cdot Vc \cdot Idc} \cdot \cos(2\omega t) \,(\text{providingperiod}) \end{cases} \qquad (8)$$

[0113] Furthermore, the rectifying duty drec is set by the next Equation (9), thus allowing the DC voltage Vdc to have a constant value (for example, Patent Document 1).

[0114]

$$drec = \begin{cases} \dfrac{Im}{2 \cdot Idc \cdot |\sin(\omega t)|} \ (receivingperiod) \\ \dfrac{Im}{Idc} \cdot |\sin(\omega t)| \ (providingperiod) \end{cases} \qquad (9)$$

[0115] In the first embodiment, the duty arithmetic unit 1021 generates the duties dc and drec according to Equations (8) and (9), respectively, using the amplitude Im obtained from the amplitude determining unit 103a as the amplitude Im in Equations (3), (8), and (9). In other words, the duty arithmetic unit 1021 receives the amplitudes Vm and Im, the DC current Idc, and the phase ωt in the first embodiment.

[0116] However, the input power Pdc to be input to the inverter 5 from the DC link 7 is equal to a product of the DC voltage Vdc and the DC current Idc. Since the inverter 5 receives the input power Pdc (= Pin + Pc – Pl) obtained by subtracting the receiving power Pl from a sum of the ripple power Pin and the providing power Pc, Equation (10) below holds.

[0117]

$$Idc = \frac{Pin + Pc - Pl}{Vdc} = \frac{Vm \cdot Im}{2 \cdot Vdc} \qquad (10)$$

[0118] Thus, Equations (8) and (9) may be modified into Equations (11) and (12), respectively. The DC voltage Vdc may be input to the duty arithmetic unit 1021 as a command value, instead of the DC current Idc.

[0119]

$$dc = \begin{cases} 0 \ (receivingperiod) \\ \dfrac{Vdc}{Vc} \cdot \cos(2\omega t) \ (providingperiod) \end{cases} \qquad (11)$$

[0120]

$$drec = \begin{cases} \dfrac{Vdc}{Vm} \cdot \dfrac{1}{|\sin(\omega t)|} \text{ (receivingperiod)} \\ \dfrac{2 \cdot Vdc}{Vm} \cdot |\sin(\omega t)| \text{ (providingperiod)} \end{cases} \quad (12)$$

[0121] (f-2) Reactor current il

In the critical mode, the reactor current il rises from 0 to a peak value during a period ΔT1 during which the switch Sl is conducting, and drops from the peak value to 0 during a period ΔT2 during which the switch Sl is non-conducting. Such periods ΔT1 and ΔT2 are alternately set. When these rise and drop approximate linear change in the time, the reactor current il that is half the peak value flows in average.

[0122] Considering that the rectified voltage Vrec = |Vin| = Vm·|sin(ωt)| is applied to the power buffer circuit 4, the period ΔT1 is expressed by Equation (13) below to which an inductance L of the reactor L4 is introduced.

[0123]

$$\Delta T1 = \frac{2 \cdot il \cdot L}{Vm \cdot |\sin(\omega t)|} \quad (13)$$

[0124] Thus, the period ΔT1 during which the switch Sl is conducting is determined by Equation (14) using the reactor current command il* expressed by Equation (3) as the reactor current il in Equation (13).

[0125]

$$\Delta T1 = \frac{2 \cdot L}{Vm} \cdot Im \cdot \left(1 - \frac{1}{2 \cdot \sin^2(\omega t)}\right) \quad (14)$$

[0126] In Equation (14), the amplitude Im can be obtained from the amplitude determining unit 103a, and the coefficient 2·L/Vm can be regarded as a proportional gain for a voltage control system. Thus, once the charge command iL* to be expressed by

Equations (15) is determined, the period ΔT1 is determined by voltage feedback control.

[0127]

$$iL^* = Im \cdot F1(\omega t)$$

$$F1(\omega t) = 1 - \frac{1}{2 \cdot \sin^2(\omega t)} \qquad (15)$$

[0128] Here, the function F1(ωt) is the same as the function F(ωt) above, and is a function of the phase θ (= ωt) to be used in the first embodiment. As described in "B. Basic ideas of technique to be proposed", the charge command iL* is determined by a product of the amplitude Im and the function F1 (ωt).

[0129] Then, the function F1 (ωt) is determined according to the discharge duty dc determined by Equation (8) or (11), the rectifying duty drec determined by Equation (9) or (12), and the distribution factor k that is equal to 1.

[0130] The charging operation controller 103c operates a counter until reaching the charge command iL*, and converts the counted value into the period ΔT1 of the charge switch signal SSl (during which the switch Sl is conducting). The conversion factor of the counter also functions as a proportional gain for a voltage control system, similarly as the coefficient 2·L/Vm.

[0131] When the period ΔT1 starts to be counted for the charge switch signal SSl is the timing when the switch Sl is turned ON, which is triggered by the voltage Vl decreasing to 0 that is to be applied to the reactor L4. This is because the switch Sl may be switched from OFF to ON in the critical mode when the reactor current il decreases to 0 and because the timing with which the reactor current il decreases to 0 can be regarded as the timing with which the voltage Vl decreases to 0.

[0132] (f-3) Advantages

FIGS. 8 and 9 are graphs each indicating behaviors of various quantities when

rectifying duty drec, and the discharge duty dc are different in value from those used in the first embodiment.

[0137] The discharge duty dc and the rectifying duty drec expressed by Equations (11) and (12) allow the DC voltage Vdc to be constant. This can be understood from the fact that Equation (7) identically holds in consideration of $Vrec = Vm \cdot |\sin(\omega t)|$.

[0138] However, during drec ≤ 1 and a providing period, $|\sin(\omega t)| \leq 1/\sqrt{2}$ holds. Thus, as seen from the rectifying duty during the providing period in the right side of Equation (12), as long as the DC voltage Vdc is maintained constant, the value never exceed $1/\sqrt{2}$ of the amplitude Vm.

[0139] The second embodiment introduces a technique for improving a ratio R of the DC voltage Vdc to the amplitude Vm (hereinafter referred to as a "voltage utilization factor") by adopting the next Equation (16) expressing the DC voltage Vdc, thus indicating a function F2 (ωt) that is a function F (ωt) when the technique is adopted.

[0140]

$$Vdc = \begin{cases} Vm \cdot |\sin(\omega t)| (receivingperiod) \\ Vm \cdot |\cos(\omega t)| (providingperiod) \end{cases} \qquad (16)$$

[0141] The following description will describe, in order, the probability that the voltage utilization factor R may exceed $1/\sqrt{2}$ by setting the DC voltage Vdc through Equation (16), existence of the rectifying duty drec and the discharge duty dc for (though approximately) obtaining the DC voltage Vdc, and the reactor current command il* and the function F2 (ωt) when the DC voltage Vdc is set.

[0142] (g-1) Improvement in voltage utilization factor R

An average Ra of the voltage utilization factors R during a receiving period is obtained from the next Equation (17). Furthermore, since each phase difference between the providing period and the receiving period and between a sinusoidal

waveform and a cosine waveform is π/2, the average Ra during the providing period is equal to that during the receiving period.

[0143]

$$\begin{aligned} Ra &= \frac{1}{Vm}\cdot\frac{1}{\pi/2}\cdot\int_{\pi/4}^{3\pi/4} Vm\cdot\left|\sin(\omega t)\right| d(\omega t) \\ &= \frac{2\sqrt{2}}{\pi} = \frac{4}{\pi}\cdot\frac{1}{\sqrt{2}} \end{aligned} \quad (17)$$

[0144] Thus, during any of the providing period and the receiving period, the voltage utilization factors R have been improved in average to 4/π (>1) times that indicated in the first embodiment.

[0145] (g-2) Setting of duty

According to the second embodiment, drec = 1 and dc = 0 hold during the receiving period. Such rectifying duty drec and discharge duty dc satisfy and can set respective conditions applied thereto, that is, $0 \le drec \le 1$, $0 \le dc \le 1$, and drec + dc + dz = 1.

[0146] Accordingly, a result of the calculation of the right side of Equation (7) is equal to the right side for the receiving period in Equation (16).

[0147] During the providing period, the rectifying duty drec and the discharge duty dc are set by Equation (18) and Equation (19), respectively.

[0148]

$$drec = \sqrt{2}\cdot\left|\sin(\omega t)\right| (providingperiod) \quad (18)$$

[0149]

$$dc = \frac{Vm}{Vc}\cdot\cos(2\omega t) (providingperiod) \quad (19)$$

[0150] Since $0 \le |\sin(\omega t)| \le 1/\sqrt{2}$ holds during the providing period, the rectifying duty drec set by Equation (18) satisfies the condition $0 \le drec \le 1$ applied thereto.

Furthermore, since $0 \leq \cos(2\omega t) \leq 1$ holds during the providing period, the discharge duty dc set by Equation (19) satisfies $0 \leq dc \leq 1$, and drec + dc + dz = 1 by increasing the both-end voltage Vc more than the amplitude Vm. For the following convenience, a voltage ratio $\alpha = Vc/Vm$ is introduced herein.

[0151] The DC voltage Vdc during the providing period can be obtained from the next Equation (20) by setting the rectifying duty drec and the discharge duty dc as described above.

[0152]

$$\begin{aligned} &Vrec \cdot drec + Vc \cdot dc + 0 \cdot dz \\ &= Vm \cdot \sqrt{2} \cdot \sin^2(\omega t) + Vm \cdot \cos(2\omega t) \quad (20) \\ &= \frac{Vm}{\sqrt{2}}\left[1 + \left(\sqrt{2} - 1\right) \cdot \cos(2\omega t)\right] \end{aligned}$$

[0153] Equation (20) approximates Equation (16) well when, for example, the phase ωt takes a value ranging from $3\pi/4$ to $5\pi/4$ during the providing period. Specifically, it is known that a difference in integral value over the providing period between the DC voltage Vdc expressed by Equation (16) and the DC voltage Vdc expressed by Equation (20) is less than 1%.

[0154] As described above, satisfying dc = dz = 0 during the receiving period and using the duty drec and the duty dc expressed by Equation (18) and Equation (19) allow the waveforms of the DC voltage Vdc to be approximated to the ones expressed by Equation (16), thus improving the voltage utilization factors R.

[0155] (g-3) Reactor current il

During the providing period, the discharge duty dc expressed by Equation (19) adopted in the second embodiment is Vm/Vdc times that in Equation (11) adopted in the first embodiment. Since $Vdc/Vm = 2\sqrt{2}/\pi$ holds in the second embodiment as clarified from Equation (17), the discharge duty dc according to the second embodiment is $\pi/(2\sqrt{2})$

times that according to the first embodiment.

[0156] Thus, the amount of charge to be provided to the DC link 7 by the discharge current ic during the providing period according to the second embodiment is $k \cdot \pi/(2\sqrt{2})$ times that according to the first embodiment in consideration of the distribution factor k. Thus, the reactor current il flowing during the receiving period has to be $k \cdot \pi/(2\sqrt{2})$ times that according to the first embodiment. Thus, the reactor current command il* is set by the next Equation (21) in consideration of Equation (3).

[0157]

$$il^* = Im \cdot \left(|\sin(\omega t)| - \frac{1}{2 \cdot |\sin(\omega t)|} \right) \cdot k \cdot \frac{\pi}{2\sqrt{2}} \qquad (21)$$

[0158] Thus, Equations (22) yield the function F2 (ωt) in the second embodiment from Equations (15) and (21).

[0159]

$$\begin{aligned} iL^* &= Im \cdot F2(\omega t) \\ F2(\omega t) &= F1(\omega t) \cdot \frac{k \cdot \pi}{2\sqrt{2}} \\ &= \frac{k \cdot \pi}{2\sqrt{2}} \left[1 - \frac{1}{2 \cdot \sin^2(\omega t)} \right] \end{aligned} \qquad (22)$$

[0160] The function F2 (ωt) is determined according to the distribution factor k, the discharge duty dc which is determined at value 0 during the receiving period and determined by Equation (19) during the providing period, and the rectifying duty drec which is determined at value 1 during the receiving period and determined by Equation (18) during the providing period.

[0161] As seen from the current irec indicated by FIGS. 10 and 11 to be described later, a sinusoidal waveform of the input current Iin as the basis of Equation (3) does not hold

in the second embodiment. Thus, strictly speaking, application of Equation (3) is not rational to obtain Equations (22).

[0162] However, in consideration of the overall receiving period, Equation (3) holds even when the input current Iin does not have a sinusoidal waveform. Thus, the function F2 (ωt) may be determined with the input current Iin having a sinusoidal waveform also according to the second embodiment.

[0163] In other words, considering that the reactor current il flows only during the receiving period, a product of the rectified voltage Vrec and the reactor current command il* expressed by Equation (3) suffices the AC component $\hat{Pin}$.

[0164] Calculating the product yields the next Equation (23), thus clarifying that the product Vrec · il* is equal to the AC component $\hat{Pin}$.

[0165]

$$\begin{aligned} Vrec \cdot il^* &= Vm \cdot |\sin(\omega t)| \cdot Im \cdot \left(|\sin(\omega t)| - \frac{1}{2 \cdot \sin(\omega t)} \right) \\ &= Vm \cdot Im \cdot \left[\sin^2(\omega t) - \frac{1}{2} \right] \\ &= -\frac{Vm \cdot Im}{2} \cdot \cos(2\omega t) \end{aligned} \qquad (23)$$

[0166] Since Equations (6) and (10) hold independent of the rectifying duty drec and the discharge duty dc, the DC current Idc is obtained from the next Equation (24) using Equations (6) and (10) also in the second embodiment. Here, the DC voltage Vdc is approximated by Equation (16).

[0167]

$$Idc = \frac{Pdc}{Vdc} = \frac{Vm \cdot Im}{2 \cdot Vdc} [1 - (1 - k) \cdot \cos(2\omega t)] \qquad (24)$$

[0168] Accordingly, the charge command iL* can be obtained using the function F2 (ωt) according to the second embodiment similarly as the function F1 (ωt) according to

included in the DC voltage Vdc have the same waveforms in both FIGS. 10 and 11.

[0173] However, since the DC current Idc is expressed by Equation (24) and depends on the distribution factor k, it largely differs between k = 1 in FIG. 10 and k = 1/3 in FIG. 11.

[0174] The currents ic and il in the tier third from the top in FIG. 11 where k = 1/3 are reduced more than those in FIG. 10 where k = 1. Such reduction in the currents il and ic is preferable in view of reduction in the power capacitance required for the reactor L4 and the capacitor C4 that are used in the power buffer circuit 4, and downsizing the reactor L4 and the capacitor C4 and reduction in their costs.

[0175] (g-5) Example of technique for distributing ripple of power according to distribution factor k

This section will describe an example of a technique for satisfying Equation (24) and distributing the ripple of power according to the distribution factor k.

[0176] In this example, operations on a normal AC load are dq-axis controlled which is well known. The power equation on the dq-axis is generally expressed by Equation (25). The symbols V* and I denote a command value of a voltage to be applied to the AC load and a current flowing through the AC load, respectively. Since these are alternating, a dot representing a complex number is on each of the symbols V* and I. Note that a q-axis voltage and a d-axis voltage ideally follow a command value (hereinafter referred to as a "q-axis voltage command value") Vq* and a command value (hereinafter referred to as a "d-axis voltage command value") Vd*, respectively.

[0177]

$$P + jQ = \dot{V}^* \cdot \dot{I} = Vd^* \cdot Id + Vq^* \cdot Iq + j(Vq^* \cdot Id - Vd^* \cdot Iq) \quad (25)$$

[0178] Since the power supplied from the DC power lines LH and LL to the inverter 5 has no reactive power, the power is expressed by Equation (26) with disregard of the

second term of Equation (25).

[0179]

$$Pdc = Vd^* \cdot Id + Vq^* \cdot Iq \qquad (26)$$

[0180] Thus, control can be performed by matching the AC component of Equation (26) with the second term in the right side of Equation (6) to satisfy Equation (24). FIG. 12 is a block diagram illustrating an example of a structure for performing the control. The structure is provided for, for example, the output voltage command generating unit 1011 in FIG. 2.

[0181] First, portions based on the prior art in the structure of FIG. 12 will be simply described. Trigonometric function values $\cos\beta^*$ and $-\sin\beta^*$ are obtained from a current phase command value β^*, and a q-axis current command value Iq* and a d-axis current command value Id* are generated from the obtained trigonometric function values $\cos\beta^*$ and $-\sin\beta^*$ and a current command value Ia*. Assuming the inductive load 6 as a rotary machine, a q-axis voltage command value Vq* and a d-axis voltage command value Vd* are obtained on the basis of the rotational angular velocity ωm, a field flux Φa, a d-axis inductance Ld, and a q-axis inductance Lq of the rotary machine, the q-axis current command value Iq*, the d-axis current command value Id*, a q-axis current Iq, and a d-axis current Id. Then, voltage command values Vu*, Vv*, and Vw* are generated to control the inverter 5 using the q-axis voltage command value Vq* and the d-axis voltage command value Vd*.

[0182] In the structure illustrated in FIG. 1, for example, the velocity sensor 9 senses the load currents iu, iv, and iw flowing through the inductive load 6, and provides the control device 10 with the rotational angular velocity ωm, the q-axis current Iq, and the d-axis current Id based on the load currents iu, iv, and iw.

[0183] Hereinafter, a processor 71 that performs the control for matching the AC

using the output of the PI processor 716. Specifically, a subtractor 701 calculates a deviation between the rotational angular velocity ωm and its command value ωm* as the normal processes for obtaining the current command value Ia*. A PI processor 702 performs proportional-integral control on the deviation to temporarily obtain the current command value Ia*. Then, the adder 715 increases the current command value Ia* using the output from the PI processor 716.

[0189] Then, the q-axis voltage command value Vq* and the d-axis voltage command value Vd* are generated by applying the known technique to the current command value Ia* corrected by the processor 71 in such a manner. Such a control is performed by applying feedback to the q-axis voltage command value Vq*, the d-axis voltage command value Vd*, the q-axis current Iq, and the d-axis current Id so that the difference output from the subtractor 714 converges to 0. In other words, such a control enables the AC component of Equation (26) to be matched with the second term in the right side of Equation (6).

[0190] H. Third embodiment

(h-1) Setting of duty

The third embodiment does not adopt the quarter-period control adopted in the first and second embodiments. In other words, the rectifying duty drec and the discharge duty dc are defined without particularly distinguishing between the receiving period and the providing period in the third embodiment. However, the rectifying duty drec and the discharge duty dc do not depend on the distribution factor k, similarly as the first and the second embodiments.

[0191] Specifically, the rectifying duty drec and the discharge duty dc are determined by Equation (27) and Equation (28), respectively.

[0192]

$$\mathrm{drec} = \frac{\mathrm{Vdc}}{\mathrm{Vm}} \cdot \left|\sin(\omega t)\right| \qquad (27)$$

[0193]

$$\begin{aligned} \mathrm{dc} &= \frac{\mathrm{Vdc}}{\mathrm{Vc}} \cdot \cos^2(\omega t) \\ &= \frac{\mathrm{Vdc}}{2 \cdot \mathrm{Vc}} \cdot \left[1 + \cos(2\omega t)\right] \end{aligned} \qquad (28)$$

[0194] Although the both-end voltage Vc contains ripples to be described later, it is maintained almost constant. Thus, the discharge duty dc is in direct proportion to [1 + cos (2ωt)], and varies at a frequency twice that of the single-phase AC voltage Vin as a fundamental frequency. Since the discharge duty dc is defined without distinguishing between the receiving period and the providing period in the third embodiment as described above, the providing power Pc provided by the power buffer circuit 4 to the DC link 7 also varies at the frequency twice that of the single-phase AC voltage Vin as a fundamental frequency.

[0195] Equation (29) is obtained from Equations (27) and (28). Accordingly, Equation (7) identically holds. Thus, the DC voltage Vdc can be set to a constant value.

[0196]

$$\begin{aligned} &\mathrm{Vrec} \cdot \mathrm{drec} + \mathrm{Vc} \cdot \mathrm{dc} + 0 \cdot \mathrm{dz} \\ &= \mathrm{Vm} \cdot \left|\sin(\omega t)\right| \cdot \frac{\mathrm{Vdc}}{\mathrm{Vm}} \cdot \left|\sin(\omega t)\right| + \mathrm{Vdc} \cdot \cos^2(\omega t) \\ &= \mathrm{Vdc} \end{aligned} \qquad (29)$$

[0197] Furthermore, $0 \leq \mathrm{drec} \leq 1$ is satisfied under $\mathrm{Vdc} \leq \mathrm{Vm}$. Furthermore, setting the DC voltage Vdc lower than or equal to the both-end voltage Vc can establish a setting that satisfies $0 \leq \mathrm{dc} \leq 1$ and $\mathrm{drec} + \mathrm{dc} + \mathrm{dz} = 1$.

[0198] (h-2) Reactor current il

Next, the reactor current il required to satisfy Equation (6), that is, the reactor

current command il* is obtained. Since the input power Pdc is expressed by a product of the DC voltage Vdc and the DC current Idc as described above, the current irec1 is obtained by the next Equation (30) from Equations (24) and (27).

[0199]

$$\begin{aligned} irecl &= drec \cdot Idc \\ &= \frac{Vdc}{Vm} \cdot \left|\sin(\omega t)\right| \cdot \frac{Vm \cdot Im}{2 \cdot Vdc} \cdot \left[1-(1-k)\cdot\cos(2\omega t)\right] \\ &= \frac{Im}{2} \cdot \left|\sin(\omega t)\right| \cdot \left[1-(1-k)\cdot\cos(2\omega t)\right] \end{aligned} \qquad (30)$$

[0200] Then, the reactor current command il* is determined by the next Equation (31) so that the input current Iin has a sinusoidal waveform. As understood from Equation (31), the reactor current command il* varies at the frequency twice that of the single-phase AC voltage Vin as a fundamental frequency. Furthermore, the rectified voltage Vrec varies in the same manner. Thus, the receiving power Pl received by the power buffer circuit 4 from the DC link 7 also varies at the frequency twice that of the single-phase AC voltage Vin as a fundamental frequency.

[0201] Consequently, both the receiving power Pl and the providing power Pc are set to vary at the frequency twice that of the single-phase AC voltage Vin as a fundamental frequency according to the third embodiment.

[0202]

$$\begin{aligned} il^* &= Im \cdot \left|\sin(\omega t)\right| - irecl \\ &= \frac{Im}{2} \cdot \left|\sin(\omega t)\right| \cdot \left[1+(1-k)\cdot\cos(2\omega t)\right] \end{aligned} \qquad (31)$$

[0203] Furthermore, Equations (32) can yield a function F3 (ωt) from Equation (31) according to the third embodiment.

[0204]

CLAIMS

1. A direct-power-converter control device that controls a direct power converter,

said direct power converter including:

a DC link including a first power supply line and a second power supply line;

a converter that receives a single-phase AC voltage, and outputs ripple power to said DC link in which said first power supply line is higher in potential than said second power supply line;

a power buffer circuit provided between said first and second power supply lines, said power buffer circuit buffering power by buffered power obtained by multiplying an AC component of said ripple power by a distribution factor; and

an inverter that converts a DC voltage between said first and second power supply lines into an AC voltage,

said power buffer circuit including:

a discharge circuit including a capacitor and a switch connected in series with said capacitor between said first and second power supply lines, said switch being closer to said first power supply line relative to said capacitor; and

a charge circuit that charges said capacitor,

said control device comprising an inverter controller, a discharge controller, and a charge controller,

wherein said inverter controller outputs an inverter control signal for controlling an operation of said inverter on the basis of a rectifying duty, a discharge duty, and a command value of a voltage to be output by said inverter, said rectifying duty being a duty at which said

converter is brought into conduction with said DC link, said discharge duty being a duty at which said switch is conducting,

said discharge controller outputs a discharge switch signal for bringing said switch into conduction on the basis of said discharge duty, and

said charge controller includes:

an amplitude determining unit that determines an amplitude of an input current to be input to said converter by performing at least proportional-integral control on a deviation between a voltage across said capacitor and an average voltage command value that is a command value of an average of said voltage across said capacitor;

a charge command generating unit that determines a charge command on a current flowing through said charge circuit by multiplying by said amplitude a function of a phase of said single-phase AC voltage, said function being determined according to said discharge duty, said rectifying duty, and said distribution factor; and

a charging operation controller that controls a charging operation of said charge circuit on the basis of said charge command.

2. The direct-power-converter control device according to claim 1,

wherein said discharge duty and said rectifying duty are set so that said power buffer circuit receives power from said DC link during a period during which a cosine value is negative and provides power to said DC link during a period during which said cosine value is positive, said cosine value being a cosine of a value twice said phase.

3. The direct-power-converter control device according to claim 1,

wherein power received by said power buffer circuit from said DC link and power provided by said power buffer circuit to said DC link are set to vary at a frequency twice a frequency of said single-phase AC voltage as a fundamental frequency.

4. The direct-power-converter control device according to one of claims 1 to 3,

wherein said function is determined with said input current having a sinusoidal waveform.

5. The direct-power-converter control device according to claim 1,

wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

6. The direct-power-converter control device according to claim 2,

wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

7. The direct-power-converter control device according to claim 3,

wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

8. The direct-power-converter control device according to claim 4,

wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

ABSTRACT

In a power buffer circuit included in a direct power converter, variations in voltage across a buffer capacitor are suppressed even when the electrostatic capacity of the buffer capacitor varies. A control device (10) includes a charge controller (103). The charge controller (103) includes an amplitude determining unit (103a), a charge command generating unit (103b), and a charging operation controller (103c). The amplitude determining unit (103a) determines an amplitude (Im) of a current to be input to a converter by performing at least proportional-integral control on a deviation (ΔVc) between a voltage (Vc) across the buffer capacitor and an average voltage command value (Vc*) that is a command value of an average of the voltage (Vc) across the buffer capacitor. The charge command generating unit (103b) determines a charge command (iL*) by multiplying by the amplitude (Im) a function (F(θ)) determined according to a discharge duty (dc), a rectifying duty (drec), and a distribution factor of power. The charging operation controller (103c) controls a charging operation of the buffer capacitor on the basis of the charge command (iL*).