TESTING CIRCUIT, TESTING DEVICE AND TESTING METHOD THEREFOR

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese patent application No. 2020108929685 filed on August 31, 2020, and entitled “TESTING CIRCUIT, TESTING DEVICE AND TESTING METHOD THEREFOR”, the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The disclosure relates to a testing circuit, a testing device and a testing method therefor.

BACKGROUND

[0003] A memory is a device configured to store data. The memory usually includes multiple storage arrays, and each storage array includes multiple memory cells. The memory cells serve as basic unit structures for storing data, and each memory cell has a data storage function.

[0004] When reading and writing operations are performed on the memory, it needs to be controlled by a pulse signal. Exemplarily, the pulse signal may be configured to control a transistor pair connected to a word line to be on or off. Specifically, when the pulse signal is valid, reading or writing operations are performed on the memory cells, and when the pulse signal is invalid, the memory cells keep the original data. As the requirements for the reading and writing speed of the memory continue to be higher, it is necessary to further increase a transmission frequency of the pulse signal and reduce a pulse width. In order to ensure the reliability of the pulse signal, it is necessary to test the pulse width through a testing circuit to ensure that the generated pulse signal is the same as a designed signal.

SUMMARY

[0005] According to some embodiments, a first aspect of the disclosure provides a testing circuit, including:

[0006] a first sampling module, configured to receive a to-be-tested pulse signal, and generate a first sampled signal according to the pulse signal; and

[0007] a second sampling module, configured to receive the pulse signal, and generate a second sampled signal according to the pulse signal,

[0008] where the second sampled signal and the first sampled signal have a phase difference, the phase difference being equal to a pulse width of the pulse signal.

[0009] According to some embodiments, a second aspect of the disclosure provides a testing device, including:

[0010] the above-mentioned testing circuit; and

[0011] an analysis module, connected to the testing circuit, and configured to obtain a width of a pulse signal according to the first sampled signal and the second sampled signal.

[0012] According to some embodiments, a third aspect of the disclosure provides a testing method, based on the above-mentioned testing device, including:

[0013] a to-be-tested pulse signal is received;

[0014] a first sampled signal and a second sampled signal are generated according to the pulse signal; and

[0015] the first sampled signal and the second sampled signal are obtained, and a width of the pulse signal is obtained according to the first sampled signal and the second sampled signal,

[0016] where the second sampled signal and the first sampled signal have a phase difference, the phase difference being equal to a pulse width of the pulse signal.

[0017] Details of one or more embodiments of the disclosure will be proposed in the

following drawings and descriptions. Other features and advantages of the disclosure will become apparent from the description, the accompanying drawings and the claims.

BRIEF DESCRIPTION OF THEDRAWINGS

[0018] In order to more clearly illustrate the technical solutions of embodiments of the disclosure or the traditional technology, the accompanying drawings required for describing the embodiments or the traditional technology will be briefly introduced below. It is apparent that the accompanying drawings in the following description show only some embodiments of the disclosure, and those of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

[0019] FIG. 1 illustrates a schematic structural diagram of a testing circuit of a first embodiment.

[0020] FIG. 2 illustrates a signal timing diagram of an embodiment.

[0021] FIG. 3 illustrates a schematic structural diagram of a testing circuit of a second embodiment.

[0022] FIG. 4 illustrates a schematic structural diagram of a testing circuit of a third embodiment.

[0023] FIG. 5 illustrates a schematic structural diagram of a testing circuit of a fourth embodiment.

[0024] FIG. 6 illustrates a signal timing diagram of another embodiment.

[0025] FIG. 7 illustrates a schematic structural diagram of a testing circuit of a fifth embodiment.

[0026] FIG. 8 illustrates a schematic structural diagram of a testing device of an embodiment.

[0027] FIG. 9 illustrates a flow chart of a testing method of an embodiment.

[0028] Description of element reference numerals:

[0029] Testing circuit: 10; transmission gate: 210; second sampling module: 200; second inverter: 130; second temporary storage unit: 220; third inverter: 140; fourth inverter: 230; fifth inverter: 240; first sampling module: 100; first inverter: 120; first temporary storage unit: 110; and analysis module: 20.

DETAILED DESCRIPTION

[0030] With the continuous narrowing of a pulse width, higher requirements are raised for a testing circuit and a testing device of the pulse width, and an existing testing circuit can no longer accurately test the narrowing pulse width.

[0031] In order to facilitate the understanding of embodiments of the disclosure, the embodiments of the disclosure will be described in a more comprehensive manner with reference to related drawings. Preferred embodiments of the embodiments of the disclosure are shown in the accompanying drawings. The embodiments of disclosure may, however, be embodied in many different forms which are not limited to the embodiments described herein. Rather, these embodiments are provided so that the disclosure of the embodiments of the disclosure will be more thorough and complete.

[0032] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by those skilled in the art to which the embodiments of the disclosure belong. The terms used herein in the specification of the embodiments of the disclosure are for the purpose of describing specific embodiments only and are not intended to be limiting of the embodiments of the disclosure. The term "and/or" as used herein includes any and all combinations of one or more related listed items.

[0033] In the description of the embodiments of the disclosure, it is to be understood that directions or positional relationships indicated by the terms "upper", "lower", "vertical", "horizontal", "inner", and "outer" are the directions or positional relationships based on the accompanying drawings. They are only for the convenience of describing the embodiments of the disclosure and simplifying the description, rather than indicating or implying that a device or element referred to must have a specific orientation or be constructed and operated in a specific orientation, and therefore cannot be understood as restrictions on the embodiments of the application.

[0034] FIG. 1 illustrates a schematic structural diagram of a testing circuit 10 of a first embodiment. The testing circuit 10 is configured to process a to-be-tested pulse signal and obtain a pulse width of the to-be-tested pulse signal through the processed signal. With reference to FIG. 1, the testing circuit includes a first sampling module 100 and a second sampling module 200. The first sampling module 100 and the second sampling module 200 may be sampling circuits respectively.

[0035] The first sampling module 100 is configured to receive the to-be-tested pulse signal, and generate a first sampled signal according to the pulse signal.

[0036] The to-be-tested pulse signal is generated by a pulse generator and is divided into at least two paths. One path of the pulse signal is transmitted to the testing circuit 10 for testing, and the other path of the pulse signal is transmitted to a memory array to control data reading and writing of the memory array. The to-be-tested pulse signal includes at least one pulse, and the pulse width of the pulse signal refers to a duration of a high level of the pulse. When the pulse signal includes a plurality of pulses, pulse widths of the plurality of pulses may be the same or different.

[0037] In particular, taking one pulse as an example for description, it is understandable that a signal with a certain pulse width has a rising edge and a falling edge, and a time interval between the rising edge time and the falling edge time is the pulse width. Generating the first sampled signal according to the pulse signal refers to generating the first sampled signal in response to a level change of the pulse signal, that is, generating the first sampled signal in response to the rising edge or the falling edge of the pulse signal.

[0038] The second sampling module 200 is configured to receive the pulse signal, and generate a second sampled signal according to the pulse signal.

[0039] In particular, the first sampling module 100 generates the first sampled signal in response to one of the rising edge and the falling edge of the pulse signal, and the second sampling module 200 generates the second sampled signal in response to the other of the rising edge and the falling edge of the pulse signal. The second sampled signal and the first sampled signal have a phase difference. For example, the first sampled signal and the second sampled signal may have a same signal waveform, but have the phase difference in, that is, if one of the first sampled signal and the second sampled signal is delayed corresponding to the

phase difference, the signal may coincide with the other signal. According to a generation principle of the first sampled signal and the second sampled signal, the phase difference is equal to the pulse width of the pulse signal. Therefore, the pulse width of the pulse signal may be further obtained according to the first sampled signal and the second sampled signal.

[0040] In the embodiment, the testing circuit 10 includes: the first sampling module 100 configured to receive the to-be-tested pulse signal and generate the first sampled signal according to the pulse signal, and the second sampling module 200 configured to receive the pulse signal and generate the second sampled signal according to the pulse signal, in which the second sampled signal and the first sampled signal have a phase difference, the phase difference being equal to the pulse width of the pulse signal. In the embodiment, two sampled signals are generated based on one pulse signal, that is, the pulse signal with a narrow pulse width is split into the first sampled signal and the second sampled signal that are easier to identify and calculate, so as to reduce the requirement for testing speed and testing accuracy of a subsequent analysis module 20 and to provide the testing circuit 10 with higher accuracy.

[0041] Further, by generating the first sampled signal and the second sampled signal with the same waveform, the difficulty of identifying the first sampled signal and the second sampled signal may be reduced, thereby improving the testing accuracy. Exemplarily, the first sampled signal and the second sampled signal may both be square wave signals, and have a same signal amplitude, frequency and duty cycle, so that phase information may be obtained by identifying the rising edges or the falling edges of the first sampled signal and the second sampled signal. The first sampled signal and the second sampled signal may also be sine wave signals and have the same signal amplitude and frequency, so that the phase information may be obtained by identifying peaks or valleys of the first sampled signal and the second sampled signal. In other examples, the first sampled signal and the second sampled signal may also be signals of other waveforms such as triangle waves, sawtooth waves, etc. The embodiment of the disclosure does not specifically limit the waveforms thereof.

[0042] Furthermore, even if the signal waveforms of the first sampled signal and the second sampled signal are different, as long as the first sampled signal and the second sampled signal are both generated based on the input pulse signal, and the phase information of the first sampled signal and the second sampled signal may be obtained through the analysis module 20 so that the pulse width may be obtained by analyzing the obtained phase information, this solution also belongs to the protection scope of the disclosure.

[0043] In one of the embodiments, the first sampling module 100 generates the first sampled signal in response to the falling edge of the pulse signal, and the second sampling module 200 generates the second sampled signal in response to the rising edge of the pulse signal.

[0044] In particular, FIG. 2 illustrates a signal timing diagram of an embodiment. With reference to FIG. 2, in the embodiment, the pulse signal includes one pulse, and initial states of the first sampled signal and the second sampled signal are both 0. The state of the first sampled signal is switched in response to the falling edge of the pulse signal, that is, the state is switched from a state '0' to a state '1', and the state of the first sampled signal is switched at a moment t2. The state of the second sampled signal is switched in response to the rising edge of the pulse signal, that is, the state is switched from the state '0' to the state '1', and the state of the second sampled signal is switched at a moment t1. In the embodiment, a time interval between t1 and t2 is the pulse width T1. In the embodiment, the pulse width may be obtained through calculation by obtaining the switching moments of the two signals without the need to sample the rising and falling edges of the same pulse with a very short time interval through a testing machine, thereby reducing the requirements for response speed of the testing machine and improving testing accuracy of the pulse width.

[0045] In one of the embodiments, a first delay time of the first sampling module 100 on a transmission path is equal to a second delay time of the second sampling module 200 on a data transmission path. With further reference to FIG. 1, an output terminal of the pulse generator is defined as A, the first sampled signal and the second sampled signal are transmitted to the same analysis module 20 for analysis, a port of the analysis module 20 for receiving the first sampled signal is defined as B1, a port of the analysis module 20 for receiving the second sampled signal is defined as B2, and then the first delay time is a transmission time of the signal on a path AB, while the second delay time is a transmission time of the signal on a path AB2. Exemplarily, elements with similar data processing and transmission time may be arranged in the first sampling module 100 and the second sampling module 200 respectively, so that the first delay time and the second delay time are equal. In the embodiment, by setting the delay time to be equal, the synchronization of the first sampled signal and the second sampled signal may be improved, thereby reducing the influence of difference in signal reception moments on a testing result. It is to be noted that considering actual circuit conditions, the above-mentioned time equality does not mean absolute equality,

but a certain error is allowed, as long as the error has a small impact on a pulse width test, such as a 1% error.

[0046] FIG. 3 illustrates a schematic structural diagram of a testing circuit 10 of a second embodiment. With reference to FIG. 3, in this embodiment, a first sampling module 100 includes: a first temporary storage unit 110 configured to sample a first to-be-sampled signal in response to a pulse signal so as to generate a first temporary storage signal. A triggering type of the temporary storage unit 110 is edge triggering, and an edge of the first temporary storage signal corresponds to a first edge of the pulse signal and corresponds to an edge of a first sampled signal. The first temporary storage unit 110 includes one or more of a trigger, a latch or a register.

[0047] In the embodiment, the first temporary storage unit 110 may sample and latch an edge of the pulse signal, so as to accurately and stably output the first temporary storage signal. Further, since the edge of the first temporary storage signal corresponds to the first edge (for example, a falling edge) of the pulse signal, the first temporary storage signal may be output as the first sampled signal and a pulse width of the input pulse signal may be analyzed. It can be understood that, in order to make a first delay time and a second delay time equal, a second temporary storage unit 220 may be arranged in a second sampling module 200, and the structure of the second temporary storage unit 220 is of the same structure as the first temporary storage unit 110, so that the synchronization of the signals and the accuracy of a testing result are improved.

[0048] In one of the embodiments, the first sampling module 100 further includes: a third inverter 140. An input terminal of the third inverter 140 is connected to the pulse signal, an output terminal of the third inverter 140 is connected to a drive terminal of the first temporary storage unit 110, and the third inverter 140 is configured to receive the pulse signal and output an inverted pulse signal to the first temporary storage unit 110.

[0049] In order to realize that sampling edges of the first temporary storage unit 110 and the second temporary storage unit 220 are different, on the one hand, response setting may be made in internal structures of the temporary storage units, that is, exemplarily, the first temporary storage unit 110 is made to respond to the falling edge and the second temporary storage unit 220 is made to respond to a rising edge. On the other hand, the internal structures of the first temporary storage unit 110 and the second temporary storage unit 220 may also be

completely the same, and sampling of different edges may be realized by changing input signals. That is, exemplarily, the first temporary storage unit 110 and the second temporary storage unit 220 are both made to respond to the rising edge, but the third inverter 140 is arranged in front of the first temporary storage unit 110; and after the input pulse signal passes the third inverter 140, an original state '0' is inverted into '1' and an original state '1' is inverted into '0', so that the rising edge in the original signal is converted into a falling edge, and the falling edge in the original signal is converted a rising edge. Through the above-mentioned structure of this embodiment, the first temporary storage unit 110 may sample the rising edge of the inverted pulse signal, but actually sample the falling edge of the pulse signal, and the second temporary storage unit 220 is not connected to the inverter, so that sampling of different edges of the first temporary storage unit 110 and the second temporary storage unit 220 is realized.

[0050] Further, in order to make the first delay time the same as the second delay time, a transmission gate 210 may be arranged on a data transmission path of the second temporary storage unit 220, and a delay time of the transmission gate 210 is equal to a delay time of the third inverter 140. In the embodiment shown in FIG. 3, the transmission gate 210 is arranged between the pulse generator and the second temporary storage unit 220. In other embodiments, the transmission gate 210 may also be connected to an output terminal the second temporary storage unit 220, and the effect of the above equal delay time may still be realized.

[0051] FIG. 4 illustrates a schematic structural diagram of a testing circuit 10 of a third embodiment. With reference to FIG. 4, in the embodiment, a first temporary storage unit 110 and a second temporary storage unit 220 are both D triggers, input terminals of the first temporary storage unit 110 and the second temporary storage unit 220 are both connected to a same to-be-sampled signal source, reset terminals of the first temporary storage unit 110 and the second temporary storage unit 220 are both connected to a reset signal source, a drive terminal of the first temporary storage unit 110 is connected to an inverted pulse signal, and a drive terminal of the second temporary storage unit 220 is connected to a pulse signal. In particular, the to-be-sampled signal source has a constant output. In the embodiment, the to-be-sampled signal source may output a high level constantly. When a reset signal output by the reset signal source is enabled, the first temporary storage unit 110 and the second temporary storage unit 220 both output a state '0'; when the reset signal output by the reset signal source is not enabled, the first temporary storage unit 110 and the second temporary

storage unit 220 sample a to-be-sampled signal in response to signals input by the drive terminals respectively, and therefore are switched to output a state '1' respectively at different moments.

[0052] In other embodiments, the reset signal source may also be replaced with a setting signal source, set terminals of the first temporary storage unit 110 and the second temporary storage unit 220 are both connected to the setting signal source, and the to-be-sampled signal source constantly outputs a low level. Similar to the previous embodiment, when a setting signal output by the setting signal source is enabled, the first temporary storage unit 110 and the second temporary storage unit 220 both output the state '1'; and when the setting signal output by the setting signal source is not enabled, the first temporary storage unit 110 and the second temporary storage unit 220 sample the to-be-sampled signal in response to signals input by the drive terminals respectively, and therefore are switched to output the state '0' respectively at different moments.

[0053] FIG. 5 illustrates a schematic structural diagram of a testing circuit 10 of a fourth embodiment. With reference to FIG. 5, in the embodiment, a first sampling module 100 further includes: a first inverter 120, which forms a first feedback loop together with a first temporary storage unit 110; and the first feedback loop is configured to respond to a pulse signal and generate a first feedback signal, and an edge of the first feedback signal corresponds to a first edge of the pulse signal. It is understandable that the testing circuit 10 provided in the preceding embodiment needs to continuously switch signals input by a reset signal source so that pulse widths of multiple consecutive pulses can be tested, and the switching of reset signals needs to be matched with arrival times of pulses so that the pulse widths can be accurately tested.

[0054] Specifically, an input terminal of the first inverter 120 is connected to an output terminal of the first temporary storage unit 110, an output terminal of the first inverter 120 is connected to an input terminal of the first temporary storage unit 110, and the first inverter 120 is configured to invert a first temporary storage signal so as to generate the first feedback signal.

[0055] In the embodiment, the first feedback loop is formed by the first temporary storage unit 110 and the first inverter 120, and feedback is made through the first feedback signal, so that the first sampling module 100 in the testing circuit 10 may realize automatic switching

and testing. Correspondingly, a fourth inverter 230 is also arranged in a second sampling unit, so that a second temporary storage unit 220 and the fourth inverter 230 jointly form a second feedback loop, thereby realizing automatic switching and testing of a second sampling module 200. Further, FIG. 6 is a signal timing diagram of another embodiment. With reference to FIG. 6, an edge of the first feedback signal may correspond to a falling edge of the pulse signal, and an edge of a second feedback signal may correspond to a rising edge of the pulse signal, and the first feedback signal is output as a first sampled signal while the second feedback signal is output as a second sampled signal.

[0056] FIG. 7 illustrates a schematic structural diagram of a testing circuit 10 of a fifth embodiment. With reference to FIG. 7, in the embodiment, a first sampling module 100 further includes a second inverter 130, an input terminal of the second inverter 130 is connected to an output terminal of a first inverter 120, and the second inverter 130 is configured to receive a first feedback signal and generate a first sampled signal according to the first feedback signal. In the embodiment, by arranging the second inverter 130, a switching mode of the first sampled signal may be made to correspond to a switching mode of a signal output by a first temporary storage unit 110.

[0057] With further reference to FIG. 7, in the embodiment, a second sampling module 200 includes a transmission gate 210, a second temporary storage unit 220, a fourth inverter 230 and a fifth inverter 230.

[0058] An input terminal of the transmission gate 210 is connected to a pulse signal, an output terminal of the transmission gate 210 is connected to a drive terminal of the second temporary storage unit 220 and the transmission gate 210 is configured to transmit the pulse signal to the second temporary storage unit 220.

[0059] An input terminal of the second temporary storage unit 220 is connected to an output terminal of the fourth inverter 230, the second temporary storage unit 220 is configured to sample a signal output by the fourth inverter 230 in response to the pulse signal so as to generate a second temporary storage signal and an edge of the second temporary signal corresponds to a second edge of the pulse signal.

[0060] The fourth inverter 230 is configured to invert the second temporary signal so as to generate a second feedback signal.

[0061] An input terminal of the fifth inverter 240 is connected to an output terminal of the fourth inverter 230, and the fifth inverter 240 is configured to receive the second feedback signal and generate a second sampled signal according to the second feedback signal.

[0062] In particular, the first temporary storage unit 110 corresponds to the second temporary storage unit 220, the first inverter 120 corresponds to the fourth inverter 230, the second inverter 130 corresponds to the fifth inverter 240, and the third inverter 140 corresponds to the transmission gate 210. Therefore, the second sampling module 200 of the embodiment may refer to the implementation of the first sampling module 100 described above, which will not be repeated here.

[0063] FIG. 8 illustrates a schematic structural diagram of a testing device of an embodiment. With reference to FIG. 8, in the embodiment, the testing device includes: the above-mentioned testing circuit 10; and an analysis module 20 connected to the testing circuit 10 and configured to obtain a width of a pulse signal according to the first sampled signal and the second sampled signal. The analysis module 20 may be an analysis circuit. For the specific limitation of the testing circuit 10, reference may be made to the above limitation, which will not be repeated here. In the embodiment, the testing device realizing accurate pulse width tests is realized by the testing circuit 10 and the analysis module 20.

[0064] FIG. 9 illustrates a flow chart of a testing method of an embodiment, based on the above-mentioned testing device. With reference to FIG. 9, in the embodiment, the method includes S100 to S300.

[0065] In S100, a to-be-tested pulse signal is received.

[0066] In S200, a first sampled signal and a second sampled signal are generated according to the pulse signal.

[0067] In S300, the first sampled signal and the second sampled signal are obtained, and a width of the pulse signal is obtained according to the first sampled signal and the second sampled signal.

[0068] The second sampled signal and the first sampled signal have a phase difference, and the phase difference is equal to a pulse width of the pulse signal.

[0069] It is to be noted that for specific limitation on the testing method, reference may be

made to the above limitation on the testing device, which will not be repeated here.

[0070] It is to be understood that although steps of the flow chart in FIG. 9 are shown sequentially as indicated by arrows, the steps are not necessarily performed sequentially as indicated by the arrows. Unless specifically stated otherwise herein, the steps are not performed in a strict order of limitation, and the steps may be performed in other orders. Moreover, at least a part of the steps in the flow chart may include multiple sub steps or stages that are not necessarily performed at the same time, but may be performed at different times, and the steps or stages are not necessarily performed in sequence, but rather may be performed in turns or alternatively with other steps or at least a part of the steps or stages in the other steps.

[0071] The technical features of the above embodiments can be combined arbitrarily. In order to make the description concise, all possible combinations of various technical features in the above embodiments are not completely described. However, as long as there is no contradiction in the combination of these technical features, it is to be regarded as the scope of this specification.

[0072] The foregoing embodiments only describe several implementations of the disclosure, and their description is specific and detailed, but cannot therefore be understood as a limitation to the patent scope of the disclosure. It is to be noted that those of ordinary skill in the art may further make variations and improvements without departing from the inventive concepts of the embodiments of the disclosure, and these all fall within the protection scope of the embodiments of the disclosure. Therefore, the scope of protection of the patent of the embodiments of the disclosure shall subject to the appended claims.

CLAIMS

1. A testing circuit, comprising:

a first sampling module, configured to receive a to-be-tested pulse signal, and generate a first sampled signal according to the pulse signal; and

a second sampling module, configured to receive the pulse signal, and generate a second sampled signal according to the pulse signal,

wherein the second sampled signal and the first sampled signal have a phase difference, the phase difference being equal to a pulse width of the pulse signal.

2. The testing circuit of claim 1, wherein the first sampling module is configured to generate the first sampled signal in response to a falling edge of the pulse signal, and the second sampling module is configured to generate the second sampled signal in response to a rising edge of the pulse signal.

3. The testing circuit of claim 1, wherein a first delay time of the first sampling module on a first transmission path is equal to a second delay time of the second sampling module on a second data transmission path.

4. The testing circuit of claim 1, wherein the first sampling module comprises:

a first temporary storage unit, configured to sample a first to-be-sampled signal in response to the pulse signal so as to generate a first temporary storage signal, wherein a triggering type of the first temporary storage unit is edge triggering, and an edge of the first temporary storage signal corresponds to a first edge of the pulse signal and corresponds to an edge of the first sampled signal.

5. The testing circuit of claim 4, wherein the first temporary storage unit comprises one or more

of a trigger, a latch or a register.

6. The testing circuit of claim 4, wherein the first sampling module further comprises:

a first inverter, wherein the first inverter and the first temporary storage unit form a first feedback loop, the first feedback loop is configured to respond to the pulse signal and generate a first feedback signal, and an edge of the first feedback signal corresponds to the first edge of the pulse signal.

7. The testing circuit of claim 6, wherein an input terminal of the first inverter is connected to an output terminal of the first temporary storage unit, an output terminal of the first inverter is connected to an input terminal of the first temporary storage unit, and the first inverter is configured to invert the first temporary storage signal so as to generate the first feedback signal.

8. The testing circuit of claim 7, wherein the first sampling module further comprises:

a second inverter, wherein an input terminal of the second inverter is connected to the output terminal of the first inverter, and the second inverter is configured to receive the first feedback signal, and generate the first sampled signal according to the first feedback signal.

9. The testing circuit of claim 4, wherein the first sampling module further comprises:

a third inverter, wherein an input terminal of the third inverter is connected to the pulse signal, an output terminal of the third inverter is connected to a drive terminal of the first temporary storage unit, and the third inverter is configured to receive the pulse signal and output an inverted pulse signal to the first temporary storage unit.

10. The testing circuit of claim 9, wherein the second sampling module comprises a transmission gate, a second temporary storage unit, a fourth inverter and a fifth inverter,

wherein an input terminal of the transmission gate is connected to the pulse signal, an

output terminal of the transmission gate is connected to a drive terminal of the second temporary storage unit, and the transmission gate is configured to transmit the pulse signal to the second temporary storage unit;

an input terminal of the second temporary storage unit is connected to an output terminal of the fourth inverter, and the second temporary storage unit is configured to, in response to the pulse signal, sample a signal output by the fourth inverter so as to generate a second temporary storage signal, an edge of the second temporary signal corresponding to a second edge of the pulse signal;

the fourth inverter is configured to invert the second temporary signal so as to generate a second feedback signal; and

an input terminal of the fifth inverter is connected to an output terminal of the fourth inverter, and the fifth inverter is configured to receive the second feedback signal, and generate the second sampled signal according to the second feedback signal.

11. The testing circuit of claim 1, wherein the first sampled signal and the second sampled signal are square wave signals, and have a same signal amplitude, frequency and duty cycle.

12. The testing circuit of claim 10, wherein the first temporary storage unit is configured to respond to a falling edge, and the second temporary storage unit is configured to respond to a rising edge.

13. The testing circuit of claim 10, wherein the first temporary storage unit and the second temporary storage unit both respond to a rising edge, and the third inverter is arranged in front of the first temporary storage unit.

14. A testing device, comprising:

the testing circuit of any of claims 1 to 13; and

an analysis module, connected to the testing circuit, and configured to obtain a width of a

pulse signal according to the first sampled signal and the second sampled signal.

15. A testing method, performed by the testing device of claim 14, the method comprising:

receiving, by the first sampling module and the second sampling module, a to-be-tested pulse signal;

generating, by the first sampling module and the second sampling module, a first sampled signal and a second sampled signal according to the pulse signal respectively; and

obtaining, by the analysis module, the first sampled signal and the second sampled signal, and obtaining a width of the pulse signal according to the first sampled signal and the second sampled signal,

wherein the second sampled signal and the first sampled signal have a phase difference, the phase difference being equal to a pulse width of the pulse signal.

16. The testing method of claim 15, wherein generating, by the first sampling module and the second sampling module, the first sampled signal and the second sampled signal according to the pulse signal respectively comprises:

generating, by the first sampling module, the first sampled signal in response to a falling edge of the pulse signal, and

generating, by the second sampling module, the second sampled signal in response to a rising edge of the pulse signal.

17. The testing method of claim 15, wherein generating, by the first sampling module, the first sampled signal comprises:

sampling, by a first temporary storage unit of the first sampling circuit, a first to-be-sampled signal in response to the pulse signal to generate a first temporary storage signal, wherein a triggering type of the first temporary storage unit is edge triggering, and an edge of the first

temporary storage signal corresponds to a first edge of the pulse signal; and

outputting, by the first temporary storage unit, the first temporary storage signal as the first sampled signal.

18. The testing method of claim 17, further comprising:

providing a first inverter; wherein the first inverter and the first temporary storage unit form a first feedback loop; and

generating, by the first feedback loop responding to the pulse signal, a first feedback signal; wherein an edge of the first feedback signal corresponds to the first edge of the pulse signal.

19. The testing method of claim 18, further comprising:

providing a second inverter; wherein an input terminal of the second inverter is connected to the output terminal of the first inverter; and

receiving, by the second inverter, the first feedback signal, and generating the first sampled signal according to the first feedback signal.

20. The testing method of claim 17, further comprising:

providing a third inverter; wherein an input terminal of the third inverter is connected to the pulse signal, an output terminal of the third inverter is connected to a drive terminal of the first temporary storage; and receiving, by the third inverter, the pulse signal and outputting an inverted pulse signal to the first temporary storage unit.