

SYSTEM AND METHOD FOR COMBINING ELECTRICAL SIGNALS

FIELD OF INVENTION

5 Embodiments of the present invention relate to combining signals in electrical systems.

BACKGROUND

10 Any electrical system requiring a plurality of MUX couplers, external connectors, transceiver pins, central processing unit (CPU) cards and buses all interconnected together, may be of considerable mass and take up substantial space.

15 Figure 1 illustrates one embodiment of a prior art electrical system 100 that includes a main CPU card 110, which is located within a housing 102. The main CPU card 110 has an A bus 111 with two terminals 111a and 111b that transmit and receive signals via signal lines 112a, 112b respectively. Terminal 111a/signal line 112a carries non-inverted voltage signals, while terminal 111b/signal line 112b
20 carries inverted voltage signals. Each of the signal lines 112a, 112b terminate at a connector 116. Connector 116 may be, for example, a coaxial connector. The connector 116 feeds the signal from the A bus 111 via a signal line 120 to another connector 124 that forms part of a mux coupler 132. The mux coupler 132 may further be connected to an external bus 182a via a signal line 136. In some
25 embodiments, external bus 182a may form part of an aircraft avionics system.

 This embodiment of the prior art electrical system 100 may further include a B Bus 113 of main CPU card 110. The B bus 113 may include two terminals 113a and 113b that transmit and receive signals via signal lines 114a, 114b respectively.
30 Terminal 113a/signal line 114a carries non-inverted voltage signals, while terminal 113b/signal line 114b carries inverted voltage signals. Each of the signal lines 114a, 114b terminate at a connector 118. Connector 118 may be, for example, a coaxial connector. The connector 118 feeds the signal from the B bus 113 via a signal line 122 to another connector 126 that forms part of an additional mux coupler 134. The
35 mux coupler 134 may further be connected to an external bus 182b via a signal line

138. In some embodiments, external bus 182b may form part of an aircraft avionics system.

The electrical system 100 may also include a backup CPU card 150, which is located within the housing 102. The backup CPU card 150 has an A bus 151 with two terminals 151a and 151b that transmit and receive signals via signal lines 152a, 152b respectively. Terminal 151a/signal line 152a carries non-inverted voltage signals, while terminal 151b/signal line 152b carries inverted voltage signals. Each of the signal lines 152a, 152b terminate at a connector 156. Connector 156 may be, for example, a coaxial connector. The connector 156 feeds the signal from the A bus 151 via a signal line 160 to another connector 164 that forms part of a mux coupler 172. The mux coupler 172 may further be connected to the external bus 182a via a signal line 176.

This embodiment of the prior art electrical system 100 may further include a B Bus 153 of the backup CPU card 150. The B bus 153 may include two terminals 153a and 153b that transmit and receive signals via signal lines 154a, 154b respectively. Terminal 153a/signal line 154a carries non-inverted voltage signals, while terminal 153b/signal line 154b carries inverted voltage signals. Each of the signal lines 154a, 154b terminate at a connector 158. Connector 158 may be, for example, a coaxial connector. The connector 158 feeds the signal from the B bus 153 via a signal line 162 to another connector 166 that forms part of an additional mux coupler 174. The mux coupler 174 may further be connected to the external bus 182b via a signal line 178.

In this embodiment of the prior art system 100, in order for the two channels (one channel from A bus 111 from the main system 110, and one channel from the A bus 151 from the backup system 150) to be connected to the same bus 182a 4 sets of transceiver signals 112a/112b/152a/152b (dual redundant for each channel) using two separate connectors 116, 156 are required to be routed out of the housing 102. These signals communicate with other external systems through the external mux couplers 132/172, each of which also requires a separate connector 124, 164. Similar limitations are found with the backup signals from each of the B busses 113, 153.

In one embodiment of the prior art system 100, a single circular connector 180 may be used to transmit each of the four signals from the A buses 111, 151 and

B busses 113, 153. This circular connector would include a signal pin for each of the non-inverted and inverted signal lines 112a, 112b, 114a, 114b, 152a, 152b, 154a and 154b from each of the CPU cards 110, 150. When several more channels are involved, each having separate non-inverted and inverted signal lines, additional connectors, transceiver pins and mux couplers are required for additional signals. All of these connectors, transceiver pins, and couples take up additional space and add weight to the system 100.

An example of an electrical system that may include of a plurality of MUX couplers, external connectors, transceiver pins, CPU cards and buses interconnected together, can be found in some avionics systems that follow the MIL-STD-1553 standard. The MIL-STD-1553 standard is the de facto avionics bus standard for the integration of military systems. The standard is used extensively in upgrade programs as well as for new applications and integration platforms in military avionics systems.

With a growing number of aircraft systems involved in upgrade programmes, many buses are required to be connected internally in an aircraft for communications between systems. This results in larger boxes to accommodate many external connectors, transceiver pins, mux couplers and cables. Moreover, upgrade programmes may introduce new systems, each also having a main and a backup function, into a single enclosure or chassis. However, there are constraints to the weight and space available in any particular aircraft to accommodate the additional components and their respective connections. Additionally, systems that include many external mux couplers, cables and transceiver pins make system engineering and design very complex.

A need therefore exists to provide a system and method that address at least one of the above problems.

SUMMARY

One aspect of the present invention provides a system for combining a plurality of electrical signals, the system comprising: a first central processing unit (CPU) located within a housing, the first CPU capable of transmitting and receiving a first signal on an A bus; a second CPU located within the housing, the second CPU

capable of transmitting and receiving a second signal on an A bus; wherein each of said first and second signals are combined on a single connector.

In some embodiments, the system may further include a first resistor network electrically connected between each of said A busses and said connector, such that said first resistor network assists in preventing an overload of one of said A busses when a signal is transmitted from the other of said A busses and output through said connector.

In some embodiments of the system each bus may further comprise a wire pair having an inverted and non-inverted signal line, said first resistor network may comprise a resistor on each wire in said wire pairs and said inverted signal line may use a first pin of said connector, while said non-inverted signal lines may use a second pin of said connector. Each of the resistors in said first resistor network may step down a voltage at a receiving terminal associated with one of said signals on said A bus to a maximum allowed by a standard for a receiving channel when said other signal channel on said A bus is transmitting.

In other embodiments, each CPU may further comprise a B bus comprising a wire pair having an inverted and non-inverted signal line. The system may further comprise a second resistor network electrically connected to said B bus of each of said CPUs and having a resistor on each wire in said wire pairs, and said inverted signal line may use a first pin of a second connector, while said non-inverted signal line may use a second pin of said second connector.

In some embodiments of the system, each of said first and second CPUs may be capable of performing identical functions. Each of said inverted and non-inverted signal lines from each of said A and B busses may terminate on a single pin of a single multi-pin connector.

In further embodiments, each of said CPUs may transmit and receive said signals according to a MIL-STD-1553 data standard.

An alternate aspect of the present invention provides a method for combining a plurality of electrical signals in a system, the method comprising the steps of: providing a first central processing unit (CPU) located within a housing, the first CPU capable of transmitting and receiving a first signal on an A bus; providing a second

CPU located within the housing, the second CPU capable of transmitting and receiving a second signal on an A bus; and providing a single connector that transmits and receives both said first signal and said second signal when combined on said connector.

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In some embodiments, the method may further include providing a first resistor network electrically connected between each of said A busses and said connector, such that said first resistor network assists in preventing an overload of one of said A busses when a signal is transmitted from the other of said A busses and output through said connector.

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In some embodiments of the method, each bus may further comprise a wire pair having an inverted and non-inverted signal line, said first resistor network may comprise a resistor on each wire in said wire pairs and said inverted signal line may use a first pin of said connector, while said non-inverted signal line may use a second pin of said connector. The method may further comprise the step of selecting a value for each resistor in said first resistor network such that each of said resistors steps down a voltage at a receiving terminal associated with one of said data channels to a maximum allowed by a standard for a receiving channel when said other data channel is transmitting.

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In alternate embodiments, each CPU may further comprise a B bus comprising a wire pair having an inverted and non-inverted signal line; and a second resistor network electrically connected to said B bus of each of said CPUs and having a resistor on each wire in said wire pairs. In further embodiments, the method may further comprise electrically connecting said inverted signal line of each of said B busses to a first pin of a second connector, and electrically connecting said non-inverted signal line of each of said B busses to a second pin of said second connector.

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In further embodiments, the method may further comprise electrically connecting each of said inverted and non-inverted signal lines from each of said A and B busses to a single pin of a single multi-pin connector. Each of said first and second central processing units may be capable of performing identical functions. In some embodiments, each of said data channels may conform to a MIL-STD-1553 data standard.

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BRIEF DESCRIPTION OF THE DRAWINGS

Example embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 illustrates one embodiment of a prior art system of combining electrical signals from two channels;

Figure 2 illustrates one embodiment of a system for combining electrical signals from two channels according to the present invention; and

Figure 3 illustrates a flow chart showing one embodiment of a method for implementing the system of Figure 2.

DETAILED DESCRIPTION

Figure 2 illustrates one embodiment of a system, designated generally as reference numeral 200, to connect transceiver signals of a main (first) CPU card 210 and a backup (second) CPU card 250 inside a housing 202, such that the signals may be output on a single external connector, such as a circular or other connector with coaxial or pin contacts. It is understood that embodiments of the present invention may be implemented by having a larger or smaller number of components that may be electrically connected in alternate configurations. The embodiment of the system 200 is provided by way of example only. It is understood that, in this embodiment of the system 200, the first CPU card 210 and the second CPU card 250 may be capable of performing identical functions. Additional CPU cards may also be added as desired.

In this embodiment, the main CPU card 210 includes an A bus 212 that transmits and receives signals via two terminals 212a and 212b. In this embodiment, terminal 212a carries non-inverted voltage signals while terminal 212b carries inverted voltage signals. Terminal 212a may be connected to a resistor R1 260 via a cable 213a. Terminal 212b may be connected to a resistor R2 261 via a cable 213b. It is understood that, in this embodiment of the system 200, the term "cable"

may refer to any form of electrical connection, for example, but not limited to, signal lines, cables, wires, traces on Printed Circuit Boards, etc.

The backup CPU card 250 includes an A bus 252 that transmits and receives
5 signals via two terminals 252a and 252b. In this embodiment, terminal 252a carries non-inverted voltage signals while terminal 252b carries inverted voltage signals. Terminal 252a may be connected to a resistor R1 264 via a cable 253a. Terminal 252b may be connected to a resistor R2 265 via a cable 253b. The resistors 260, 261 located on the A bus signal lines 213a and 213b of the first CPU card 210, and
10 the resistors 264, 265 located on the A bus signal lines 253a, 253b of the second CPU card 250 may form a single resistor network.

The signal line 253a may be connected to the signal line 213a at a node 290. Similarly, the signal line 253b may be connected to the signal line 213b at a node
15 291. The signal lines 213a and 213b may then be connected to a single contact 216 on an external connector 280. In some embodiments, contact 216 may be a coaxial contact. In alternate embodiments, each of the signal lines 213a, 213b may be connected to individual non-coaxial contacts (not shown) on a single circular connector 280. In alternate embodiments, each of the signal lines 213a and 213b
20 may be connected to a single external connector (not shown), which in some embodiments may be a coaxial connector. The connector 216/280 may then be connected via signal line 220 to another connector 224 on a mux coupler 232 that forms part of a larger system, such as an avionics system. The mux coupler 232 may then be connected to, for example, an aircraft A bus 282a.

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In this embodiment of the system 200, the main CPU card 210 may also have a B bus 214 that transmits and receives signals via two terminals 214a and 214b. In this embodiment, terminal 214a carries non-inverted voltage signals while terminal 214b carries inverted voltage signals. Terminal 214a may be connected to a resistor
30 R1 262 via a cable 215a. Terminal 214b may be connected to a resistor R2 263 via a cable 215b.

Correspondingly, the backup CPU card 250 may also have a B bus 254 that transmits and receives signals via two terminals 254a and 254b. In this embodiment,
35 terminal 254a carries non-inverted voltage signals while terminal 254b carries inverted voltage signals. Terminal 254a may be connected to a resistor R1 266 via a cable 255a. Terminal 254b may be connected to a resistor R2 267 via a cable 255b.

The resistors 262, 263 located on the B bus signal lines 215a and 215b of the first CPU card 210, and the resistors 266, 267 located on the B bus signal lines 255a, 255b of the second CPU card 250 may form an additional resistor network.

5 The signal line 255a may be connected to the signal line 215a at a node 292. Similarly, the signal line 255b may be connected to the signal line 215b at a node 293. The signal lines 215a and 215b may then be connected to another single contact 218 on an external connector 280. In some embodiments, contact 218 may be a coaxial contact. In alternate embodiments, each of the signal lines 215a, 215b
10 may be connected to individual non-coaxial contacts (not shown) on the single circular connector 280. In alternate embodiments, each of the signal lines 215a and 215b may be connected to a single external connector (not shown), which in some embodiments may be a coaxial connector. The connector 218/280 may then be connected via signal line 222 to another connector 226 on a mux coupler 234 that
15 forms part of a larger system, such as an avionics system. The mux coupler 234 may then be connected to, for example, an aircraft B bus 282b.

 In this embodiment of the system 200, a plurality of interconnected wires, which may include a non-inverted and an inverted signal line, resistor(s) and
20 transceiver pins/connectors, may be referred to as a single data channel. Each of the A busses and B busses of the CPU cards 210, 250 may therefore form two data channels. When the signals from the A bus 212 of the main CPU card 210, and the A bus 252 of the backup CPU card 250 are combined according to the teachings of the present embodiment of the system 200, both data channels may then be output
25 through contact 216 on signal line 220. Similarly, when the signals from the B bus 214 of the main CPU card 210, and the B bus 254 of the backup CPU card 250 are combined according to the teachings of the present embodiment of the system 200, both data channels may then be output through contact 218 on signal line 222. In some embodiments, the two data channels may each be provided as two data pins
30 on a single circular connector 280. It is understood that other types of multi-pin connectors may also be used.

 Each resistor network (one set of resistors 260/261/264/265 for bus A 212, 252 of each CPU card 210, 250, and another set of resistors 262/263/266/267 for
35 bus B 214, 254 of each CPU card 210, 250) may include thick film or other types of resistors having specially selected resistance values. The resistance values may be calculated based, for example, on empirical data, depending upon the number/type

and arrangement/type of external equipment connected to the aircraft bus. In some embodiments, the resistor value for all resistors 260-267 may be identical. In alternate embodiments, each resistor may have a different resistor value. In further alternate embodiments, each of the R1 resistors 260, 264 on data bus A 212, 252 of CPU cards 210, 250 respectively, may have identical values. Similarly, each of the R2 resistors 261, 265 on data bus A 212, 252 of CPU cards 210, 250 respectively, may also have identical values. The same may be true for the R1 and R2 resistors associated with the B busses 214, 254 of the CPU cards 210, 250 respectively. In some embodiments, the R1 and R2 resistor values associated with the A busses 212, 252 may be different from the R1 and R2 resistor values associated with the B busses 214, 254.

The resistors 260-267 step down the voltage at, for example, the A bus 252 of the backup CPU card 250 when the A bus 212 of the main CPU card is transmitting. This prevents overload of the CPU card that is not transmitting. In one embodiment, the step down voltage may be the maximum allowed by the MIL-STD-1553 standard of 20 Volts point to point. This may be accomplished using equal values for R1 and R2 of 18 ohms. The resistors 260-267 used in this embodiment of the system 200 may be implemented with very small components that have insignificant weight and space requirements compared to the mux couplers that they replace. Embodiments of the system 200 thus allow two channels to be combined on a single set of external connector pins or a single coaxial connector. This saves both weight and space compared to prior art system 100.

The interconnected signals between the channels are routed and combined on the monolithic backplane to the external connectors on the housing 202. This results in a smaller mechanical enclosure, as fewer transceiver pins are required. An alternate embodiment has the circular connectors mounted on an RFI (radio frequency interface) filter board that is connected to the backplane. In this embodiment, the interconnected signal may be routed and combined on the RFI filter board.

Figure 3 is a flow chart illustrating one method, designated generally as reference numeral 300, of combining a plurality of electrical signals using the system of Figure 2. The method 300 includes a first step of providing a first central processing unit (CPU) 210 located within a housing 202, as shown with reference numeral 302. The first CPU 210 may be capable of transmitting and receiving a first

signal on an A bus 212. The method 300 includes a next step of providing a second CPU 250 located within the housing 202, as shown with reference numeral 304. The second CPU 250 may be capable of transmitting and receiving a second signal on an A bus 252. The final step is providing a single coaxial connector 216 that transmits
5 and receives both said first signal and said second signal, as shown with reference numeral 306.

Additional optional steps for the method 300 may include providing a first resistor network electrically connected between each of the A busses 212, 252 and
10 the connector, such that the first resistor network assists in preventing an overload of one of the A busses 212, 252 when a signal is transmitted from the other of the A busses 252, 212 and output through the connector. Further optional steps for the method 300 may include performing similar steps with respect to the B busses 214, 254 of the first and second CPUs 210, 250, respectively.

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If an embodiment of the system 200 and method 300 is used in an aircraft following the MIL-STD-1553 standard, 2 channels, one channel from the main system 210 and one channel from the backup system 250, in a single housing, are able to communicate with external systems on the same aircraft bus 282a, 282b
20 using different bus operation modes. The system 200 and method 300 provide for a reduction in the number of transceiver pins or connectors, mux couplers and associated cabling. This system of interconnection is seamless and transparent to the other systems in an aircraft and does not result in any system degradation and disruption.

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It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the embodiments without departing from a spirit or scope of the invention as broadly described. The embodiments are, therefore, to be considered in all respects to be
30 illustrative and not restrictive.

CLAIMS

1. A system for combining a plurality of electrical signals, the system comprising:

a first central processing unit (CPU) located within a housing, the first
CPU capable of transmitting and receiving a first signal on an A bus; and
a second CPU located within the housing, the second CPU capable of
transmitting and receiving a second signal on an A bus;
wherein each of said first and second signals are combined on a
single connector.

2. The system of claim 1, further comprising a first resistor network electrically
connected between each of said A busses and said connector, such that said first
resistor network assists in preventing an overload of one of said A busses when a
signal is transmitted from the other of said A busses and output through said
connector.

3. The system of claim 2, wherein each bus further comprises a wire pair having
an inverted and non-inverted signal line, said first resistor network comprises a
resistor on each wire in said wire pairs and said inverted signal line uses a first pin of
said connector, while said non-inverted signal lines uses a second pin of said
connector.

4. The system of claim 3, wherein each of said resistors in said first resistor
network steps down a voltage at a receiving terminal associated with one of said
signals on said A bus to a maximum allowed by a standard for a receiving channel
when said other signal channel on said A bus is transmitting.

5. The system of claims 1 or 2, wherein;

each CPU further comprises a B bus comprising a wire pair having an
inverted and non-inverted signal line; and

said system further comprises a second resistor network electrically
connected to said B bus of each of said CPUs and having a resistor on each
wire in said wire pairs, and said inverted signal line uses a first pin of a
second connector, while said non-inverted signal line uses a second pin of
said second connector.

6. The system of claim 5, wherein each of said first and second CPUs are capable of performing identical functions.

7. The system claims 4 or 5, wherein said each of said inverted and non-inverted signal lines from each of said A and B busses terminates on a single pin of a single multi-pin connector.

8. The system of any one of the preceding claims, wherein each of said CPUs transmits and receives said signals according to a MIL-STD-1553 data standard.

9. A method for combining a plurality of electrical signals in a system, the method comprising the steps of:

providing a first central processing unit (CPU) located within a housing, the first CPU capable of transmitting and receiving a first signal on an A bus;

providing a second CPU located within the housing, the second CPU capable of transmitting and receiving a second signal on an A bus; and

providing a single connector that transmits and receives both said first signal and said second signal when combined on said connector.

10. The method of claim 9, further comprising providing a first resistor network electrically connected between each of said A busses and said connector, such that said first resistor network assists in preventing an overload of one of said A busses when a signal is transmitted from the other of said A busses and output through said connector.

11. The method of claim 9, wherein each bus further comprises a wire pair having an inverted and non-inverted signal line, said first resistor network comprises a resistor on each wire in said wire pairs and said inverted signal line uses a first pin of said connector, while said non-inverted signal line uses a second pin of said connector, the method further comprising the step of selecting a value for each resistor in said first resistor network such that each of said resistors steps down a voltage at a receiving terminal associated with one of said data channels to a maximum allowed by a standard for a receiving channel when said other data channel is transmitting.

12. The method of any one of claims 9-11, wherein each CPU further comprises a B bus comprising a wire pair having an inverted and non-inverted signal line; and a second resistor network electrically connected to said B bus of each of said CPUs and having a resistor on each wire in said wire pairs, and; and

5 the method further comprises electrically connecting said inverted signal line of each of said B busses to a first pin of a second connector, and electrically connecting said non-inverted signal line of each of said B busses to a second pin of said second connector.

10 13. The method of claim 12, further comprising electrically connecting each of said inverted and non-inverted signal lines from each of said A and B busses to a single pin of a single multi-pin connector.

14. The method of claims 12 or 13, wherein each of said first and second central
15 processing units are capable of performing identical functions.

15. The method of any one of claims 9-14, wherein each of said data channels conforms to a MIL-STD-1553 data standard.

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