[0004] Standalone ~~alone~~ uLED pixels or devices used for pick-and-place assemblies fall broadly into 2 categories: thin film flip-chip (TFFC) or vertical thin film (VTF), each with its specific advantages and applications, along with limitations associated with their typical designs. While a TFFC design typically offers a lower forward voltage, higher current drive capability and therefore higher brightness and efficiency performance, a VTF design offers easier dimensional down-scaling for smaller and higher density micro-LED designs.

[0005] Due to the numerous numbers of standalone ~~alone~~ micro-LED devices, it is a goal to make them reliably and ~~efficiency~~efficiently, and it is a goal that the micro-LED devices themselves are efficient. Making standalone ~~alone~~ micro-LED pixels efficiently facilitates utilizing their micron-sized spacing effectively for transmitting light. There is a further ongoing need to maximize light-emitting area while improving handling and processing of standalone micro-LEDs.

SUMMARY

[0006] Provided herein are light sources and methods of making them. A uLED having a thin film flip-chip (TFFC) design is advantageous in offering benefits of both thin film flip-chip (TFFC) and vertical thin film (VTF) architectures through a design that is dimensionally down-scalable while maximizing light-emitting area (LEA) of the epitaxy. The design also maximizes the light output extraction.

[0007] In an aspect, a micro-light emitting diode (uLED) device comprises: a mesa comprising: a plurality of semiconductor layers including an n-type layer, an active layer, and a p-type layer; a p-contact layer contacting the p-type layer; the mesa comprising a height spanning from a top surface of the p-contact layer to a bottom surface of the n-type layer and a width spanning a first sidewall of the n-type layer to a second sidewall of the n-type layer; the top surface of the p-contact layer having a different planar orientation compared to the first and second sidewalls of the n-type layer; a cathode contacting the first sidewall of the n-type layer; a first region of dielectric material that insulates the p-contact layer, the active layer, and a first sidewall of the p-type layer from the cathode; an anode contacting the top surface of the p-contact layer; and a second region of dielectric material that insulates the active layer, a second sidewall of the p-type layer, and the second sidewall of the n-type layer from the anode.

[0008] In another aspect, a display device comprises: a backplane; a plurality of individually-placed uLED devices attached to the backplane, each of the uLED devices

404p. A p-contact layer 405 contacts the p-type layer 404p. A cathode 419 contacts a first sidewall of the n-type layer 404n-s1. A first region of dielectric material 417a insulates the p-contact layer 404p, the active layer 406, and a first sidewall of the p-type layer 404p-s1 from the cathode 419. An anode 425 contacts the top surface of the p-contact layer 405t. A second region of dielectric material 417b insulates the active layer 406, a second sidewall of the p-type layer 404ps-2, and the second sidewall of the n-type layer 404n-s2 from the anode 425.

DISPLAY DEVICES

[00108] FIG. 6 schematically illustrates an exemplary display device utilizing uLED devices disclosed herein. In one or more embodiments, the display device is an LED illumination array and lens system. In one or more embodiments, the display device is an LED light emitting array. As shown in FIG. 6, display device 650 comprises a plurality or array of uLEDs 601 of varying colors, 600r for a red pixel, 600b for a blue pixel, and 600g for a green pixel. In one or more embodiments, each of the uLEDs is individually addressable and illuminable. It is understood that the number of each color and arrangement of the same will be application-specific. The plurality of pixels ~~are~~ is attached to a backplane 652. In one or more embodiments, an automatic pick-and-place device removes each uLED from a support (e.g., 303 of FIGS. 3A-3B), and mounts the uLED on the backplane, and welds the bonding surfaces of the uLED (e.g. first bonding surface 319-s1 of the cathode and second bonding surface 325-s1 of the anode), which may be conducted by any combination of thermal and/or ultrasonic and/or compressive methods, to the backplane. In one or more embodiments, there is a bonding metal pattern on the backplane to correspond to the bonding surfaces of the uLED. The plurality of pixels are enclosed in a housing ~~358~~658, which has a display face (or lens or other optical feature) 660. Electrodes 654 and 656 electrically connect the backplane 652 to a driver integrated circuit (not shown).

[00109] In one or more embodiments, arrays of micro-LEDs (μLEDs or uLEDs) are used. Micro-LEDs can support high density pixels having a lateral dimension less than 100 μm by 100 μm. In some embodiments, micro-LEDs with dimensions of about 50 μm in diameter or width and smaller can be used. Such micro-LEDs can be used for the manufacture of color displays by aligning in close proximity micro-LEDs comprising red, blue and green wavelengths.

~~What is claimed is:~~

CLAIMS

1. A method of manufacturing a micro-light emitting diode (uLED) device comprising:

depositing a plurality of semiconductor layers including an n-type layer, an active layer, and a p-type layer on a substrate;

depositing a p-contact layer on the plurality of semiconductor layers;

depositing a hard mask layer on the p-contact layer;

etching a portion of the semiconductor layers, the p-contact layer, and the hard mask layer to form trenches and plurality of mesas, each of the mesas having a height spanning from a top surface of the p-contact layer to a bottom surface of the n-type layer and a width spanning a first sidewall of the n-type layer to a second sidewall of the n-type layer;

depositing a dielectric metal over the substrate into the trenches and on an uppermost surface of the substrate;

first etching to expose the p-contact layer and a first portion of a surface of the substrate;

second etching to expose the n-type layer and a second portion of the surface of the substrate;

depositing a first metal onto areas exposed by the first etching and the second etching; and

etching to form a cathode and an anode which are isolated from each other;

the foregoing steps forming a processed structure.

2. The method of claim 1, wherein the width of the mesa is less than 100 micrometers.

3. The method of claim 1, wherein the height of the mesa is less than or equal to the width of the mesa.

4. The method of claim 1, wherein the first etching and/or the second etching independently comprise anisotropic etching.

5. The method of claim 1 comprising conducting a masking prior to the etching to expose the p-contact layer.

6. The method of claim 1, wherein two planar orientations of the p-contact layer are exposed during the etching to expose the p-contact layer.

7. The method of claim 1, wherein two planar orientations of the n-layer are exposed during the etching to expose the n-layer.

8. The method of claim 1 comprising conducting a masking prior to the etching to expose the n-type layer.

9. The method of claim 1 comprising forming a passivation layer on the processed structure.

10. The method of claim 1 comprising adhering bonding surfaces of the cathode and the anode to a support; removing the substrate; and singulating the mesas to form individual uLED devices.

11. The method of claim 1, wherein the n-type layer comprises N-GaN and the p-type layer comprises P-GaN.

12. The method of claim 1, wherein a first region of dielectric material insulates the p-contact layer, the active layer, and a first sidewall of the p-type layer from the cathode, and a second region of dielectric material insulates the active layer, a second sidewall of the p-type layer, and the second sidewall of the n-type layer from the anode; and the dielectric material of the first region and of the second region independently each comprise a material selected from the group consisting of SiO_2, AlO_x, and SiN, each independently has a thickness in a range of from 200 nm to 1 μm.

13. The method of claim 1, wherein the p-contact layer contacting the p-type layer substantially spans a width of the p-type layer.

14. The method of claim 1, wherein the p-type layer substantially spans a width of the active layer.

15. A method of making a display device comprising:

attaching plurality of micro light emitting diodes (uLEDs) to a backplane by a pick-and-place method; and

enclosing the plurality of ~~LEDs~~uLEDs in a housing with a display face;

each of the uLEDS comprising:

a mesa comprising:

a plurality of semiconductor layers including an n-type layer, an active layer, and a p-type layer;

a p-contact layer contacting the p-type layer;

the mesa comprising a height spanning from a top surface of the p-contact layer to a bottom surface of the n-type layer and a width spanning a first sidewall of the n-type layer to a second sidewall of the n-type layer; the top surface of the p-contact layer having a different planar orientation compared to the first and second sidewalls of the n-type layer;

a cathode contacting the first sidewall of the n-type layer;

a first region of dielectric material that insulates the p-contact layer, the active layer, and a first sidewall of the p-type layer from the cathode;

an anode contacting the top surface of the p-contact layer; and

a second region of dielectric material that insulates the active layer, a second sidewall of the p-type layer, and the second sidewall of the n-type layer from the anode.

16. The method of claim 15, wherein the width of the mesa is less than 100 micrometers.

17. The method of claim 15, wherein the height of the mesa is less than or equal to the width of the mesa.

18. The method of claim 15, wherein the p-contact layer contacting the p-type layer substantially spans a width of the p-type layer.

19. The method of claim 15, wherein the p-type layer substantially spans a width of the active layer.