

Method for the control and regulation of a combustion engine

The invention relates to a method for controlling and regulating a combustion engine in accordance with the preamble of claim 1 and an electronic regulating and control device for combustion engines in accordance with the preamble of claim 3.

When electronically regulating a diesel engine, a digital output signal is provided by a regulator. In dependence upon this signal, an electro-mechanical drive for the adjusting member should be adjusted for example by the fuel-injection pump or by pump nozzles. A pulse width modulator having downstream a low-pass filter is then used advantageously as a digital-analogue convertor. It must be taken into consideration here that the drive, by reason of its electrical (inductivity) and mechanical (mass) characteristics, demonstrates a more or less distinctive low-pass behaviour, than is required when dimensioning the low-pass filter. In any case if the control signal is insufficiently filtered, a mechanical disturbance of the adjusting member can occur, namely an oscillating movement with the pulse frequency of the control signal. The costs required for the low-pass filter, in particular with the lower timing frequencies, are regarded as a disadvantage.

The use of pulse width modulated signals for controlling the adjusting members for the quantity of fuel injected is, for example, evident in DE-A-33 11 351 and in this case the adjusting member is controlled directly by the pulse width modulated signal. The use of a pulse width modulated signal is also evident to the applicant from DE-A-37 30 443 but this signal is deployed here as a control input of a servo circuit for the adjusting member. The term "control signal for controlling an electric-mechanical adjusting member" is therefore to be understood in the sense that it similarly embraces a direct control, such as a control of a servo circuit for the adjusting member.

The document JP-A-59 120 776 (abstract) discloses a fuel pump control which is dependent on the rotational speed and which is achieved in such a way that a pulse sequence, which is dependent on the rotational speed, is fed to a monostable multi-vibrator, which forms from the pulse sequence a pulse which is dependent on the rotational speed and whose individual pulses are of constant duration. This pulse is fed to a fuel pump. When the rotational speed increases, the keying behaviour of the pulse increases accordingly and the fuel pump is fed in the centre with more electrical energy. Such a control is unsuitable for an actual regulation for example in the sense of the previously mentioned documents.

A pulse width modulator for converting a binary digital value to a pulse width modulated signal, which is achieved when using a microcomputer, can for example be taken from the company document "Embedded Controller Handbook", Intel, Order Number 21 09 18-005, 1987. In this case, a digital value is fed to a register, at whose output the value e.g. 8-bit (in the binary system) is present. A timing pulse frequency is fed to a counter input, whose output, which is also 8-bit here is compared in a comparator with the previously mentioned value. The output of the comparator, which checks for equality, is fed to the reset input of a flip-flop, whose set input receives the overflow signal of the counter. A pulse width modulator is then present at the Q output of the flip-flop. This signal has within each timing, a pulse, whose width or rather length increases with the increased size of the said value. With a numerical value of 0, the width of the pulse disappears, with a numerical value 255, the width corresponds almost to the period of time T_0 .

With this known solution, the relative amplitude of the voltage fluctuation, independent of the number of bits with a filter-time constant $\tau = T_0$ and with a keying ratio for the pulse within each timing of 1:1, amounts to almost 25%. With a keying ratio which is reducing or increasing in size, the

relative amplitude of the voltage fluctuations drops, however with a keying ratio of 1:5 or 5:1, it still amounts to approximately 10%. In order to reduce the relative voltage fluctuations, it is therefore necessary to select greater filter-time constants, which causes a corresponding deterioration of the dynamics, which has an extremely unfavourable effect on the driving behaviour of the vehicle.

It should be noted here, that the terms "Dualcode" and "Binärcode" (binary code) are used in accordance with literature in the German language (e.g. U. Tietze, Ch. Schenk: "Halbleiterschaltungstechnik" (Technology in semiconductor circuitry) Springer Publishers, Berlin 1983).

The object of the invention is, instead of the previously normal pulse width modulation, to convert the output signal of the computer into a control signal for an electro-mechanical adjusting member, which with the same costs, in particular also with regard to the filtering, has considerably less relative voltage fluctuations of the analogue signal. This object is achieved by means of a method according to the characterising feature of claim 1 or rather by means of a device according to the characterising feature of claim 3.

The invention offers the advantage that, with the same circuitry costs such as in accordance with the state of the art, the undulation of the output signal is significantly reduced. With the same requirements of the residual undulation, it is possible to maintain considerably lower costs for a downstream low-pass filter, than in accordance with the state of the art. The term "downstream low-pass filter", embraces here also a load with a low-pass character, which was already mentioned previously.

Further features are characterised in the dependent subordinate claims.

The invention together with further advantages is explained further in the following by way of examples, which are illustrated in the drawing, in which Fig. 1 is block diagram of an example of a device in accordance with the invention, Fig. 2 is a further example of a device in accordance with the invention and Fig. 3a and b are, in the time graphs within a timing pulse, the forms of the output signal dependent upon the preceding signal with a device in accordance with the state of the art (Fig. 3a) and with a device in accordance with the invention (Fig. 3b).

Fig. 1 is a schematic illustration of a diesel engine 1 having a fuel-injection pump 2, whose control rod 3, which determines the quantity of fuel supplied, can be adjusted by means of an electro-mechanical drive 4. An output signal b, which represents the basis for the adjustment of the control rod 3, is calculated by a computer 5 from the signals of the operating values of the engine 1 and also of the vehicle.

Operating values which are essential as input values for the computer 5 are the driving pedal position, which produces a corresponding signal f by way of a sensor 7 and the rotational speed of the engine 1, wherein a rotational speed signal n is supplied to the computer 5 by a rotational speed sensor 8. In Fig. 1, still further sensors 9 are illustrated schematically, these sensors can provide additional operating value signals, e.g. with regard to engine temperature, air pressure, fuel temperature etc.

The output signal b of the computer 5 and the relevant other output signals b'b" are present in a digital, binary coded form and are fed to a register 10, from where it arrives as an 8-bit word B at the input B_0 to B_7 of an 8 bit comparator 11. Such a comparator can for example be realised with logic modules MM54C85, 4-bit magnitude comparator by National Semiconductor. The company document "Logic Databook", Volume 1, National Semiconductor Corporation", 1984 illustrates the logic construction of such modules and describes how they are

connected together to form word lengths, which are greater than 4-bit.

With further reference to Fig. 1, it should be said that the output signal b and the word B are fed, accurate to one bit value, to the comparator 11, i.e. the output with the lowest bit value (LSB = least significant bit) of the Register, is connected with the input B_0 of the comparator 11.

Furthermore, a binary counter 12 is provided, to which counter timing pulses f_1 each of the period of time T_1 are fed. These counter timing pulses originate expediently from a timing pulse generator (not further illustrated) which is required by the computer 5. An 8-bit output of the counter 12 is connected to the second input of the comparator 11, however the counter output is connected here to the comparator input in such a way that the output MSB (most significant bit) of the counter 12 corresponds to the input A_0 of the comparator 11 with the lowest bit value (LSB), i.e. the sequence of the bits is reversed when wiring up, or, in other words, the counter signal a is fed to the comparator 11 in a reverse form.

At the output of the comparator 11, which checks whether the word A at the inputs A_0 to A_7 is smaller than the word B at the inputs B_0 to B_7 , there occurs a control signal of the time period T_0 , which comprises within each time period individual pulses, whose total length within each time period T_0 is proportional to the value of the output signal b of the computer 5. This is illustrated for a 4-bit comparator in Fig. 3b, and the previously normal pulse width modulation is compared in Fig. 3a. The preceding value B is characterised on the left by the numbers 0 to 15.

Periods of time T_0 containing the counter timing pulses each of duration T_1 are related to each other by way of the word length n of the comparator by way of $T_0 = T_1 \cdot 2^n$. The word length in Fig. 1 is represented by 8-bit and in Fig. 3 by 4-

bit. In practice, however, word lengths of 8 to 16 bit or more are used.

A D-flip-flop 13 can be connected downstream of the output of the comparator 11. This D-flip-flop 13 is pulse edge controlled by the counter timing pulses f_1 and releases the control signal from the switch spike, which occurs in the comparator 11. An inverter is in so doing connected in advance of the timing input of the flip-flop 13. It is advisable to remove the switch spike, above all with the higher timing frequencies, if the running times in the comparator cause spikes of significantly noticeable lengths, which could cause a falsification of the preceding signal.

The control signal s is fed to the electro-mechanical drive 4 by way of a simple low-pass filter 14 and an output stage 15.

Fig. 2 illustrates an example of a 4-bit comparator which is realised when using traditional gate modules and Fig. 3b as previously mentioned, illustrates the associated control signal for the 16 possible preceding values. In Fig. 3b, the significant improvement in the voltage undulation obtained after filtering is already obviously evident to the person skilled in the art. Naturally, this improvement is demonstrated both mathematically and experimentally and is indicated in the following by way of a comparison for the respective unfavourable case of the keying ratio (e.g. number 8 in Fig. 3a).

With a pulse width modulator in accordance with the state of the art, the relative voltage fluctuations with a filter-time constant $\tau = T_0$ amounts to approximately 25% and in fact is dependent of the number of bits used.

With the invention, these voltage fluctuations with the same filter time constants are:

4-bit below 12%
10-bit below 0.2%
16-bit below $40 \cdot 10^{-6}$

It can be seen from this, that the costs for filtering when using the invention are drastically reduced. With regard to the already mentioned low-pass characteristic inherent in the electro-mechanical adjusting member, a low-pass filter can in many cases be completely omitted.

Adjusting members, which should be controlled based on the output signal b of the computer 5, are in particular the control rod of a fuel-injection pump, as illustrated in Fig. 1. The adjusting members can, however, also be used to adjust the point of time of fuel injection, the quantity of air, an exhaust-gas recirculation valve, a throttle valve and the like, which is indicated by the signals $b'b''$ in Fig. 1.

A particular advantage associated with the invention can be seen in the rapid and error-free reaction to a change in the preceding value, which is not only provided by means of favourably dimensioning the filter. If in fact the preceding value B is changed within the period of time T_0 to a particularly smaller value, then, with a construction in accordance with the invention, a reaction in the desired direction occurs in almost all cases prior to completing the same time period. With designs in accordance with the state of the art, when changing the preceding value during the course of the period of time, in the most unfavourable case, either so-called freak values (once-through output of 100%) occur, or the desired change only occurs during the course of the next period of time T_0 . Such a malfunction can have fatal consequences for the driving operation of the motor vehicle.

If the subject matter of the present application is that the total duration of the control signal s is substantially proportional to the value of the binary output signal b , then

this should not mean that an offset is excluded.



Claims

1. Method for controlling and regulating an internal combustion engine, where a digital, binary output signal is calculated in a computer in dependence upon the signals of the operating values, such as for example the rotational speed, the accelerator pedal position, the engine temperature etc. and this calculated binary signal is converted into a control signal, which comprises pulses of constant level, and the total duration of the control signal within a predetermined fixed timing period is proportional to the value of the binary signal and this control signal is used to control an electro-magnetic adjusting member, characterised in that the control signal within each timing period is, depending on the value of the binary signal (b), divided into individual pulses, and the summation of the duration of the individual pulses within the timing period is proportional to the value of the binary signal (b) and the individual pulses are divided substantially evenly within each timing period.
2. Method according to claim 1, characterised in that the calculated binary signal (b) is represented as an n-bit preceding binary signal, the timing pulses for producing the durations of the individual pulses are counted binary, in order to provide an n-bit binary counter signal (a), which is compared using a comparator with the preceding binary signal and $n > 1$ [apparent omission in German text] for the purpose of comparison, the binary counter signal (a) is fed to the comparator in a reverse sequence according to its binary bits and a comparison is carried out as to whether the numerical value, according to the reverse sequence of the binary bits, of the binary counter signal is smaller than the numerical value of the preceding binary signal.
3. Electronic regulating and controlling device for internal combustion engines for carrying out the method in accordance with one of claims 1 to 2, having a computer 5, to which is fed the rotational speed signal (n) of a rotational

speed sensor (8) and further signals of operating values determined by means of sensors and, for the purpose of outputting an n-bit preceding binary signal (b) calculated from the operating values, the computer (5) is fitted with an n-bit binary counter which is fed a timing signal (f1) for the purpose of forming an n-bit binary counter signal (a) and is also fitted with an n-bit comparator (11) which, for the purpose of comparing the binary counter signal (a) is fed with the n-bit preceding binary signal (b) and whose output signal (s) is used for controlling an electro-mechanical adjusting member (4), and $n >$ [apparent omission in German text] characterised in that the binary counter signal (a) and the preceding binary signal (b) are fed to the comparator (11) in such a way that the binary counter signal (a) with respect to the comparator input (b) is used in the reverse sequence according to its binary bits.

4. Device according to claim 3, characterised in that the comparator (11) is fitted, for the purpose of outputting an output signal, should the respective value of the pre-set binary signal (b) be larger than the corresponding value of the binary counter signal (a), which is used in the reverse sequence according to its binary places.

5. Device according to claim 3 or 4, characterised in that, a pulse edge controlled D-flip-flop (13) is connected downstream of the comparator (11).

