TITLE OF THE INVENTION

Semiconductor device and manufacturing method thereof

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001]

The present invention relates to a semiconductor device and a method of manufacturing the semiconductor device.

2. Description of the Background Art

[0002]

In semiconductor integrated circuits, particularly an integrated circuit using a MOS transistor, the degree of integration has become increasingly higher. Along with such a high degree of integration, miniaturization of a MOS transistor for highly integrated circuits has been progressed into a nano region. The progress in miniaturization of the MOS transistor involves problems about difficulty in suppressing a leakage current and restriction on reduction in circuit occupancy area due to a need for ensuring a required current amount. With a view to solving this problem, there has been proposed a surrounding gate transistor (SGT) having a structure where a source, a gate and a drain are vertically arranged relative to a substrate, and the gate is formed to surround a columnar (pillar-shaped) semiconductor layer (see, for example, the following Patent Documents 1 to 3).

[0003]

[Patent Document 1] JP 02-071556A

[Patent Document 2] JP 02-188966A

[Patent Document 3] JP 02-145761A

[0004]

In the SGT, a channel region is formed to surround a lateral surface of the columnar semiconductor, so that a large gate width is achieved within a small occupancy area. This means that it is required to allow a large ON-current to pass through the small occupancy

area. In this case, if resistances of the source and drain are high, the large ON-current will cause difficulty in applying a desired voltage to the source and drain. Therefore, there is a need for an SGT manufacturing method (including a design technique) for reducing the resistances of the source and drain. The large ON-current also gives rise to a need for reducing resistances of contacts.

[0005]

In a conventional MOS transistor, a gate electrode is formed by depositing a gate material, transferring a gate pattern to a resist on a substrate through lithography to form a mask, and etching the gate material using the mask. That is, in the conventional MOS transistor, a gate length is designed based on the gate pattern. In contrast, in the SGT, the lateral surface of the columnar semiconductor serves as a channel region, and thereby a current flows vertically relative to the substrate. That is, in the SGT, a gate length is designed based on a manufacturing method, instead of based on a gate pattern, so that the gate length and a variation in the gate length are determined by the manufacturing method.

[0006]

In the SGT, it is required to reduce a diameter of the columnar semiconductor in order to suppress an increase in leakage current along with the miniaturization. In addition, it is necessary to establish a manufacturing method capable of optimizing the source and drain to restrain a short channel effect so as to suppress a leakage current.

[0007]

Further, in the SGT, it is necessary to reduce a parasitic capacitance in order to minimize power consumption. Thus, there is a need for a manufacturing method capable of reducing a parasitic capacitance.

[0008]

As with the conventional MOS transistor, the SGT has a need for reducing a manufacturing cost thereof. For this purpose, it is necessary to reduce the number of steps in a manufacturing process.

SUMMARY OF THE INVENTION

[0009]

It is therefore an object of the present invention to provide an SGT manufacturing method capable of obtaining a structure for reducing resistances of a source and a drain, a structure for reducing a parasitic capacitance, a desired gate length, desired configurations of the source and drain, and a desired diameter of a columnar semiconductor.

[0010]

In order to achieve this object, according to a first aspect of the present invention, there is provided a method of manufacturing a semiconductor device, which comprises the steps of: forming a first columnar semiconductor layer on a substrate, and forming a first flat semiconductor layer in an upper portion of the substrate lying under the first columnar semiconductor layer; forming a first semiconductor layer of a second conductive type in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; forming a first insulating film around a lower sidewall of the first columnar silicon layer and above the first flat semiconductor layer; forming a gate insulating film and a gate electrode around the first columnar silicon layer; forming a sidewall-shaped second insulating film to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode and the first insulating film; forming a second semiconductor layer of the second conductive type in an upper portion of the first columnar silicon layer, and forming a semiconductor layer of a first conductive type between the first semiconductor layer of the second conductive type and the second semiconductor layer of the second conductive type; and forming a metal-semiconductor compound on each of an upper surface of the first semiconductor layer of the second conductive type and an upper surface of the second semiconductor layer of the second conductive type, wherein the first insulating film has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer.

[0011]

Preferably, in the method of the present invention, a length between a central axis of the first columnar silicon layer and an edge of the first columnar silicon layer is larger than a sum of a length between the central axis of the first columnar silicon layer and a sidewall of the first columnar silicon layer, the thickness of the gate insulating film, a thickness of

the gate electrode, and a thickness of the sidewall-shaped second insulating film formed to surround the sidewall of the gate electrode and the first insulating film.

[0012]

Preferably, in the method of the present invention, the gate electrode has a thickness larger than that of the sidewall-shaped second insulating film formed to surround the upper sidewall of the first columnar silicon layer while contacting the upper surface of the gate electrode.

[0013]

In the method of the present invention, it is preferable that the first flat semiconductor layer being a first flat silicon layer, the first columnar semiconductor layer being a first columnar silicon layer, the semiconductor layer of the first conductive type being a silicon layer of the first conductive type, the first semiconductor layer of the second conductive type being a first silicon layer of the second conductive type, and the second semiconductor layer of the second conductive type being a second silicon layer of the second conductive type.

[0014]

In the above method, the semiconductor layer of the first conductive type may be a p-type silicon layer or a non-doped silicon layer. Further, the first semiconductor layer of the second conductive type may be an n-type silicon layer, and the second semiconductor layer of the second conductive type may be an n-type silicon layer.

[0015]

Alternatively, the semiconductor layer of the first conductive type may be an n-type silicon layer or a non-doped silicon layer. Further, the first semiconductor layer of the second conductive type may be a p-type silicon layer, and the second semiconductor layer of the second conductive type may be a p-type silicon layer.

[0016]

Preferably, the above method includes the steps of: forming a pad oxide film on the silicon substrate; forming on the pad oxide film a first nitride film for use as a mask during the formation of the first columnar silicon layer; forming a first amorphous silicon or polysilicon film on the first nitride film; applying a resist onto the first amorphous silicon

or polysilicon film, and transferring a first columnar layer pattern to the resist through lithography to leave a first resist corresponding to the first columnar layer pattern; and etching the first amorphous silicon or polysilicon film and the first nitride film in turn to form a first hard mask.

[0017]

Preferably, the above method includes the step of forming the first columnar semiconductor layer by a dry etching process using the first hard mask.

[0018]

Preferably, in the above method, the first amorphous silicon or polysilicon film serving as the first hard mask is fully etched during the dry etching process to cause a change in plasma emission intensity detectable by a dry etching apparatus, wherein the step of forming the first columnar semiconductor layer includes detecting the change in the plasma emission intensity, and determining a termination timing of the dry etching process based on the detection result to control a height dimension of the first columnar silicon layer.

[0019]

Preferably, in the above method, a height dimension of the first amorphous silicon or polysilicon film before the dry etching process is less than that of the first columnar silicon layer.

[0020]

Preferably, the above method includes the step of sacrificially oxidizing a surface of the first columnar silicon layer fabricated on the substrate so as to reduce irregularities of a sidewall of the first columnar silicon layer for use as a channel region while removing a surface portion of the first columnar silicon layer having carbon implanted thereinto during the dry etching process, and protect the first columnar silicon layer from contaminations including a by-product to be produced during a subsequent dry etching process.

[0021]

Preferably, the above method includes the steps of: applying a resist onto the substrate having the first columnar silicon layer, and transferring a first flat silicon layer pattern to the resist through lithography to leave a second resist corresponding to the first flat silicon

layer pattern; and etching the silicon substrate to form the first flat silicon layer, and removing the second resist.

[0022]

Preferably, the above method includes the steps of: depositing a filling oxide film on the first flat silicon layer and substrate having the first columnar silicon layer; flattening the filling oxide film; and etching the filling oxide film in such a manner as to allow a surface of an upper portion of the first flat silicon layer to be exposed.

[0023]

Preferably, the above method includes the step of: the offset spacer formation on the sidewall of the first columnar silicon layer.

[0024]

Preferably, in the above method, the first silicon layer of the second conductive type is formed in the lower portion of the first columnar semiconductor layer and the entirety or the upper portion of the first flat semiconductor layer by introducing an impurity of the second conductive type into the first flat semiconductor layer having the first columnar silicon layer with a offset spacer through an impurity introduction process comprising an impurity injection process. And then, the offset spacer is etched.

[0025]

Preferably, in the above method, the first silicon layer of the second conductive type is formed in the lower portion of the first columnar semiconductor layer without injecting any impurity into the upper portion of the first columnar silicon layer.

[0026]

Preferably, the above method includes the steps of: depositing a first insulating film material above and around the first columnar silicon layer fabricated on the first flat silicon layer, in such a manner that the first insulating film material deposited above the first columnar silicon layer and around the lower sidewall of the first columnar silicon layer has a thickness larger than that of the first insulating film material deposited around an intermediate/upper sidewall of the first columnar silicon layer; and etching the first insulating film material around the intermediate/upper sidewall of the first columnar silicon layer to form the first insulating film above the first columnar silicon layer and

around the lower sidewall of the first columnar silicon layer, in such a manner as to have a thickness larger than that of the gate insulating film to be formed around the first columnar silicon layer.

[0027]

Preferably, in the above method, the gate insulating film is formed on the sidewall of the first columnar silicon layer with a first hard mask of nitride film fabricated on the first flat silicon layer, wherein the method includes the steps of: forming a second amorphous silicon or polysilicon film serving as a gate electrode material, on an in-process structure obtained by the step of forming the gate insulating film, in such a manner as to allow the first columnar silicon layer to be embedded therein; and polishing the second amorphous silicon or polysilicon film by a chemical mechanical polishing process to have a flattened upper surface, wherein the nitride film serving as the first hard mask is used as a stopper against the chemical mechanical polishing process to control a polishing amount with enhanced reproducibility.

[0028]

Preferably, the above method includes the steps of: etching back the second amorphous silicon or polysilicon film serving as the gate electrode material, to allow the gate electrode to be formed with a desired gate length; and depositing a first oxide film on an in-process structure obtained by the step of etching back the second amorphous silicon or polysilicon film, whereby the first oxide film can protect an upper surface of the gate electrode from a wet etching or dry etching process to be performed in a subsequent step, so as to suppress a change or variation in the gate length and damage of the gate insulating film from the upper surface of the gate electrode.

[0029]

Preferably, the above method includes the steps of: forming a second nitride film on the first oxide film; etching back the second nitride film to form a third insulating film sidewall, and etching the first oxide film; applying a bottom anti-reflective coating (BARC) layer onto an in-process structure obtained by the step of etching back the second nitride film, applying a resist onto the BARC layer, and transferring a gate wiring pattern to the resist through lithography to leave a third resist corresponding to the gate wiring

pattern; etching the BARC layer, and the second amorphous silicon or polysilicon film serving as the gate electrode material, using the third resist as a mask, to form a gate electrode body and a gate wiring which make up the gate electrode; partly removing the first insulating film by a dry etching or wet etching to allow the surface of the first semiconductor layer of the second conductive type lying under the first columnar silicon layer to be exposed; the removing the resist and the BARC; forming the fourth oxide layer on an exposed surface of the gate electrode and the surfaces of the first semiconductor layer of the second conductive type lying under the first columnar silicon layer; removing the first nitride film above the first columnar silicon layer and the second nitride film around the first columnar silicon layer by an etching process; and removing the pad oxide film, and the first oxide film and the fourth oxide layer.

[0030]

Preferably, the above method includes the steps of: forming a third nitride film on the first columnar silicon layer fabricated on the first flat silicon layer, the gate electrode surrounding the first columnar silicon layer, etching back the third nitride film in such a manner that the respective upper surfaces of the first semiconductor layer of the second conductive type lying under the first columnar silicon layer, and the upper portion of the first columnar silicon layer, are exposed, and forming a second insulating film sidewall serving as the sidewall-shaped second insulating film, to surround the upper sidewall of the first columnar silicon layer while contacting the upper surface of the gate electrode and to surround the sidewall of the gate electrode; introducing an impurity of the second conductive type into the upper portion of the first columnar silicon layer through an impurity introduction process comprising an impurity injection process, to form the second silicon layer of the second conductive type in the upper portion of the first columnar silicon layer, and form the silicon layer of the first conductive type between the first silicon layer of the second conductive type and the second silicon layer of the second conductive type; and forming a first metal film such as a nickel (Ni) film or a cobalt (Co) film, on the respective exposed surface of the first silicon layer of the second conductive type and the gate electrode, and an upper surface of the second silicon of the second conductive type, by a sputtering process, subjecting the first metal film to a heat treatment, and removing an

unreacted part of the heat-treated film, to form a metal-semiconductor compound on each of the first silicon layer of the second conductive type and the second silicon layer of the second conductive type.

[0031]

Preferably, the above method includes the steps of: forming a contact stopper such as a nitride film, on the first columnar silicon layer fabricated on the first flat silicon layer, the gate electrode surrounding the first columnar silicon layer; forming a third oxide film serving as an interlayer insulating film, on the contact stopper, and flattening the third oxide film by a chemical mechanical polishing process; forming a contact hole in the third oxide film at position on the upper side of the second silicon layer of the second conductive type formed in the upper portion of the first columnar silicon layer, by an etching process; forming contact holes in the third oxide film at positions on respective upper sides of the first silicon layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar silicon layer, and the gate electrode, by an etching process; etching the portion of the contact stopper corresponding to the respective contact holes.

[0032]

According to a second aspect of the present invention, there is provided a semiconductor device which comprises: a first flat semiconductor layer formed on a substrate; a first columnar semiconductor layer formed on the first flat semiconductor layer; a first semiconductor layer of a second conductive type formed in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; a second semiconductor layer of the second conductive type formed in an upper portion of the first columnar silicon layer; a semiconductor layer of a first conductive type formed between the first semiconductor layer of the second conductive type formed in the lower portion of the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar silicon layer; a gate insulating film and a gate electrode which are formed around the first columnar silicon layer; a first insulating film formed between the gate electrode and the first flat semiconductor layer; a sidewall-shaped second insulating film formed to

surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode and the first insulating film; a metal-semiconductor compound formed on each of an upper surface of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer, and an upper surface of the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, wherein the first insulating film formed between the gate electrode and the first flat semiconductor layer has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer.

[0033]

According to a third aspect of the present invention, there is provided a semiconductor device which comprises: a first flat semiconductor layer formed on a substrate; a first columnar semiconductor layer formed on the first flat semiconductor layer; a first semiconductor layer of a second conductive type formed in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; a second semiconductor layer of the second conductive type formed in an upper portion of the first columnar silicon layer; a semiconductor layer of a first conductive type formed between the first semiconductor layer of the second conductive type formed in the lower portion of the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar silicon layer; a gate insulating film and a gate electrode which are formed around the first columnar silicon layer; a first insulating film formed between the gate electrode and the first flat semiconductor layer; a sidewall-shaped second insulating film formed to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode and the first insulating film; a metal-semiconductor compound formed on each of an upper surface of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer, and an upper surface of the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, wherein: the first insulating film formed between the gate

electrode and the first flat semiconductor layer has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer; and a length between a central axis of the first columnar silicon layer and an edge of the first columnar silicon layer is larger than a sum of a length between the central axis of the first columnar silicon layer and a sidewall of the first columnar silicon layer, the thickness of the gate insulating film, a thickness of the gate electrode, and a thickness of the sidewall-shaped second insulating film formed to surround the sidewall of the gate electrode and the first insulating film.

[0034]

According to a fourth aspect of the present invention, there is provided a semiconductor device which comprises: a first flat semiconductor layer formed on a substrate; a first columnar semiconductor layer formed on the first flat semiconductor layer; a first semiconductor layer of a second conductive type formed in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; a second semiconductor layer of the second conductive type formed in an upper portion of the first columnar silicon layer; a semiconductor layer of a first conductive type formed between the first semiconductor layer of the second conductive type formed in the lower portion of the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar silicon layer; a gate insulating film and a gate electrode which are formed around the first columnar silicon layer; a first insulating film formed between the gate electrode and the first flat semiconductor layer; a sidewall-shaped second insulating film formed to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode; a metal-semiconductor compound formed on each of an upper surface of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer, and an upper surface of the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, wherein: the first insulating film formed between the gate electrode and the first flat semiconductor layer has a thickness larger than that of the gate

insulating film formed around the first columnar silicon layer; and the gate electrode has a thickness larger than that of the sidewall-shaped second insulating film formed to surround the upper sidewall of the first columnar silicon layer while contacting the upper surface of the gate electrode.

[0035]

As above, the method according to the first aspect of the present invention, comprises the steps of: forming a first columnar semiconductor layer on a substrate, and forming a first flat semiconductor layer in an upper portion of the substrate lying under the first columnar semiconductor layer; forming a first semiconductor layer of a second conductive type in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; forming a first insulating film around a lower sidewall of the first columnar silicon layer and above the first flat semiconductor layer; forming a gate insulating film and a gate electrode around the first columnar silicon layer; forming a sidewall-shaped second insulating film to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode and the first insulating film; forming a second semiconductor layer of the second conductive type in an upper portion of the first columnar silicon layer, and forming a semiconductor layer of a first conductive type between the first semiconductor layer of the second conductive type and the second semiconductor layer of the second conductive type; and forming a metal-semiconductor compound on each of an upper surface of the first semiconductor layer of the second conductive type and an upper surface of the second semiconductor layer of the second conductive type, wherein the first insulating film has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer.

[0036]

The above feature of the present invention makes it possible to provide an SGT manufacturing method capable of obtaining a structure for reducing resistances of a source and a drain, a structure for reducing a parasitic capacitance, a desired gate length, desired configurations of the source and drain, and a desired diameter of a columnar semiconductor.

[0037]

In the method according to one preferred embodiment of the present invention, a length between a central axis of the first columnar silicon layer and an edge of the first columnar silicon layer is larger than a sum of a length between the central axis of the first columnar silicon layer and a sidewall of the first columnar silicon layer, the thickness of the gate insulating film, a thickness of the gate electrode, and a thickness of the sidewall-shaped second insulating film formed to surround the sidewall of the gate electrode and the first insulating film. This feature makes it possible to adequately form a metal-semiconductor compound on the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar semiconductor layer, so as to reduce a resistance of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar semiconductor layer.

[0038]

In the method according to one preferred embodiment of the present invention, the gate electrode has a thickness larger than that of the sidewall-shaped second insulating film formed to surround the upper sidewall of the first columnar silicon layer while contacting the upper surface of the gate electrode. This feature makes it possible to adequately form a metal-semiconductor compound on the gate electrode, according to need, so as to reduce a resistance of the gate electrode.

[0039]

The method according to one preferred embodiment of the present invention includes the steps of: forming a pad oxide film on the silicon substrate; forming on the pad oxide film a first nitride film for use as a mask during the formation of the first columnar silicon layer; forming a first amorphous silicon or polysilicon film on the first nitride film; applying a resist onto the first amorphous silicon or polysilicon film, and transferring a first columnar layer pattern to the resist through lithography to leave a first resist corresponding to the first columnar layer pattern; and etching the first amorphous silicon or polysilicon film and the first nitride film in turn to form a first hard mask. This feature

makes it possible to control a height of the first columnar silicon layer according to determination of a termination timing of a dry etching process in the subsequent step.

[0040]

The method according to one preferred embodiment of the present invention includes the step of forming the first columnar semiconductor layer by a dry etching process using the first hard mask. During this dry etching process, the first amorphous silicon or polysilicon film serving as the first hard mask is fully etched to cause a change in plasma emission intensity detectable by a dry etching apparatus. Thus, the change in the plasma emission intensity can be detected to determine a termination timing of the dry etching process based on the detection result to control a height dimension of the first columnar silicon layer.

[0041]

In the method according to one preferred embodiment of the present invention, a height dimension of the first amorphous silicon or polysilicon film before the dry etching process is less than that of the first columnar silicon layer. This feature makes it possible to adequately determine the termination timing of the dry etching process.

[0042]

The method according to one preferred embodiment of the present invention includes the step of sacrificially oxidizing a surface of the first columnar silicon layer fabricated on the substrate. This feature makes it possible to reduce irregularities of a sidewall of the first columnar silicon layer for use as a channel region while removing a surface portion of the first columnar silicon layer having carbon implanted thereinto during the dry etching process, and protect the first columnar silicon layer from contaminations including a by-product to be produced during a subsequent dry etching process.

[0043]

The method according to one preferred embodiment of the present invention includes the steps of: applying a resist onto the substrate having the first columnar silicon layer, and transferring a first flat silicon layer pattern to the resist through lithography to leave a second resist corresponding to the first flat silicon layer pattern; and etching the silicon substrate to form the first flat silicon layer, and removing the second resist. This feature

makes it possible to adequately achieve an interelement isolation.

[0044]

The method according to one preferred embodiment of the present invention includes the steps of: depositing a filling oxide film on the first flat silicon layer and substrate having the first columnar silicon layer; flattening the filling oxide film; and etching the filling oxide film in such a manner as to allow a surface of an upper portion of the first flat silicon layer to be exposed. This feature makes it possible to adequately achieve an interelement isolation.

[0045]

The method according to one preferred embodiment of the present invention includes the step of: the offset spacer formation on the sidewall of the first columnar silicon layer. This feature makes it possible to prevent an impurity from being implanted from the sidewall of the first columnar silicon layer during an impurity injection process.

[0046]

In the method according to one preferred embodiment of the present invention, the first silicon layer of the second conductive type is formed in the lower portion of the first columnar semiconductor layer and the entirety or the upper portion of the first flat semiconductor layer by introducing an impurity of the second conductive type into the first flat semiconductor layer having the first columnar silicon layer with a offset spacer through an impurity introduction process comprising an impurity injection process. And then, the offset spacer is etched. This feature makes it possible to efficiently form the first silicon layer of the second conductive type.

[0047]

In the method according to one preferred embodiment of the present invention, the first silicon layer of the second conductive type is formed in the lower portion of the first columnar semiconductor layer without injecting any impurity into the upper portion of the first columnar silicon layer. This feature makes it possible to easily optimize conditions of respective impurity injection processes for the upper portion of the first columnar silicon layer and the first flat silicon layer lying the first columnar silicon layer, to restrain a short channel effect so as to reduce a leakage current.

[0048]

The method according to one preferred embodiment of the present invention includes the steps of: depositing a first insulating film material above and around the first columnar silicon layer fabricated on the first flat silicon layer, in such a manner that the first insulating film material deposited above the first columnar silicon layer and around the lower sidewall of the first columnar silicon layer has a thickness larger than that of the first insulating film material deposited around an intermediate/upper sidewall of the first columnar silicon layer; and etching the first insulating film material around the intermediate/upper sidewall of the first columnar silicon layer to form the first insulating film above the first columnar silicon layer and around the lower sidewall of the first columnar silicon layer, in such a manner as to have a thickness larger than that of the gate insulating film to be formed around the first columnar silicon layer. This feature makes it possible to reduce a gate-source parasitic capacitance.

[0049]

In the method according to one preferred embodiment of the present invention, the gate insulating film is formed on the sidewall of the first columnar silicon layer with a first hard mask of nitride film fabricated on the first flat silicon layer, wherein the method includes the steps of: forming a second amorphous silicon or polysilicon film serving as a gate electrode material, on an in-process structure obtained by the step of forming the gate insulating film, in such a manner as to allow the first columnar silicon layer to be embedded therein; and polishing the second amorphous silicon or polysilicon film by a chemical mechanical polishing process to have a flattened upper surface. According to this feature, the nitride film serving as the first hard mask can be used as a stopper against the chemical mechanical polishing process to control a polishing amount with enhanced reproducibility.

[0050]

The method according to one preferred embodiment of the present invention includes the steps of: etching back the second amorphous silicon or polysilicon film serving as the gate electrode material, to allow the gate electrode to be formed with a desired gate length; and depositing a first oxide film on an in-process structure obtained by the step of etching

back the second amorphous silicon or polysilicon film. According to this feature, the first oxide film can protect an upper surface of the gate electrode from a wet etching or dry etching process to be performed in a subsequent step, so as to suppress a change or variation in the gate length and damage of the gate insulating film from the upper surface of the gate electrode.

[0051]

The method according to one preferred embodiment of the present invention includes the steps of: forming a second nitride film on the first oxide film; etching back the second nitride film to form a third insulating film sidewall, and etching the first oxide film; applying a bottom anti-reflective coating (BARC) layer onto an in-process structure obtained by the step of etching back the second nitride film, applying a resist onto the BARC layer, and transferring a gate wiring pattern to the resist through lithography to leave a third resist corresponding to the gate wiring pattern; etching the BARC layer, and the second amorphous silicon or polysilicon film serving as the gate electrode material, using the third resist as a mask, to form a gate electrode body and a gate wiring which make up the gate electrode; partly removing the first insulating film by a dry etching or wet etching to allow the surface of the first semiconductor layer of the second conductive type lying under the first columnar silicon layer to be exposed; the removing the resist and the BARC; forming the fourth oxide layer on an exposed surface of the gate electrode and the surfaces of the first semiconductor layer of the second conductive type lying under the first columnar silicon layer; removing the first nitride film above the first columnar silicon layer and the second nitride film around the first columnar silicon layer by an etching process; and removing the pad oxide film, and the first oxide film and the fourth oxide layer. This feature makes it possible to form the gate electrode around the first columnar silicon layer.

[0052]

The method according to one preferred embodiment of the present invention includes the steps of: forming a third nitride film on the first columnar silicon layer fabricated on the first flat silicon layer, the gate electrode surrounding the first columnar silicon layer, etching back the third nitride film in such a manner that the respective upper surfaces of the first semiconductor layer of the second conductive type lying under the first columnar

silicon layer, and the upper portion of the first columnar silicon layer, are exposed, and forming a second insulating film sidewall serving as the sidewall-shaped second insulating film, to surround the upper sidewall of the first columnar silicon layer while contacting the upper surface of the gate electrode and to surround the sidewall of the gate electrode; introducing an impurity of the second conductive type into the upper portion of the first columnar silicon layer through an impurity introduction process comprising an impurity injection process, to form the second silicon layer of the second conductive type in the upper portion of the first columnar silicon layer, and form the silicon layer of the first conductive type between the first silicon layer of the second conductive type and the second silicon layer of the second conductive type; and forming a first metal film such as a nickel (Ni) film or a cobalt (Co) film, on the respective exposed surface of the first silicon layer of the second conductive type and the gate electrode, and an upper surface of the second silicon of the second conductive type, by a sputtering process, subjecting the first metal film to a heat treatment, and removing an unreacted part of the heat-treated film, to form a metal-semiconductor compound on each of the first silicon layer of the second conductive type and the second silicon layer of the second conductive type. According to this feature, the gate electrode, and each of the first silicon layer of the second conductive type formed under the first columnar silicon layer and the second silicon layer of the second conductive type formed in the upper portion of the first columnar silicon layer, are isolated from each other by the second insulating film sidewall. This makes it possible to prevent a short between the gate electrode and the respective ones of the first silicon layer of the second conductive type formed under the first columnar silicon layer and the second silicon layer of the second conductive type formed in the upper portion of the first columnar silicon layer, due to the metal-semiconductor compounds. In addition, the upper sidewall of the first columnar silicon layer is covered by the second insulating film sidewall. This makes it possible to prevent a metal-semiconductor compound from being formed on the upper sidewall of the first columnar silicon layer.

[0053]

The method according to one preferred embodiment of the present invention includes the steps of: forming a contact stopper such as a nitride film, on the first columnar silicon

layer fabricated on the first flat silicon layer, the gate electrode surrounding the first columnar silicon layer; forming a third oxide film serving as an interlayer insulating film, on the contact stopper, and flattening the third oxide film by a chemical mechanical polishing process; forming a contact hole in the third oxide film at position on the second silicon layer of the second conductive type formed in the upper portion of the first columnar silicon layer, by an etching process; forming two contact holes in the third oxide film at positions on respective upper sides of the first silicon layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar silicon layer, and the gate electrode, by an etching process; etching the portion of the contact stopper corresponding to the respective contact holes. This feature makes it possible to reduce a resistance of the contact.

[0054]

The semiconductor device according to the second aspect of the present invention comprises: a first flat semiconductor layer formed on a substrate; a first columnar semiconductor layer formed on the first flat semiconductor layer; a first semiconductor layer of a second conductive type formed in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; a second semiconductor layer of the second conductive type formed in an upper portion of the first columnar silicon layer; a semiconductor layer of a first conductive type formed between the first semiconductor layer of the second conductive type formed in the lower portion of the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar silicon layer; a gate insulating film and a gate electrode which are formed around the first columnar silicon layer; a first insulating film formed between the gate electrode and the first flat semiconductor layer; a sidewall-shaped second insulating film formed to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode and the first insulating film; a metal-semiconductor compound formed on each of an upper surface of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer, and an upper surface of the second

semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, wherein the first insulating film formed between the gate electrode and the first flat semiconductor layer has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer.

[0055]

In the semiconductor device according to the second aspect of the present invention, different voltages can be applied to respective ones of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar semiconductor layer, the gate electrode, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer. In addition, respective resistances of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, can be reduced while reducing a gate-source parasitic capacitance.

[0056]

The semiconductor device according to the third aspect of the present invention comprises: a first flat semiconductor layer formed on a substrate; a first columnar semiconductor layer formed on the first flat semiconductor layer; a first semiconductor layer of a second conductive type formed in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; a second semiconductor layer of the second conductive type formed in an upper portion of the first columnar silicon layer; a semiconductor layer of a first conductive type formed between the first semiconductor layer of the second conductive type formed in the lower portion of the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar silicon layer; a gate insulating film and a gate electrode which are formed around the first columnar silicon layer; a first insulating film formed between the gate electrode and the first flat semiconductor layer; a sidewall-shaped second insulating film formed to surround

an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode and the first insulating film; a metal-semiconductor compound formed on each of an upper surface of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer, and an upper surface of the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, wherein: the first insulating film formed between the gate electrode and the first flat semiconductor layer has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer; and a length between a central axis of the first columnar silicon layer and an edge of the first columnar silicon layer is larger than a sum of a length between the central axis of the first columnar silicon layer and a sidewall of the first columnar silicon layer, the thickness of the gate insulating film, a thickness of the gate electrode, and a thickness of the sidewall-shaped second insulating film formed to surround the sidewall of the gate electrode and the first insulating film.

[0057]

In the semiconductor device according to the third aspect of the present invention, in addition to the advantages of the semiconductor device according to the third aspect of the present invention, the metal-semiconductor compound can be adequately formed on the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar semiconductor layer to reduce a resistance of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer lying under the first columnar semiconductor layer.

[0058]

The semiconductor device according to the fourth aspect of the present invention comprises: a first flat semiconductor layer formed on a substrate; a first columnar semiconductor layer formed on the first flat semiconductor layer; a first semiconductor layer of a second conductive type formed in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor

layer; a second semiconductor layer of the second conductive type formed in an upper portion of the first columnar silicon layer; a semiconductor layer of a first conductive type formed between the first semiconductor layer of the second conductive type formed in the lower portion of the first columnar semiconductor layer, and the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar silicon layer; a gate insulating film and a gate electrode which are formed around the first columnar silicon layer; a first insulating film formed between the gate electrode and the first flat semiconductor layer; a sidewall-shaped second insulating film formed to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode; a metal-semiconductor compound formed on each of an upper surface of the first semiconductor layer of the second conductive type formed in the entirety or the upper portion of the first flat semiconductor layer, and an upper surface of the second semiconductor layer of the second conductive type formed in the upper portion of the first columnar semiconductor layer, wherein: the first insulating film formed between the gate electrode and the first flat semiconductor layer has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer; and the gate electrode has a thickness larger than that of the sidewall-shaped second insulating film formed to surround the upper sidewall of the first columnar silicon layer while contacting the upper surface of the gate electrode.

[0059]

In the semiconductor device according to the fourth aspect of the present invention, in addition to the advantages of the semiconductor device according to the third aspect of the present invention, a metal-semiconductor compound can be adequately on the gate electrode, according to need, to reduce a resistance of the gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0060]

FIG. 1(a) is a top plan view showing one step in a method of manufacturing a semiconductor device, according to one embodiment of the present invention.

FIG. 1(b) is a sectional view taken along the line A-A' in FIG. 1(a).

FIG. 2(a) is a top plan view showing one step in the method.

FIG. 2(b) is a sectional view taken along the line A-A' in FIG. 2(a).

FIG. 3(a) is a top plan view showing one step in the method.

FIG. 3(b) is a sectional view taken along the line A-A' in FIG. 3(a).

FIG. 4(a) is a top plan view showing one step in the method.

FIG. 4(b) is a sectional view taken along the line A-A' in FIG. 4(a).

FIG. 5(a) is a top plan view showing one step in the method.

FIG. 5(b) is a sectional view taken along the line A-A' in FIG. 5(a).

FIG. 6(a) is a top plan view showing one step in the method.

FIG. 6(b) is a sectional view taken along the line A-A' in FIG. 6(a).

FIG. 7(a) is a top plan view showing one step in the method.

FIG. 7(b) is a sectional view taken along the line A-A' in FIG. 7(a).

FIG. 8(a) is a top plan view showing one step in the method.

FIG. 8(b) is a sectional view taken along the line A-A' in FIG. 8(a).

FIG. 9(a) is a top plan view showing one step in the method.

FIG. 9(b) is a sectional view taken along the line A-A' in FIG. 9(a).

FIG. 10(a) is a top plan view showing one step in the method.

FIG. 10(b) is a sectional view taken along the line A-A' in FIG. 10(a).

FIG. 11(a) is a top plan view showing one step in the method.

FIG. 11(b) is a sectional view taken along the line A-A' in FIG. 11(a).

FIG. 12(a) is a top plan view showing one step in the method.

FIG. 12(b) is a sectional view taken along the line A-A' in FIG. 12(a).

FIG. 13(a) is a top plan view showing one step in the method.

FIG. 13(b) is a sectional view taken along the line A-A' in FIG. 13(a).

FIG. 14(a) is a top plan view showing one step in the method.

FIG. 14(b) is a sectional view taken along the line A-A' in FIG. 14(a).

FIG. 15 (a) is a top plan view showing one step in the method.

FIG. 15(b) is a sectional view taken along the line A-A' in FIG. 15(a).

FIG. 16(a) is a top plan view showing one step in the method.

FIG. 16(b) is a sectional view taken along the line A-A' in FIG. 16(a).

FIG. 17(a) is a top plan view showing one step in the method.

FIG. 17(b) is a sectional view taken along the line A-A' in FIG. 17(a).

FIG. 18(a) is a top plan view showing one step in the method.

FIG. 18(b) is a sectional view taken along the line A-A' in FIG. 18(a).

FIG. 19(a) is a top plan view showing one step in the method.

FIG. 19(b) is a sectional view taken along the line A-A' in FIG. 19(a).

FIG. 20(a) is a top plan view showing one step in the method.

FIG. 20(b) is a sectional view taken along the line A-A' in FIG. 20(a).

FIG. 21(a) is a top plan view showing one step in the method.

FIG. 21(b) is a sectional view taken along the line A-A' in FIG. 21(a).

FIG. 22(a) is a top plan view showing one step in the method.

FIG. 22(b) is a sectional view taken along the line A-A' in FIG. 22(a).

FIG. 23(a) is a top plan view showing one step in the method.

FIG. 23(b) is a sectional view taken along the line A-A' in FIG. 23(a).

FIG. 24(a) is a top plan view showing one step in the method.

FIG. 24(b) is a sectional view taken along the line A-A' in FIG. 24(a).

FIG. 25(a) is a top plan view showing one step in the method.

FIG. 25(b) is a sectional view taken along the line A-A' in FIG. 25(a).

FIG. 26(a) is a top plan view showing one step in the method.

FIG. 26(b) is a sectional view taken along the line A-A' in FIG. 26(a).

FIG. 27(a) is a top plan view showing one step in the method.

FIG. 27(b) is a sectional view taken along the line A-A' in FIG. 27(a).

FIG. 28(a) is a top plan view showing one step in the method.

FIG. 28(b) is a sectional view taken along the line A-A' in FIG. 28(a).

FIG. 29(a) is a top plan view showing one step in the method.

FIG. 29(b) is a sectional view taken along the line A-A' in FIG. 29(a).

FIG. 30(a) is a top plan view showing one step in the method.

FIG. 30(b) is a sectional view taken along the line A-A' in FIG. 30(a).

FIG. 31(a) is a top plan view showing one step in the method.

FIG. 31(b) is a sectional view taken along the line A-A' in FIG. 31(a).

FIG. 32(a) is a top plan view showing one step in the method.

FIG. 32(b) is a sectional view taken along the line A-A' in FIG. 32(a).

FIG. 33(a) is a top plan view showing one step in the method.

FIG. 33(b) is a sectional view taken along the line A-A' in FIG. 33(a).

FIG. 34(a) is a top plan view showing one step in the method.

FIG. 34(b) is a sectional view taken along the line A-A' in FIG. 34(a).

FIG. 35(a) is a top plan view showing one step in the method.

FIG. 35(b) is a sectional view taken along the line A-A' in FIG. 35(a).

FIG. 36(a) is a top plan view showing one step in the method.

FIG. 36(b) is a sectional view taken along the line A-A' in FIG. 36(a).

FIG. 37(a) is a top plan view showing one step in the method.

FIG. 37(b) is a sectional view taken along the line A-A' in FIG. 37(a).

FIG. 38(a) is a top plan view showing one step in the method.

FIG. 38(b) is a sectional view taken along the line A-A' in FIG. 38(a).

FIG. 39(a) is a top plan view showing a semiconductor device obtained by the method.

FIG. 39(b) is a sectional view taken along the line A-A' in FIG. 39(a).

FIG. 40(a) is a top plan view showing a semiconductor device obtained by the method.

FIG. 40(b) is a sectional view taken along the line A-A' in FIG. 40(a).

FIG. 41(a) is a top plan view showing a semiconductor device obtained by the method.

FIG. 41(b) is a sectional view taken along the line A-A' in FIG. 41(a).

FIG. 42 is a sectional view taken along the line B-B' in FIG. 41(a).

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0061]

FIG. 41(a) is a top plan view showing an NMOS (N-channel metal oxide semiconductor)-type SGT obtained by an SGT manufacturing method according to one embodiment of the present invention, and FIG. 41(b) is a sectional view taken along the

line A-A' in FIG. 41(a). With reference to FIGS. 41(a) and 41(b), a structure of the NMOS-type SGT will be described below.

[0062]

A first flat silicon layer 112 which is a first flat semiconductor layer, is formed on a silicon substrate 110 which is a substrate, and a first columnar silicon layer 113 which is a first columnar semiconductor layer, is formed on the first flat silicon layer 112. A source diffusion layer 200 which is a first semiconductor layer of a second conductive type, is formed in a lower portion of the first columnar silicon layer 113 and an upper portion (or an entirety) of the flat silicon layer 112, and a drain diffusion layer 201 which is a second semiconductor layer of the second conductive type, is formed in an upper portion of the columnar silicon layer 113.

[0063]

A body 309 which is a semiconductor layer of a first conductive type, is formed between the source diffusion layer 200 formed in the lower portion of the first columnar silicon layer 113 and the upper portion (or an entirety) of the flat silicon layer 112, and the drain diffusion layer 201 formed in the upper portion of the columnar silicon layer 113.

[0064]

A gate insulating film 124, and a gate electrode 141 (a gate electrode body 141a surrounding the body 309, and a gate wiring 141b extending from the gate electrode body 141a), are formed around the first columnar silicon layer 113.

[0065]

Further, a first insulating film 303, i.e., an oxide film having a thickness larger than that of the gate insulating film 124, is formed between the gate electrode 141 and the source diffusion layer 200. Based on forming the first insulating film 303, i.e., the oxide film having a thickness larger than that of the gate insulating film 124, between the gate electrode 141 and the source diffusion layer 200, a gate-source parasitic capacitance can be reduced.

[0066]

A second insulating film sidewall 134, i.e., a sidewall-shaped second insulating film, is formed to surround an upper sidewall of the first columnar silicon layer 113 while

contacting an upper surface of the gate electrode 141 (gate electrode body 141a), and a second insulating film sidewall 133, i.e., a sidewall-shaped second insulating layer, is formed to surround a sidewall of the gate electrode 141.

[0067]

A metal-semiconductor compound 153 is formed in an upper surface of the source diffusion layer 200, and a metal-semiconductor compound 152 is formed in an upper surface of the drain diffusion layer 201. Further, a metal-semiconductor compound 151 is formed in an upper surface of the gate electrode 141.

[0068]

A contact 174 is formed on the source diffusion layer 200 (metal-semiconductor compound 153), and a contact 173 is formed on the drain diffusion layer 201 (metal-semiconductor compound 152). Further, a contact 172 is formed on the gate wiring 141b (the metal-semiconductor compound 151).

[0069]

FIG. 42 is a sectional view taken along the line B-B' in FIG. 41(a). The metal-semiconductor compound 153 is formed as a means to reduce a resistance of a source region. In order to allow the metal-semiconductor compound 153 to be formed in the source diffusion layer 200, it is necessary to satisfy the following conditional formula (1) in FIG. 42:

$$Wa > Wp + Wox + Wg + Ws \quad \text{----- (1)}$$

, wherein: Wa is a length between a central axis of the first columnar silicon layer 113 and an edge of the source diffusion layer 200;

Wp is a length between the central axis of the first columnar silicon layer 113 and a sidewall thereof;

Wox is a thickness of the gate insulating film 124 (first columnar silicon layer 113);

Wg is a width (thickness) of the gate electrode 141 (gate electrode body 141a); and

Ws is a width (thickness) of the second insulating film sidewall 133 (i.e., second insulating film).

[0070]

The metal-semiconductor compound 151 is formed as a means to reduce a resistance of a gate region. In order to allow the metal-semiconductor compound 151 to be formed in the gate electrode 141, it is necessary to satisfy the following conditional formula (2) in FIG. 42:

$$Wg > Ws \qquad \text{----- (2)}$$

, wherein Wg is the width of the gate electrode 141 (gate electrode body 141a), and Ws is the width of the second insulating film sidewall 134 (i.e., second insulating film).

[0071]

A structure satisfying the conditional formulas (1) and (2) allows the metal-semiconductor compound 151, 152, 153 to be formed so as to reduce resistance of the gate electrode, the drain region and the source region to increase an ON-current.

[0072]

The SGT can perform a transistor operation by applying a potential of zero to Vcc to the gate electrode 141 under a condition that the source diffusion layer 200 and the drain diffusion layer 201 are connected to a GND potential and a Vcc potential, respectively.

[0073]

The diffusion layer to be formed in the upper portion of the first columnar silicon layer 113, and the diffusion layer to be formed in the lower portion of the first columnar silicon layer 113 and the upper portion (or an entirety) of the flat silicon layer 112, may be a source diffusion layer and a drain diffusion layer, respectively.

[0074]

With reference to FIGS. 1(a) to 41(b), an SGT manufacturing method according to one embodiment of the present invention will be described below. FIGS. 1(a) to 41(b) show respective steps in the SGT manufacturing method according to the embodiment, wherein each of FIGS. 1 to 41 with the suffix (a) is a top plan view, and each of FIGS. 1 to 41 with the suffix (b) is a sectional view taken along the line A-A' in a corresponding one of FIGS. 1 to 41 with the suffix (a). In FIGS. 1(a) to 41(b), the same element is defined by a common reference numeral or code. In the following description, a combination of

FIGS. 1(a) and 1(b) to a combination of FIGS. 41(a) and 41(b) will be referred to as "FIG. 1" to "FIG. 41", respectively.

[0075]

Referring to FIG. 1, a pad oxide film 121 is formed on a silicon substrate 110.

[0076]

Referring to FIG. 2, a first nitride film 130 is formed on the pad oxide film 121, and then a first amorphous silicon or polysilicon film 140 is formed on the first nitride film 130.

[0077]

Referring to FIG. 3, a resist is applied onto the first amorphous silicon or polysilicon film 140, and a first columnar layer pattern is transferred to the resist through lithography to leave a first resist 301 corresponding to the first columnar layer pattern.

[0078]

Referring to FIG. 4, the first amorphous silicon or polysilicon film 140 and the first nitride film 130 are etched in turn to form a first hard mask, and then the pad oxide film 121 is etched.

[0079]

Referring to FIG. 5, the first resist 301 is removed.

[0080]

Referring to FIG. 6, the silicon substrate 110 is dry-etched, using the first hard mask consisting of respective remaining portions of the first amorphous silicon or polysilicon film 140 and the first nitride film 130, to form a first columnar silicon layer 113. During this dry etching process, the first amorphous silicon or polysilicon film 140 is also etched. In this case, when the first amorphous silicon or polysilicon film 140 is fully etched, a plasma emission intensity detectable by a dry etching apparatus is changed. Thus, a termination timing of the dry etching process can be determined by detecting the change in plasma emission intensity, so as to stably control a height dimension of the first columnar silicon layer 113 irrespective of an etching rate.

[0081]

In order to utilize the above termination-timing detection technique, it is necessary

that a thickness (height dimension) of the first amorphous silicon or polysilicon film 140 before the dry etching process for forming the first columnar silicon layer 113 is less than that of the first columnar silicon layer 113.

[0082]

Referring to FIG. 7, respective surfaces of the first columnar silicon layer 113 and the silicon substrate 110 are sacrificially oxidized to form a sacrificial oxide film 123 so as to reduce irregularities of a sidewall of the first columnar silicon layer 113 for use as a channel region, and remove respective surface portions of the first columnar silicon layer 113 and the silicon substrate 110 (i.e., silicon surface) having carbon and others implanted thereinto during the dry etching process.

[0083]

Referring to FIG. 8, a resist is applied onto the in-process structure in FIG. 7, and a first flat silicon layer pattern is transferred to the resist through lithography to leave a second resist 150 corresponding to the first flat silicon layer pattern. The above sacrificial oxide film 123 formed on the first columnar silicon layer 113 and the silicon substrate 110 by the sacrificial oxidation can protect the silicon surface from contaminations, such as by-products to be produced during a subsequent dry etching process.

[0084]

Referring to FIG. 9, the silicon substrate 110 is dry-etched to form a first flat silicon layer 112.

[0085]

Referring to FIG. 10, the second resist 150 is removed.

[0086]

Referring to FIG. 11, a filling oxide film 120 is deposited on the in-process structure in FIG. 10, and flattened to have a surface flush with an upper surface of the first nitride film 130.

[0087]

Referring to FIG. 12, the filling oxide film 120 is etched in such a manner as to allow a surface of an upper portion of the first flat silicon layer 112 to be exposed.

[0088]

Referring to FIG. 13, offset spacer 307 is formed on a sidewall of the first columnar silicon layer 113 to protect the first columnar silicon layer in source implant. Referring to FIG. 14, an impurity, such as arsenic (As) or phosphorus (P), is injected into the first flat silicon layer 112 to form a source diffusion layer 200 which is a silicon layer of a second conductive type, in a lower portion of the first columnar silicon layer 113 and an upper portion (or an entirety) of the first flat silicon layer 112.

[0089]

In this step, the first nitride film 130 formed above the first columnar silicon layer 113 prevents the impurity from being injected into the upper portion of the first columnar silicon layer 113. The impurity injection for the source diffusion layer 200 to be formed in the upper portion (or an entirety) of the first flat silicon layer 112, and the impurity injection for the drain diffusion layer 201 to be formed in the upper portion of the first columnar silicon layer 113, are performed separately, so that conditions of the respective impurity injections can be easily optimized to restrain a short channel effect so as to reduce a leakage current.

[0090]

Referring to FIG. 15, offset spacer 307 is etched.

[0091]

Referring to FIG. 16, a first insulating film material 303, such as an oxide film, is deposited on the in-process structure in FIG. 15. Specifically, the first insulating film material 303 is formed around a lower sidewall of the first columnar silicon layer 113 and above the source diffusion layer 200 and the first columnar silicon layer 113, at a relatively large thickness, and formed around an intermediate/upper sidewall of the first columnar silicon layer 113 at a relatively small thickness.

[0092]

Referring to FIG. 17, the first insulating film material 303 around the intermediate/upper sidewall of the first columnar silicon layer 113 is etched. Preferably, this etching process is an isotropic etching process. The first insulating film material 303 is formed around the lower sidewall of the first columnar silicon layer 113 and above the

source diffusion layer 200 and the first columnar silicon layer 113, at a relatively large thickness, and formed around an intermediate/upper sidewall of the first columnar silicon layer 113 at a relatively small thickness, as mentioned above. Thus, even after the etching process, a part of the first insulating film material 303 remains around the lower sidewall of the first columnar silicon layer 113 and above the source diffusion layer 200 and the first columnar silicon layer 113 (a part of the first insulating film material 303 remaining above the first columnar silicon layer 113 will hereinafter be referred to as "insulating film 306"). The first insulating film material 303 remaining around the lower sidewall of the first columnar silicon layer 113 and above the source diffusion layer 200 will make up a "first insulating film 303 having a thickness larger than that of an after-mentioned gate insulating film 124", to be formed between the source diffusion layer 200 and the subsequently-formed gate electrode 141. This first insulating film 303 can reduce a parasitic capacitance between the source diffusion layer 200 and the subsequently-formed gate electrode 141.

[0093]

The first insulating film 303 to be formed between the first flat silicon layer 112 (source diffusion layer 200) and the subsequently-formed gate electrode 141 may be formed by depositing an insulating film on the in-process structure in FIG. 15, and flattening the insulating film to have a surface flush with the upper surface of the first nitride film 130, and etching the insulating film.

[0094]

Referring to FIG. 18, a gate insulating film 124, such as an oxide film or a silicon oxynitride film, is formed on the sidewall of the pad oxide film 121 and the intermediate/upper sidewall of the first columnar silicon layer 113. Referring to FIG. 19, a second amorphous silicon or polysilicon film 141 which is a gate conductive film, is formed to allow the first columnar silicon layer 113 to be embedded therein.

[0095]

Referring to FIG. 20, the second amorphous silicon or polysilicon film 141 is polished by a chemical mechanical polishing (CMP) process to have a flattened upper surface flush with the upper surface of the first nitride film 130. In the CMP process, a polishing

amount can be controlled with enhanced reproducibility by using, as a CMP stopper, the first nitride film 130 which is the first hard mask.

[0096]

Referring to FIG. 21, the second amorphous silicon or polysilicon film 141 which is the gate conductive film, is etched back to determine a gate length.

[0097]

Referring to FIG. 22, a first oxide film 125 is deposited on the in-process structure in FIG. 21, and a second nitride film 131 is deposited on the first oxide film 125. The first oxide film 125 will protect an upper surface of the subsequently-formed gate electrode 141 from a wet etching or dry etching process to be performed in a subsequent step, so as to suppress a change in the gate length, i.e., a variation in the gate length, and damage of the gate insulating film 124 from the upper surface of the subsequently-formed gate electrode 141.

[0098]

Referring to FIG. 23, the second nitride film 131 is etched back to form a third insulating film sidewall. In this process, the first oxide film 125 is also etched. A thickness of the third insulating film sidewall will determine a thickness of a subsequently-formed gate electrode body 141a. Thus, the subsequently-formed gate electrode body 141a can have a desired thickness by adjusting the thickness of the second nitride film 131 and conditions of the etching back process. [0099]

Referring to FIG. 24, an impurity, such as phosphorus (P), is injected into the second amorphous silicon or polysilicon film 141 which is the gate conductive film.

[0100]

Referring to FIG. 25, a bottom anti-reflective coating (BARC) layer 161 is applied onto the in-process structure in FIG. 24. Then, a resist is applied onto the BARC layer 161, and a gate wiring pattern is transferred to the resist through lithography to leave a third resist 160 corresponding to the gate wiring pattern.

[0101]

Referring to FIG. 26, the BARC layer 161, and the second amorphous silicon or polysilicon film 141 which is the gate conductive film, are etched using the third resist 160

as a mask to form a gate electrode 141 consisting of a gate electrode body 141a and a gate wiring 141b.

[0102]

Referring to FIG. 27, the first insulating layer 303 is partly removed by a dry etching or wet etching process to allow the source diffusion layer 200 to be exposed.

[0103]

Referring to FIG. 28, the third resist 160 and the BARC layer 161 are removed and a fourth oxide layer 305 formed on an exposed surface of the gate electrode 141 and the source diffusion layer to protect the gate electrode 141 during a subsequent process of removing the first nitride film 130 and the second nitride film 131.

[0104]

Referring to FIG. 29, the first nitride film 130 above the first columnar silicon layer 113 and the second nitride film 131 around the first columnar silicon layer 113 are removed by a dry etching or wet etching process.

[0105]

Referring to FIG. 30, the pad oxide film 121, the first oxide film 125 and the fourth oxide layer 305 are removed.

[0106]

Referring to FIG. 31, a third nitride film 132 is formed on the in-process structure in FIG. 30.

[0107]

Referring to FIG. 32, the third nitride film 132 is etched back in such a manner that the respective upper surfaces of the source diffusion layer 200 and the first columnar silicon layer 113 are exposed, and a second insulating film sidewall 133 and a second insulating film sidewall 134 which serve as a sidewall-shaped second insulating film, are formed around a sidewall of the gate electrode 141 and an upper sidewall of the first columnar silicon layer 113, respectively. The second insulating film sidewalls 133, 134 can separate between the gate electrode 141 and respective ones of the source diffusion layer 200 and the after-mentioned drain diffusion layer 201 to be formed in the upper portion of the first columnar silicon layer 113, so as to prevent a short between the gate

electrode 141 and respective ones of the source diffusion layer 200 and the after-mentioned drain diffusion layer 201 due to after-mentioned metal-semiconductor compounds. In addition, the second insulating film sidewall 134 covering the upper sidewall of the first columnar silicon layer 113 can prevent a metal-semiconductor compound from being formed on the upper sidewall of the first columnar silicon layer 113 in a subsequent step.

[0108]

Referring to FIG. 33, an impurity, such as P or As, is introduced into the upper portion of the first columnar silicon layer 113 through an impurity introduction process comprising an impurity injection process, to form a drain diffusion layer 201 in the upper portion of the first columnar silicon layer 113. A portion of the first columnar silicon layer 113 between the source diffusion layer 200 and the drain diffusion layer 201 is formed as a body 309 which is a semiconductor layer of a first conductive type.

[0109]

Referring to FIG. 34, a first metal film, such as a nickel (Ni) film or a cobalt (Co) film, is formed on the respective exposed surface of the source diffusion layer 200 and the gate electrode 141, and an upper surface of the drain diffusion layer 201 by a sputtering process. The first metal film is then subjected to a heat treatment, and an unreacted part of the heat-treated film is removed to form a metal-semiconductor compound 151, a metal-semiconductor compound 152 and a metal-semiconductor compound 153, on the gate electrode 141, the drain diffusion layer 201 and the source diffusion layer 200, respectively.

[0110]

The metal-semiconductor compound 151 formed on the gate electrode 141 surrounding the first columnar silicon layer 113 can reduce a resistance of the gate electrode 141. As long as the width Wg of the gate electrode 141 and the width Ws of the second insulating film sidewall 134 are satisfy the following relation: $Wg > Ws$, and the upper surface of the gate electrode 141 is exposed, the metal-semiconductor compound 151 can be formed on the gate electrode 141.

[0111]

Referring to FIG. 35, a contact stopper 135, such as a nitride film, is formed on the

in-process structure in FIG. 34.

[0112]

Referring to FIG. 36, an interlayer insulating film 126 which is a third oxide film, is formed on the in-process structure in FIG. 35, and then flattened by a CMP process.

[0113]

Referring to FIG. 37, a contact hole is formed in the interlayer insulating film 126 at positions on upper side of the drain diffusion layer 201 in the upper portion of the first columnar silicon layer 113 by an etching process. The etching process for the contact holes is stopped by the contact stopper 135.

[0114]

Referring to FIG. 38, two contact holes are formed in the interlayer insulating film 126 at positions on respective upper sides of the gate wiring 141b, and the source diffusion layer 200, by an etching process. The etching process for each of the contact holes is stopped by the contact stopper 135.

[0115]

Referring to FIG. 39, portions of the contact stopper 135 corresponding to the respective contact holes are etched.

[0116]

Referring to FIG. 40, a barrier metal film 171, such as a tantalum (Ta) film or a tantalum nitride (TaN) film, is formed on an inner peripheral surface of each of the contact holes. Then, a metal film, such as a copper (Cu) film, is formed on the barrier metal film 171 by a sputtering process or a plating process, and subjected to a CMP process to form three contacts (contact plugs) 172, 173, 174 corresponding to respective ones of the gate wiring 141b, the drain diffusion layer 201 and the source diffusion layer 200. A titanium (Ti) film or a titanium nitride (TiN) film may be used as the barrier metal film 171. A tungsten (W) film may also be used. Further, a copper-containing alloy film may be used.

[0117]

Referring to FIG. 41, a barrier metal film 175, such as a Ta film or a TaN film, is formed on the in-process structure in FIG. 40, and then a metal film 176 is formed on the barrier metal film 175. Then, the barrier metal film 175 and the metal film 176 are

subjected to lithography to form three first layer wirings 177, 178, 179 corresponding to respective ones of the contacts 172, 173, 174. A titanium (Ti) film or a titanium nitride (TiN) film may be used as the barrier metal film 175. A tungsten (W) film may also be used.

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a columnar semiconductor layer (113) on a substrate (110), and forming a first flat semiconductor layer (112) in an upper portion of the substrate (110) lying under the columnar semiconductor layer (113);

forming a first semiconductor layer of a second conductive type (200) in a lower portion of the columnar semiconductor layer (113) and an entirety or an upper portion of the first flat semiconductor layer (112), which constitutes an etched mesa with edges;

forming a first insulating film (303) around a lower sidewall of first columnar semiconductor layer (113) and above the first flat semiconductor layer (112);

forming a gate insulating film (124) and a gate electrode (141) around the columnar semiconductor layer;

forming a sidewall-shaped second insulating film (133, 134) to surround an upper sidewall of the columnar semiconductor layer (113) while contacting an upper surface of the gate electrode (141) and to surround a sidewall of the gate electrode (141) and the first insulating film (303);

forming a second semiconductor layer of the second conductive type in an upper portion of the columnar semiconductor layer (113), and forming a semiconductor layer of a first conductive type between the first semiconductor layer of the second conductive type and the second semiconductor layer of the second conductive type; and

forming a metal-semiconductor compound (152, 153) on each of an upper surface of the first semiconductor layer of the second conductive type (200) and an upper surface of the second semiconductor layer of the second conductive type (201),

wherein the first insulating film (303) has a thickness larger than that of the gate insulating film (124) formed around the columnar semiconductor layer (113),

wherein the sum of the half length of the columnar semiconductor layer (113), the thickness of the gate insulating film (124), the width of the gate electrode (141a) and the width of the second insulating film (133) covering the sidewall of the gate electrode (141a)

with these layers being abutted with the side wall of one layer abutting the side wall of the next, is smaller than the length between the centre of the columnar semiconductor layer (113) and the edge of the first semiconductor layer of a second conductive type (200) in the mesa.

2. The method as defined in claim 1, wherein:

the first flat semiconductor layer (112) is a first flat silicon layer (112);

the columnar semiconductor layer (113) is a columnar silicon layer (113);

the semiconductor layer of the first conductive type (309) is a silicon layer of the first conductive type (309);

the first semiconductor layer of the second conductive type (200) is a first silicon layer of the second conductive type (200); and

the second semiconductor layer of the second conductive type (201) is a second silicon layer of the second conductive type (201).

3. The method as defined in claim 2, wherein:

the semiconductor layer of the first conductive type (309) is a p-type silicon layer or a non-doped silicon layer;

the first semiconductor layer of the second conductive type (200) is an n-type silicon layer; and

the second semiconductor layer of the second conductive type (201) is an n-type silicon layer.

4. The method as defined in claim 2, wherein:

the semiconductor layer of the first conductive type (309) is an n-type silicon layer or a non-doped silicon layer;

the first semiconductor layer of the second conductive type (200) is a p-type silicon layer; and

the second semiconductor layer of the second conductive type (201) is a p-type silicon

layer.

5. The method as defined in claim 2, which includes the steps of:

forming a pad oxide film (121) on the silicon substrate (110);

forming on the pad oxide film (121) a first nitride film (130) for use as a mask during the formation of the columnar silicon layer (113);

forming a first amorphous silicon or polysilicon film (140) on the first nitride film (130);

applying a resist onto the first amorphous silicon or polysilicon film(140), and transferring a first columnar layer pattern to the resist through lithography to leave a first resist (301) corresponding to the first columnar layer (113) pattern; and

etching the first amorphous silicon or polysilicon film and the first nitride film in turn to form a first hard mask (140, 130).

6. The method as defined in claim 5, which includes the step of forming the columnar silicon layer by a dry etching process using the first hard mask (140,130).

7. The method as defined in claim 6, wherein the first amorphous silicon or polysilicon film (140) serving as the first hard mask (140, 130) is fully etched during the dry etching process to cause a change in plasma emission intensity detectable by a dry etching apparatus, and wherein the step of forming the columnar silicon layer (113) includes detecting the change in the plasma emission intensity, and determining a termination timing of the dry etching process based on the detection result to control a height dimension of the columnar silicon layer (113).

8. The method as defined in claim 7, wherein a height dimension of the first amorphous silicon or polysilicon film (140) before the dry etching process is less than that of the columnar silicon layer (113).

9. The method as defined in claim 2, which includes the step of sacrificially oxidizing a surface of the columnar silicon layer (113) fabricated on the substrate (110) so as to reduce irregularities of a sidewall of the columnar silicon layer (113) for use as a channel region while removing a surface portion of the columnar silicon layer (113) having carbon implanted thereinto during the dry etching process, and protect the columnar silicon layer (113) from contaminations including a by-product to be produced during a subsequent dry etching process.

10. The method as defined in claim 2, which includes the steps of:

applying a resist onto the substrate (110) having the columnar silicon layer (113) and transferring a first flat silicon layer (112) pattern to the resist through lithography to leave a second resist (150) corresponding to the first flat silicon layer (112) pattern; and

etching the silicon substrate (110) to form the first flat silicon layer (112), and removing the second resist (150).

11. The method as defined in claim 2, which includes the steps of:

depositing a filling oxide film (120) on the first flat silicon layer (112) and substrate (110) having the columnar silicon layer (113) ;

flattening the filling oxide film (120); and

etching the filling oxide film (120) in such a manner as to allow a surface of an upper portion of the first flat silicon layer (112) to be exposed.

12. The method as defined in claim 2, which includes the step of the offset spacer (307) formation on the sidewall of the columnar silicon layer (113).

13. The method as defined in claim 2, wherein the first silicon layer of the second conductive type (200) is formed in the lower portion of the columnar silicon layer (113) and the entirety or the upper portion of the first flat semiconductor layer (112) by introducing an impurity of the second conductive type into the first flat semiconductor

layer (112) having the columnar silicon layer with a offset spacer (307) through an impurity introduction process comprising an impurity injection process and then, the offset spacer is etched.

14. The method as defined in claim 2, wherein the first silicon layer of the second conductive type (200) is formed in the lower portion of the columnar silicon layer (113) without injecting any impurity into the upper portion of the columnar silicon layer (113).

15. The method as defined claim 2, which includes the steps of:

depositing a first insulating film (303) material above and around the columnar silicon layer (113) fabricated on the first flat silicon layer (112), in such a manner that the first insulating film (303) material deposited above the columnar silicon layer (113) and around the lower sidewall of the columnar silicon layer (113) has a thickness larger than that of the first insulating film (303) material deposited around an intermediate/upper sidewall of the columnar silicon layer (113); and

etching the first insulating film (303) material around the intermediate/upper sidewall of the columnar silicon layer (113) to form the first insulating film (303, 306) above the columnar silicon layer (113) and around the lower sidewall of the columnar silicon layer (113), in such a manner as to have a thickness larger than that of the gate insulating film (124) to be formed around the columnar silicon layer (113).

16. The method as defined in claim 2, wherein the gate insulating film (124) is formed on the sidewall of the columnar silicon layer (113) with a first hard mask (130) of nitride film fabricated on the first flat silicon layer (112), and wherein the method includes the steps of:

forming a second amorphous silicon or polysilicon film (141) serving as a gate electrode material, on an in-process structure obtained by the step of forming the gate insulating film (124), in such a manner as to allow the columnar silicon layer (113) to be embedded therein; and

polishing the second amorphous silicon or polysilicon film (141) by a chemical

mechanical polishing process to have a flattened upper surface, wherein the nitride film (130) serving as the first hard mask is used as a stopper against the chemical mechanical polishing process to control a polishing amount with enhanced reproducibility.

17. The method as defined in claim 16, which includes the steps of:

etching back the second amorphous silicon or polysilicon film (141) serving as the gate electrode material, to allow the gate electrode (141) to be formed with a desired gate length; and

depositing a first oxide film (125) on an in-process structure obtained by the step of etching back the second amorphous silicon or polysilicon film (141), whereby the first oxide film (125) can protect an upper surface of the gate electrode (141) from a wet etching or dry etching process to be performed in a subsequent step, so as to suppress a change or variation in the gate length and damage of the gate insulating film (124) from the upper surface of the gate electrode (141).

18. The method as defined in claim 17, which includes the steps of:

forming a second nitride film (131) on the first oxide film (125);

etching back the second nitride film (131) to form a third insulating film sidewall, and etching the first oxide film(125);

applying a bottom anti-reflective coating (BARC) layer (161) onto an in-process structure obtained by the step of etching back the second nitride film (131), applying a resist onto the BARC layer (161), and transferring a gate wiring (141b) pattern to the resist through lithography to leave a third resist (160) corresponding to the gate wiring (141b) pattern;

etching the BARC layer (161), and the second amorphous silicon or polysilicon film (141) serving as the gate electrode (141) material, using the third resist (160) as a mask, to form a gate electrode body (141a) and a gate wiring (141b) which make up the gate electrode (141);

partly removing the first insulating film (303) by a dry etching or wet etching to allow

the surfaces of the first semiconductor layer of the second conductive type (200) lying under the columnar silicon layer (113) to be exposed;

the removing the resist (160) and the BARC (161);

forming the fourth oxide layer (305) on an exposed surface of the gate electrode (141) and the surfaces of the first semiconductor layer of the second conductive type (200) lying under the columnar silicon layer (113);

removing the first nitride film (130) above the columnar silicon layer (113) and the second nitride film (131) around the columnar silicon layer (113) by an etching process; and

removing the pad oxide film (121), and the first oxide film (125) and the fourth oxide layer (305).

19. The method as defined in claim 2, which includes the steps of:

forming a third nitride film (132) on the columnar silicon layer (113) fabricated on the first flat silicon layer (112), the gate electrode (141) surrounding the columnar silicon layer (113), etching back the third nitride film (132) in such a manner that the respective upper surfaces of the first semiconductor layer of the second conductive type (200) lying under the columnar silicon layer (113), and the upper portion of the columnar silicon layer (113), are exposed, and forming a second insulating film sidewall (133, 134) serving as the sidewall-shaped second insulating film, to surround the upper sidewall of the columnar silicon layer (113) while contacting the upper surface of the gate electrode (114) and to surround the sidewall of the gate electrode (141);

introducing an impurity of the second conductive type into the upper portion of the columnar silicon layer (113) through an impurity introduction process comprising an impurity injection process, to form the second silicon layer of the second conductive type (201) in the upper portion of the columnar silicon layer (113), and form the silicon layer of the first conductive type (309) between the first silicon layer of the second conductive type (200) and the second silicon layer of the second conductive type (201); and

forming a first metal film such as a nickel (Ni) film or a cobalt (Co) film, on the

respective exposed surface of the first silicon layer of the second conductive type (200) and the gate electrode (141), and an upper surface of the second silicon of the second conductive type (201), by a sputtering process, subjecting the first metal film to a heat treatment, and removing an unreacted part of the heat-treated film, to form a metal-semiconductor compound (153, 152) on each of the first silicon layer of the second conductive type (200) and the second silicon layer of the second conductive type (201).

20. The method as defined in claim 2, which includes the steps of:

forming a contact stopper (135) such as a nitride film, on the columnar silicon layer (113) fabricated on the first flat silicon layer (112), the gate electrode (141) surrounding the columnar silicon layer (113);

forming a third oxide film (126) serving as an interlayer insulating film, on the contact stopper (135), and flattening the third oxide film (126) by a chemical mechanical polishing process;

forming a contact hole in the third oxide film (126) at position on the upper side of the second silicon layer of the second conductive type (201) formed in the upper portion of the columnar silicon layer (113), by an etching process;

forming contact holes in the third oxide film (126) at positions on respective upper sides of the first silicon layer of the second conductive type (200) formed in the entirety or the upper portion of the first flat semiconductor layer (112) lying under the columnar silicon layer (113), and the gate electrode (141), by an etching process;

etching the portion of the contact stopper (135) corresponding to the respective contact holes.

21. A semiconductor device comprising:

a first flat semiconductor layer (112) formed on a substrate (110);

a columnar semiconductor layer (113) formed on the first flat semiconductor layer (112);

a first semiconductor layer of a second conductive type (200) formed in a lower

portion of the columnar semiconductor layer (113) and an entirety or an upper portion of the first flat semiconductor layer (112), which constitutes an etched mesa with edges;

a second semiconductor layer of the second conductive type (201) formed in an upper portion of the columnar semiconductor layer (113);

a semiconductor layer of a first conductive type (309) formed between the first semiconductor layer of the second conductive type (200) formed in the lower portion of the columnar semiconductor layer (113), and the second semiconductor layer of the second conductive type (201) formed in the upper portion of the columnar semiconductor layer (113);

a gate insulating film (124) and a gate electrode (141) which are formed around the columnar silicon layer (113);

a first insulating film (303) formed between the gate electrode (141) and the first flat semiconductor layer (112);

a sidewall-shaped second insulating film (133, 134) formed to surround an upper sidewall of the columnar semiconductor layer (113) while contacting an upper surface of the gate electrode (141) and to surround a sidewall of the gate electrode (141) and the first insulating film (303);

a metal-semiconductor compound (152, 153) formed on each of an upper surface of the first semiconductor layer of the second conductive type (200) formed in the entirety or the upper portion of the first flat semiconductor layer (112), and an upper surface of the second semiconductor layer (201) of the second conductive type formed in the upper portion of the columnar semiconductor layer (113),

wherein the first insulating film (303) formed between the gate electrode (141) and the first flat semiconductor layer (112) has a thickness larger than that of the gate insulating film (124) formed around the columnar semiconductor layer (113),

wherein the sum of the half length of the columnar semiconductor layer (113), the thickness of the gate insulating film (124), the width of the gate electrode (141a) and the width of the second insulating film (133) covering the sidewall of the gate electrode (141a) with these layers being abutted with the side wall of one layer abutting the side wall of the

next, is smaller than the length between the centre of the columnar semiconductor layer (113) and the edge of the first semiconductor layer of a second conductive type (200) in the mesa.