BASIC CELL ARCHITECTURE FOR MASK PROGRAMMABLE GATE ARRAY

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ABSTRACT OF THE DISCLOSURE

A highly efficient CMOS cell structure for use in a metal mask programmable gate array, such as a sea-of-gates type gate array, is disclosed herein. In a basic cell, in accordance with one embodiment of the invention, three or more sizes of N-channel transistors and three or more sizes of P-channel transistors are used. The larger size transistors are incorporated in a drive section of a cell, while the smaller size transistors are incorporated in each compute section of a cell. The particular transistors in the compute and drive sections and the arrangements of the compute and drive sections provide a highly efficient use of silicon real estate while enabling the formation of a wide variety of macrocells to be formed.

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FIG. 2.