CLAIMS

1. A phase change memory device, comprising:

a phase change memory material within an electrically insulating wall, wherein the phase change memory material is configured to store multiple data bits;

a first heater terminal in the electrically insulating wall, wherein the first heater terminal is configured to control the relative volumes of an amorphous phase and a crystalline phase of the phase change memory material in an electrical read path;

a first read terminal and a second read terminal, each having a topmost surface and a bottommost surface, in the electrically insulating wall configured to form the electrical read path between the two read terminals that crosses the first heater terminal, wherein the topmost surface and the bottommost surface of the first read terminal are horizontally aligned with a topmost surface and a bottommost surface of the first heater terminal, respectively, and wherein the first and second read terminals have a substantially consistent width from the topmost surfaces to the bottommost surfaces; and

a second heater terminal in the electrically insulating wall, wherein the second heater terminal is separated from the first heater terminal by a thickness of the phase change memory material, and wherein the topmost surface and the bottommost surface of the second read terminal are horizontally aligned with a topmost surface and a bottommost surface of the second heater terminal, respectively.

2. The phase change memory device of claim 1, wherein the second heater terminal is opposite the first heater terminal, and wherein each of the first and second read terminals has a surface coplanar with an inner surface of the electrically insulating wall.

3. The phase change memory device of claim 1, wherein at least a portion of the phase change memory material is in the crystalline phase.

4. The phase change memory device of claim 3, wherein at least a portion of the phase change memory material is in the amorphous phase.

5. The phase change memory device of claim 4, wherein the amorphous phase of the phase change memory material is in the shape of a hemisphere adjoining the first heater terminal.

6. The phase change memory device of claim 4, wherein the phase change memory material has dimensions in a range of about 50 nm (length) X 50 nm (width) X 50 nm (height) to about 250 nm (length) X 250 nm (width) X 100 nm (height).

7. The phase change memory device of claim 4, wherein the amorphous phase of the phase change memory material includes a first hemisphere adjoining the first heater terminal and a second hemisphere adjoining a second heater terminal.

8. The phase change memory device of claim 7, wherein the first read terminal directly contacts a top surface of the phase change memory material and the second read terminal directly contacts a bottom surface of the phase change memory material.

9. A phase change memory device, comprising:

a phase change memory material within an electrically insulating wall;

two heater terminals in the electrically insulating wall, wherein the heater terminals are on opposite sides of the phase change memory material such that the phase change memory material stores multiple data bits through control of relative volumes of an amorphous phase and a crystalline phase of the phase change memory material in an electrical read path; and

two read terminals in the electrically insulating wall, wherein the read terminals are on opposite sides of the two heater terminals and configured to form the electrical read path, and wherein the two read terminals have the same thickness as the electrically insulating wall, wherein the two heater terminals have a width or diameter less than 40 nanometers (nm), and the two read terminals have a width or diameter greater than 40 nanometers (nm).

10. The phase change memory device of claim 9, wherein the two read terminals are located along the same side of the electrically insulating wall.

11. The phase change memory device of claim 9, wherein the two heater terminals have a width or diameter in a range of about 10 nanometers (nm) to about 30 nm, and the two read terminals have a width or diameter in a range of about 50 nm to about 90 nm

12. The phase change memory device of claim 9, wherein the two heater terminals are made of a material selected from the group consisting of titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), titanium silicide (TiSi), cobalt silicide (CoSi), nickel silicide (NiSi), titanium carbide (TiC), tantalum carbide (TaC), tungsten (W), cobalt (Co), platinum (Pt), palladium (Pd), or tantalum (Ta), and combinations thereof.

13. The phase change memory device of claim 12, wherein the phase change memory material is $Ge_2Sb_2Te_5$ (GST).

14. A method of forming a phase change memory device, comprising:

forming a base plate layer on a substrate;

forming a first read terminal and a first heater terminal in the base plate layer;

forming a patterned phase change memory material having a first phase on the base plate layer;

forming an encapsulation layer on the patterned phase change memory material;

forming a second read terminal having a topmost surface and a bottommost surface in the encapsulation layer, wherein the second read terminal is in electrical contact with the patterned phase change memory material, wherein the phase change memory device is configured to have four or more memory states through control of relative volumes of an amorphous phase and a crystalline phase of the phase change memory material in an electrical read path between the first read terminal and the second read terminal that crosses the first heater terminal, wherein a topmost surface and a bottommost surface of the first read terminal are horizontally aligned with a topmost surface and a bottommost surface of the first heater terminal, respectively, and wherein the first and second read terminals have a substantially consistent width from the topmost surfaces to the bottommost surfaces; and

forming a second heater terminal in the encapsulation layer, wherein the second heater terminal is separated from the first heater terminal by a thickness of the phase change memory material, and wherein the topmost surface and the bottommost surface of the second read terminal are horizontally aligned with a topmost surface and a bottommost surface of the second heater terminal, respectively.

15. The method of claim 14, further comprising forming a second heater terminal in the encapsulation layer, wherein the two heater terminals have a width or diameter less than 40 nanometers (nm), and the two read terminals have a width or diameter greater than 40 nanometers (nm).

16. The method of claim 15, wherein the phase change memory material is $Ge_2Sb_2Te_5$ (GST).

17. The method of claim 16, wherein at least a portion of the phase change memory material is in a crystalline phase.

18. The method of claim 17, wherein the two heater terminals are separated by a height of the phase change memory material within an electrically insulating wall in a range of about 50 nm to about 100 nm, and wherein each of the first read terminal and the first heater terminal has a surface coplanar with an inner surface of the base plate layer.