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Abstract

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A first phase locked loop (12) generates a first timing signal (on 17) at a first horizontal synchronizing frequency ($1f_H$) corresponding to a horizontal synchronizing component (on 13) in a video signal (on 11). A converter circuit (56) derives from the first timing signal (on 17) a second timing signal (on 61), having a second frequency ($2f_H$) at a multiple of the first frequency and subject to a variation in frequency at a rate corresponding to the first frequency. A second phase locked loop (62) receives the second timing signal (on 61), which can be asymmetric within the period of the first timing signal (on 17), and a feedback signal (on 73) in accordance with the second frequency, and includes a controllable oscillator (66) for generating a smooth horizontal synchronizing signal (on 67) at the second frequency. The second phase locked loop has a characteristic loop response, determined by a low pass filter (63), preventing the voltage controlled oscillator (66) from changing frequency as fast as the rate of variation of the second timing signal (on 61). This drives the error signal for the controllable oscillator (66) toward an average value, resulting in a corrected, symmetric synchronizing signal at the second frequency. A horizontal output deflection stage (68) may be coupled to the second phase locked loop (62) for synchronized horizontal scanning in accordance with the second frequency. No additional signal processing circuitry is needed to correct the symmetry of the first timing signal generated by the first phase locked loop or the symmetry of the second timing signal derived by the converter.

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Reference Indicia Are From Fig. 4

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