FIG. 1

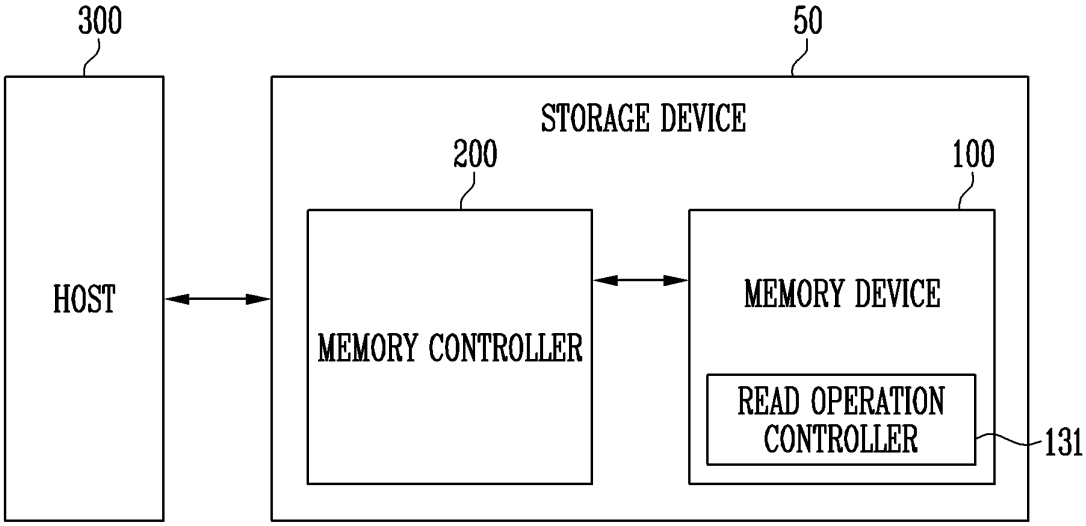

300
50
STORAGE DEVICE
200
100
HOST
MEMORY CONTROLLER
MEMORY DEVICE
READ OPERATION CONTROLLER
131

FIG. 2

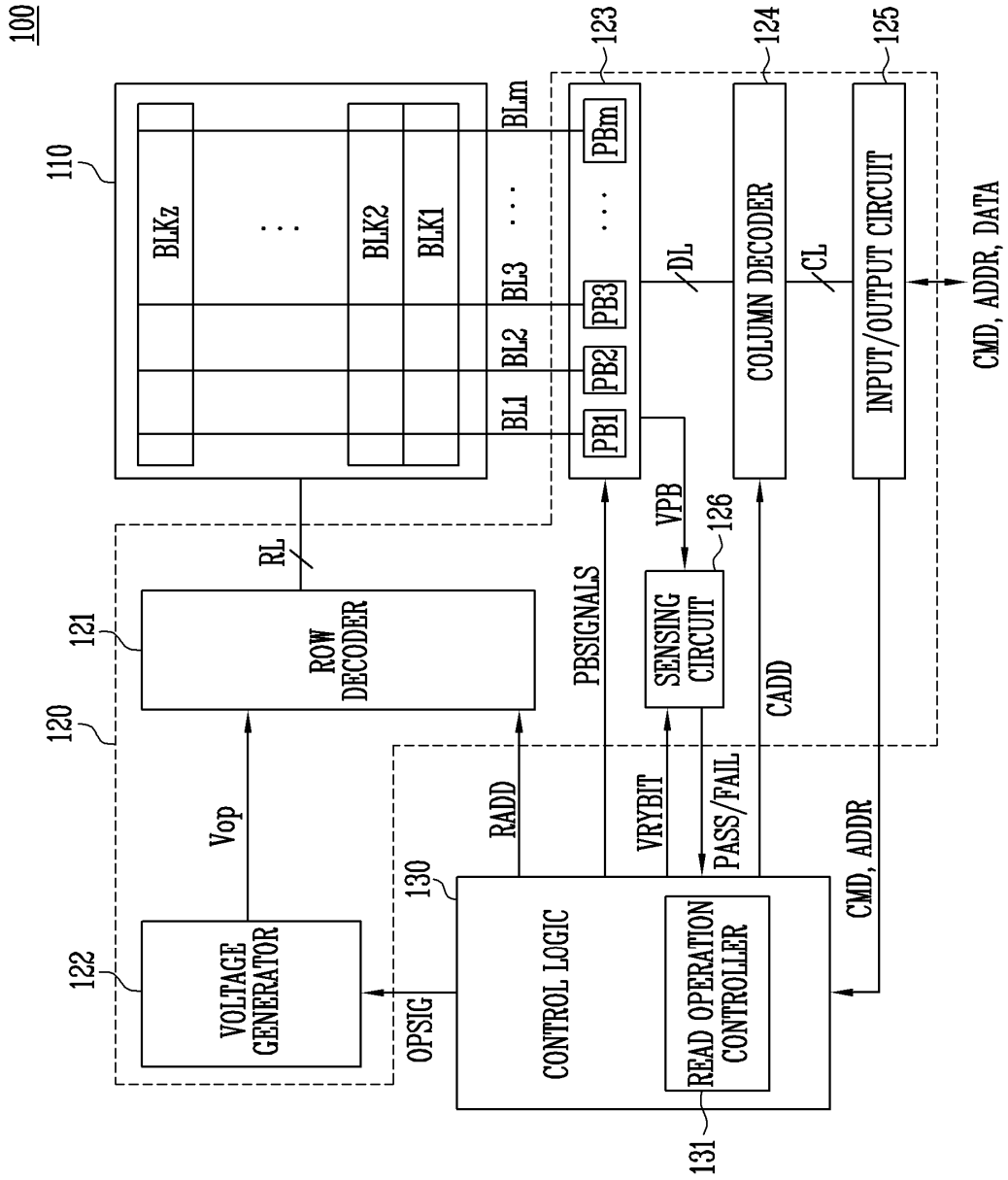

100
110
BLKz
BLK2
BLK1
BLm
BL3
BL2
BL1
123
PBm
PB3
PB2
PB1
124
COLUMN DECODER
125
INPUT/OUTPUT CIRCUIT
CMD, ADDR, DATA
DL
CL
RL
121
ROW DECODER
PBSIGNALS
VPB
126
SENSING CIRCUIT
120
Vop
RADD
VRYBIT
PASS/FAIL
CADD
130
CONTROL LOGIC
CMD, ADDR
122
VOLTAGE GENERATOR
OPSIG
READ OPERATION CONTROLLER
131

FIG. 3

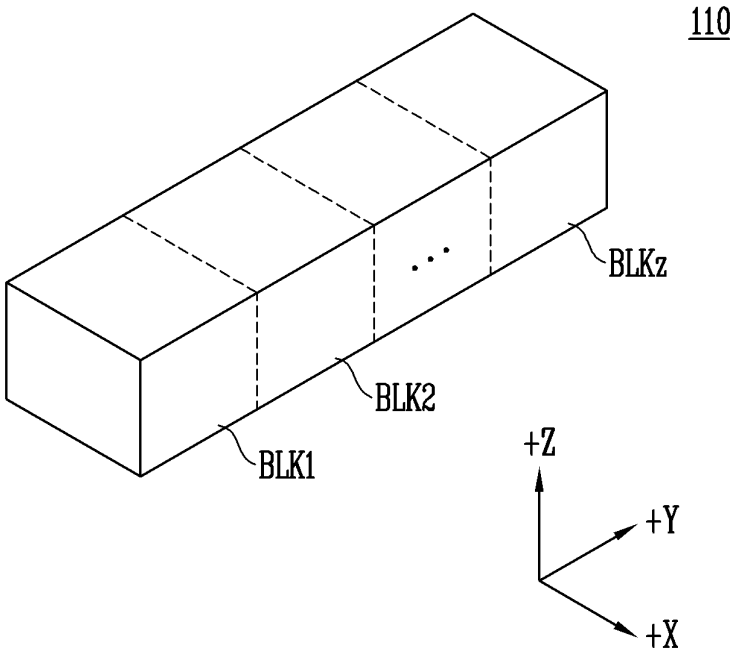


FIG. 4

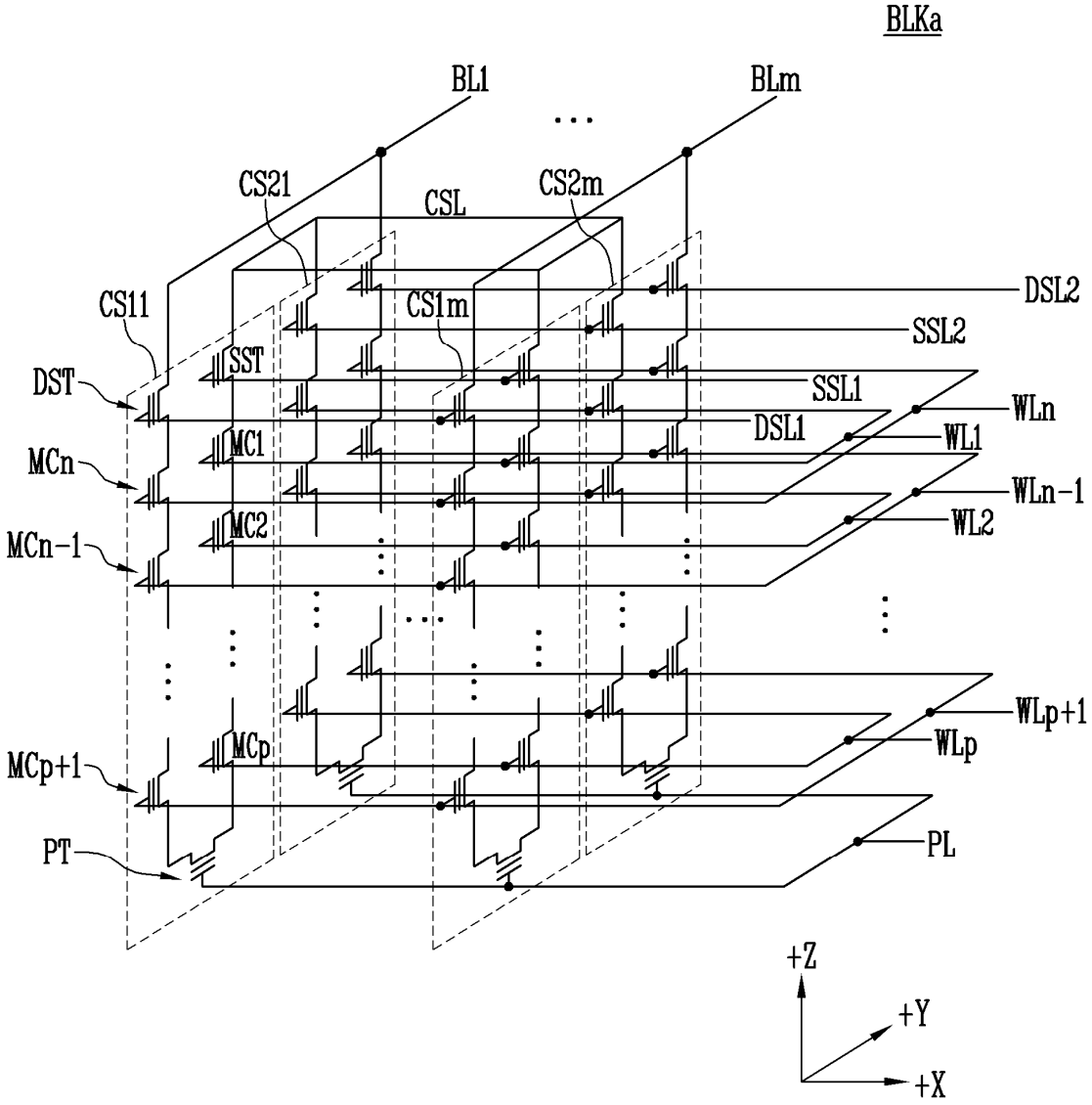

BLKa
BL1
BLm
CS21
CSL
CS2m
CS11
CS1m
DSL2
SSL2
SST
DST
SSL1
WLn
DSL1
WL1
MC1
MCn
WLn-1
WL2
MC2
MCn-1
WLp+1
WLp
MCp
MCp+1
PT
PL
+Z
+Y
+X

FIG. 5

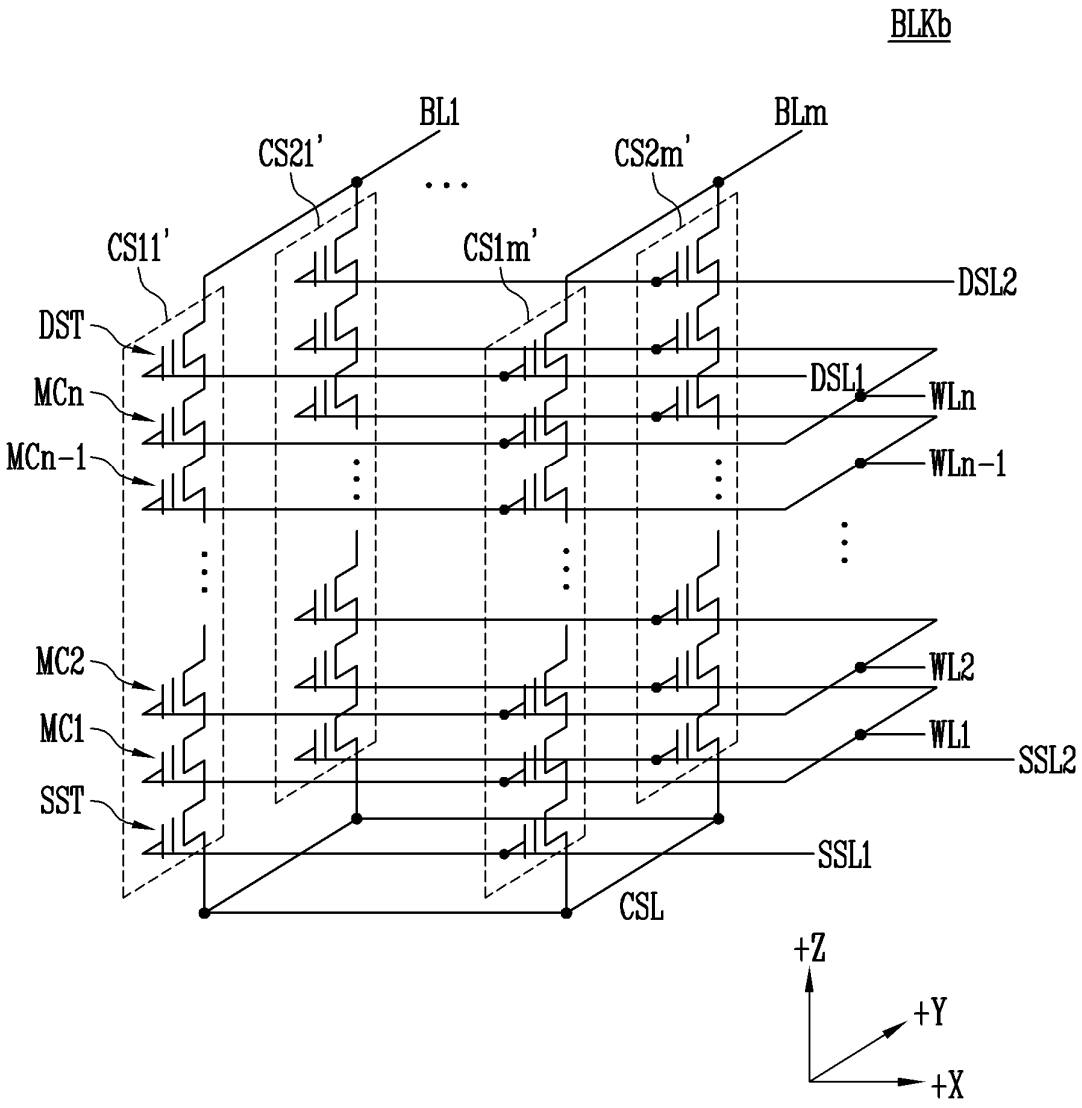

BLKb
BL1
BLm
CS21'
CS2m'
CS11'
CS1m'
DSL2
DST
DSL1
MCn
WLn
MCn-1
WLn-1
MC2
WL2
MC1
WL1
SSL2
SST
SSL1
CSL
+Z
+Y
+X

FIG. 6

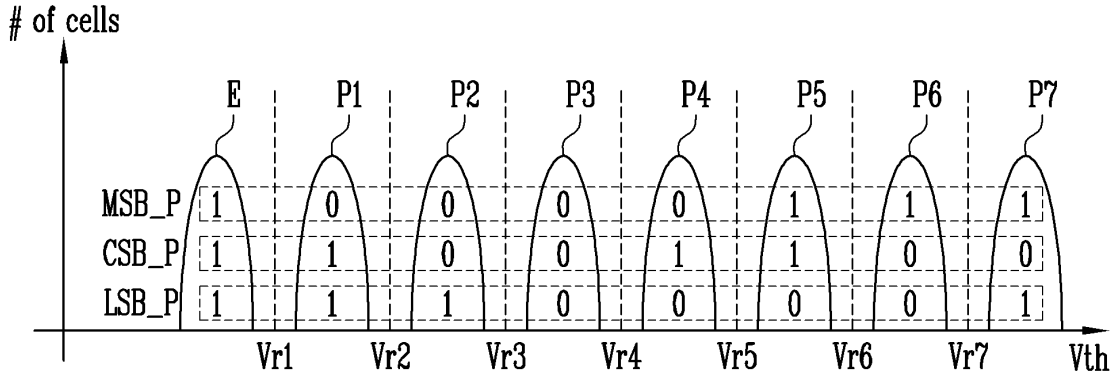

# of cells
E
P1
P2
P3
P4
P5
P6
P7
MSB_P
CSB_P
LSB_P
1 0 0 0 0 1 1 1
1 1 0 0 1 1 0 0
1 1 1 0 0 0 0 1
Vr1
Vr2
Vr3
Vr4
Vr5
Vr6
Vr7
Vth

FIG. 7

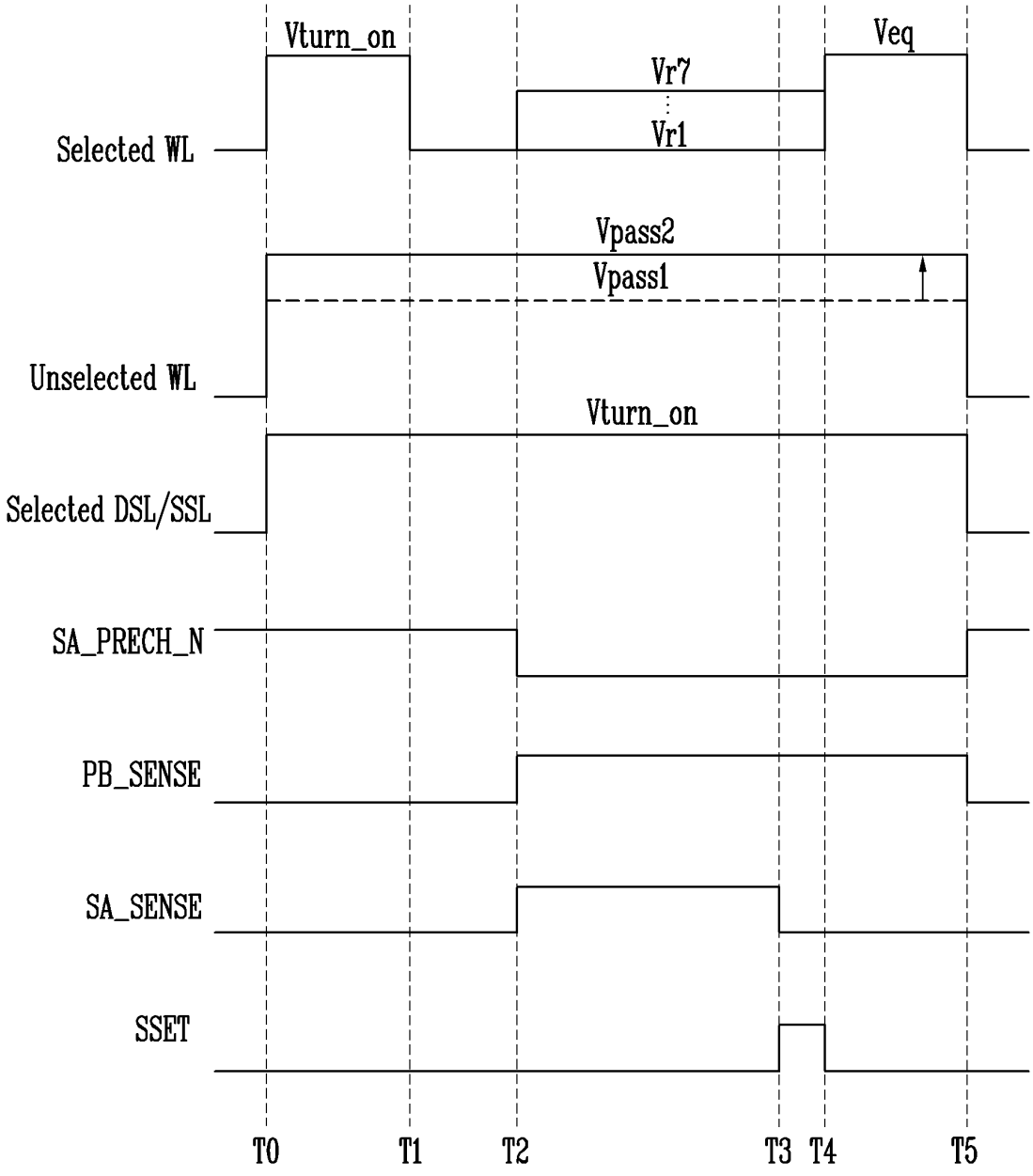

Vturn_on
Veq
Vr7
Vr1
Selected WL
Vpass2
Vpass1
Unselected WL
Vturn_on
Selected DSL/SSL
SA_PRECH_N
PB_SENSE
SA_SENSE
SSET
T0
T1
T2
T3
T4
T5

FIG. 8

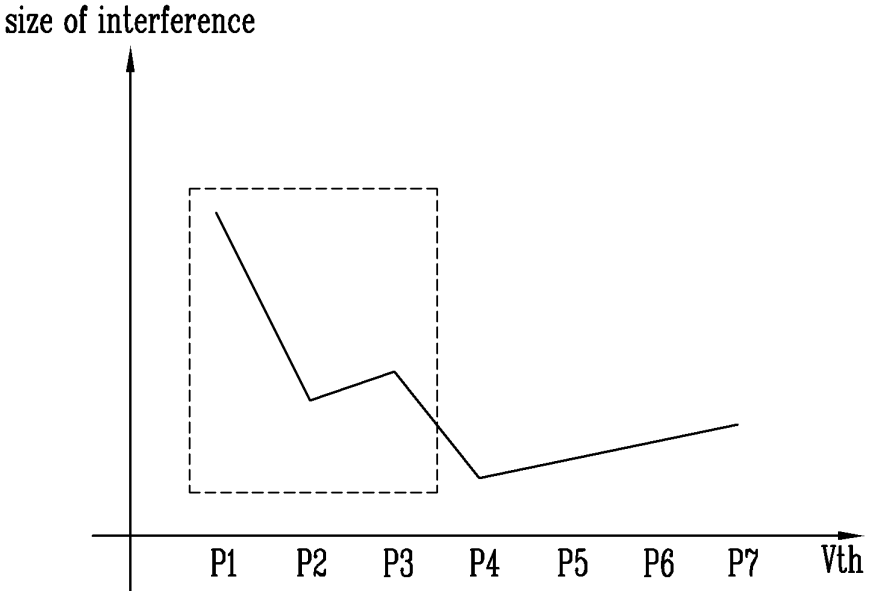


FIG. 9

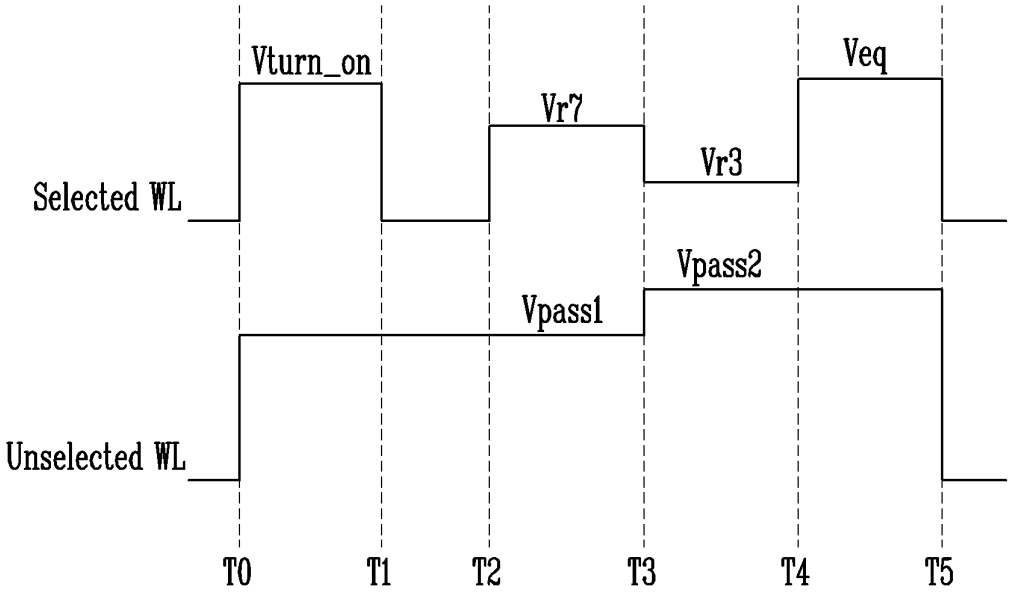

Vturn_on
Vr7
Vr3
Veq
Selected WL
Vpass2
Vpass1
Unselected WL
T0
T1
T2
T3
T4
T5

FIG. 10

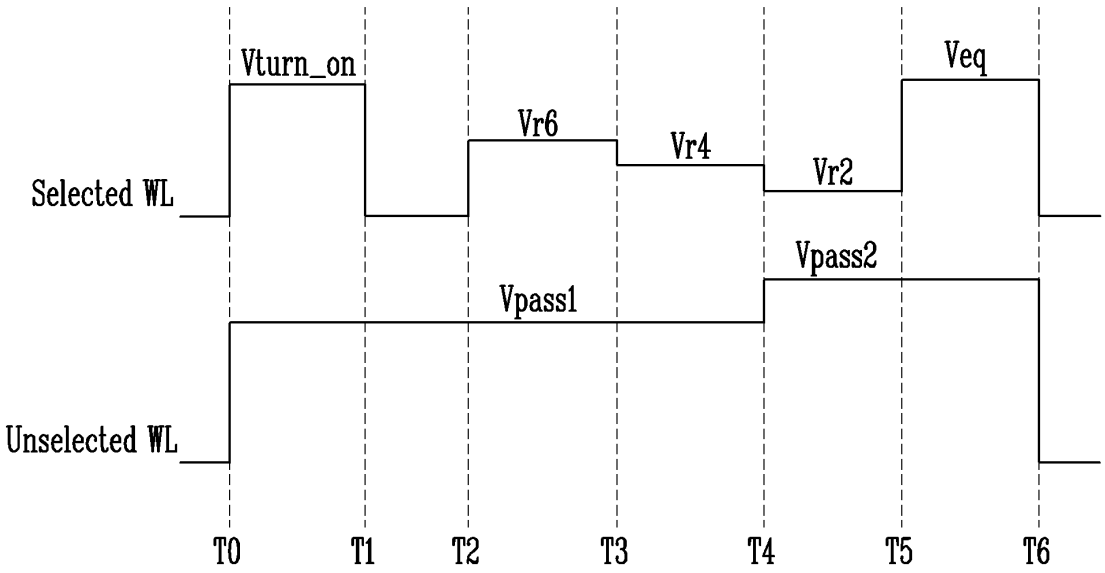

Vturn_on
Vr6
Vr4
Vr2
Veq
Selected WL
Vpass2
Vpass1
Unselected WL
T0
T1
T2
T3
T4
T5
T6

FIG. 11

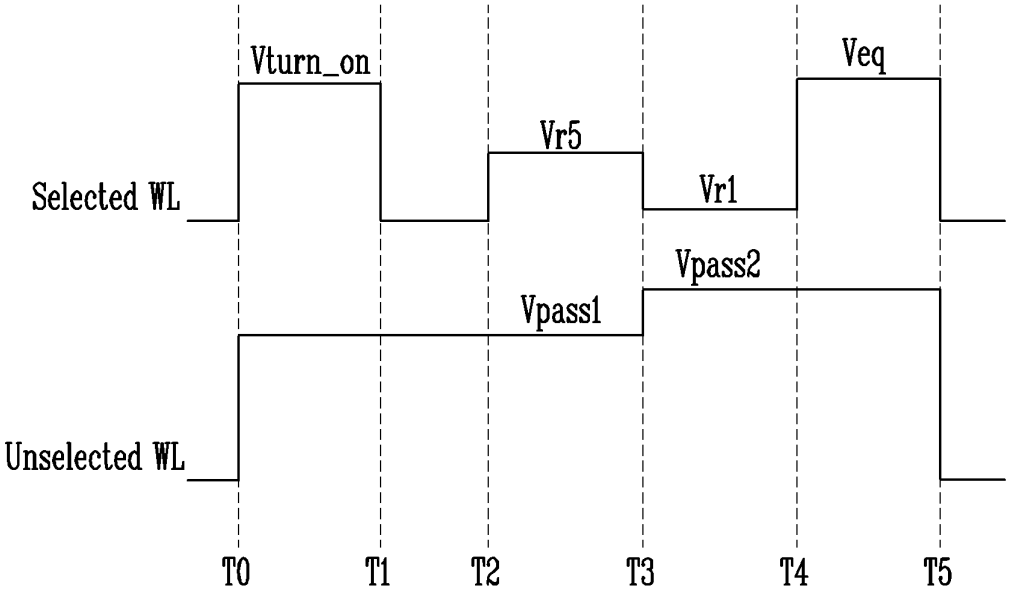

Vturn_on
Veq
Vr5
Selected WL
Vr1
Vpass2
Vpass1
Unselected WL
T0
T1
T2
T3
T4
T5

FIG. 12

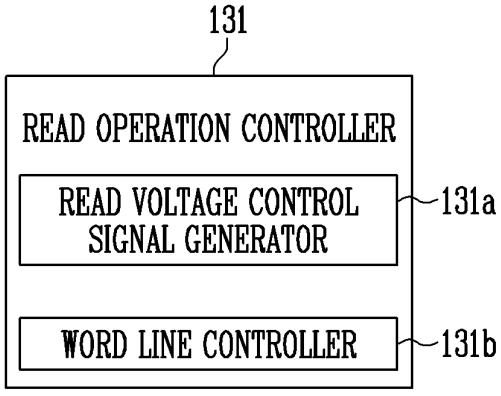

131
READ OPERATION CONTROLLER
READ VOLTAGE CONTROL SIGNAL GENERATOR
131a
WORD LINE CONTROLLER
131b

FIG. 13

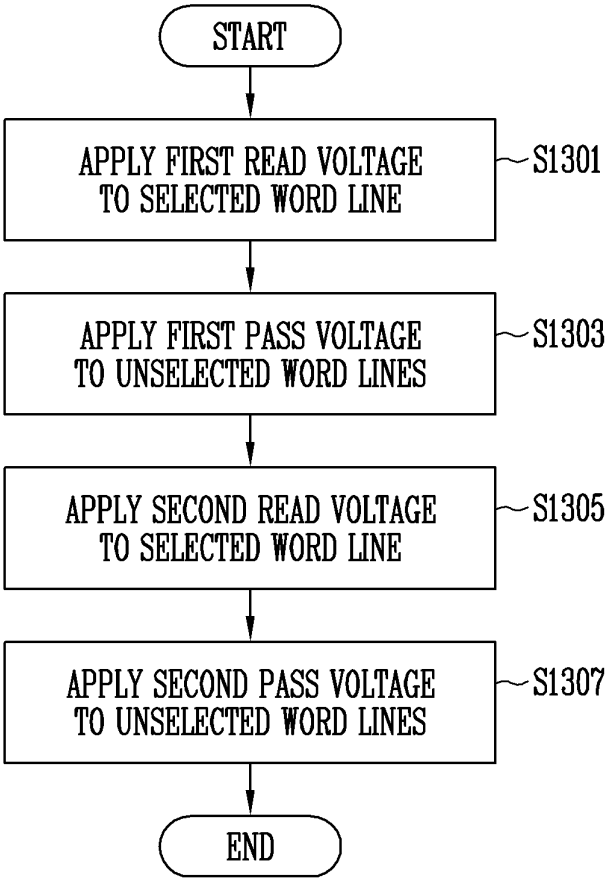

START
APPLY FIRST READ VOLTAGE TO SELECTED WORD LINE
S1301
APPLY FIRST PASS VOLTAGE TO UNSELECTED WORD LINES
S1303
APPLY SECOND READ VOLTAGE TO SELECTED WORD LINE
S1305
APPLY SECOND PASS VOLTAGE TO UNSELECTED WORD LINES
S1307
END

FIG. 14

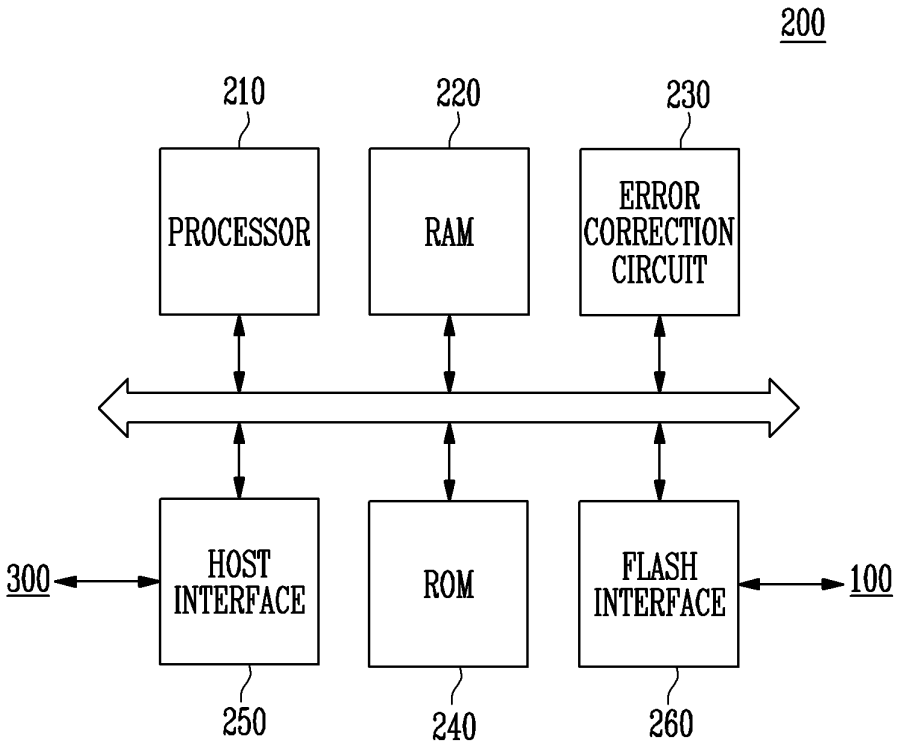

200
210
220
230
PROCESSOR
RAM
ERROR CORRECTION CIRCUIT
300
HOST INTERFACE
ROM
FLASH INTERFACE
100
250
240
260

FIG. 15

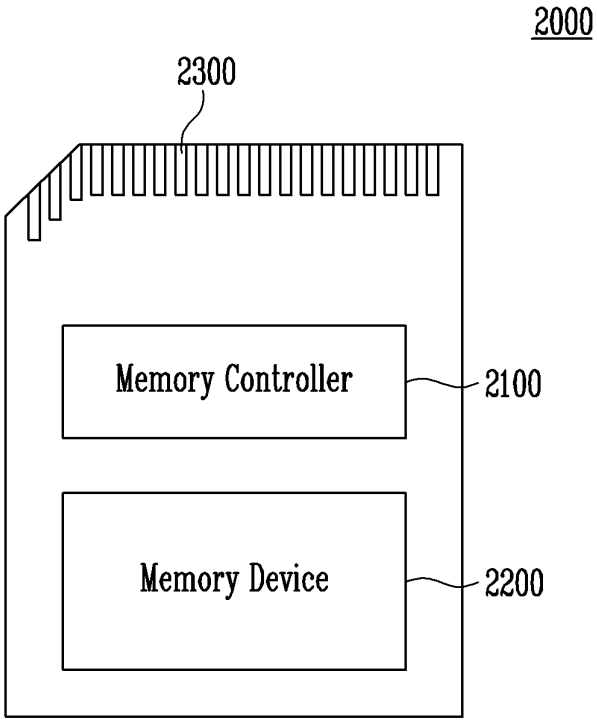


FIG. 16

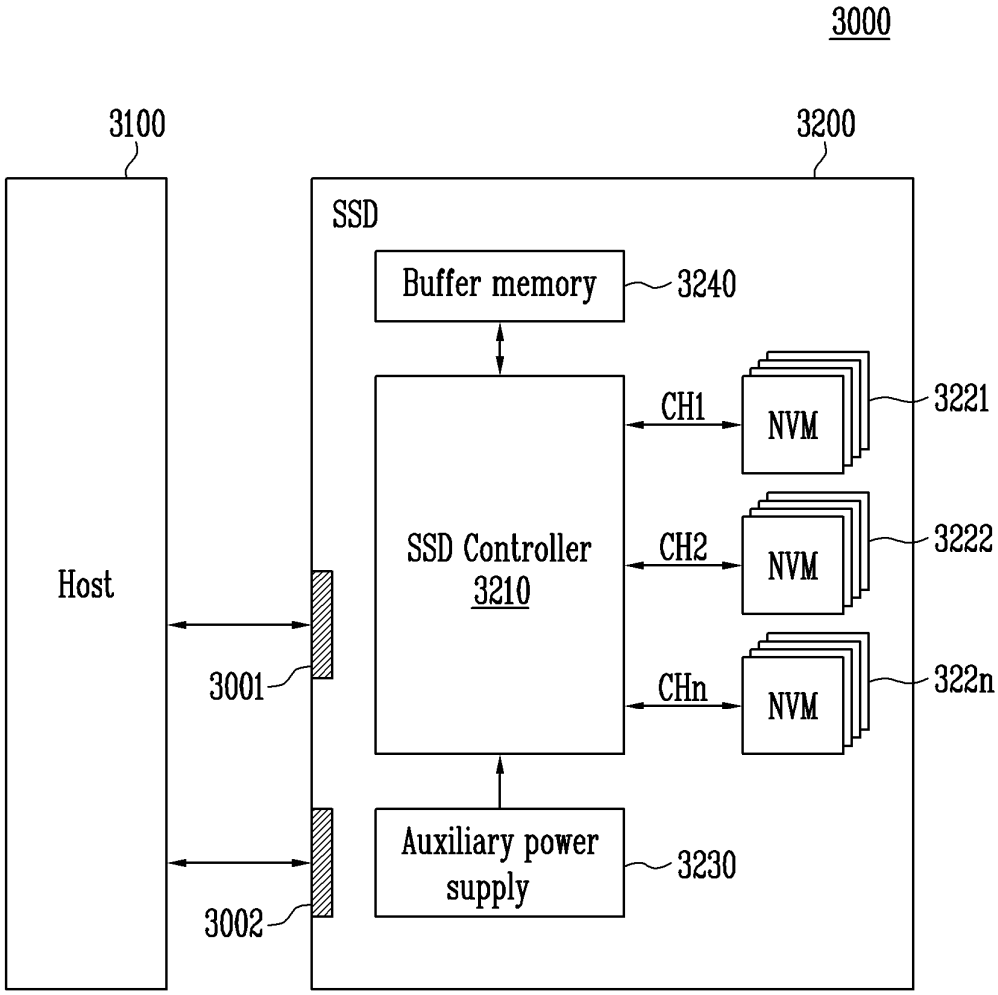
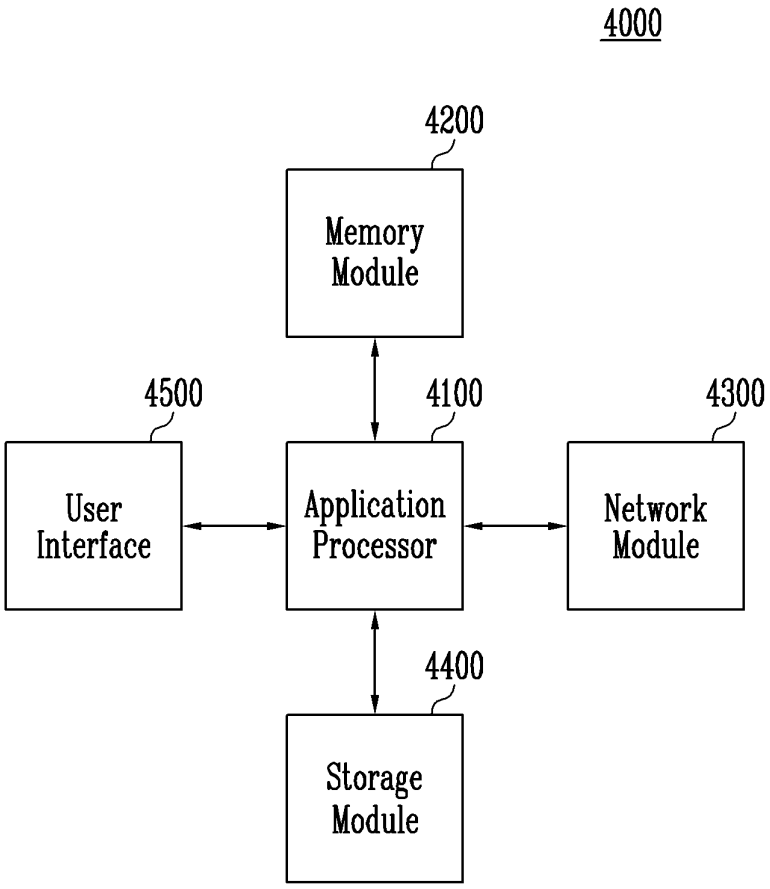

3000
3100
3200
SSD
Buffer memory
3240
SSD Controller
3210
CH1
CH2
CHn
NVM
NVM
NVM
3221
3222
322n
Host
3001
3002
Auxiliary power
supply
3230

FIG. 17


4000
4200
Memory Module
4500
4100
4300
User Interface
Application Processor
Network Module
4400
Storage Module