

There is also a need to provide a process for producing substrates having the abovementioned specifications, that is easy to implement, and compatible with specific donor and/or receiver substrates, for example comprising trapping layers of "Trap Rich" type or doped layers. Indeed, substrates of this type require limited finishing thermal budgets, in particular for smoothing the surface of the active layer on insulator (processes of "Rapid Thermal Annealing" type, as opposed to "Thermal Batch Annealing" type).

These needs are increasingly significant, in particular in the field of systems on chip or SOC which integrate several functions on one the same chip, or in the field of the co-integration of digital components and of radiofrequency components, or else in the field of microsystems integrating for example sensors or accelerometers along with read-out circuits.

An aspect of the present invention provides a process for producing an advanced substrate, comprising the following steps:

- a) Providing a receiver substrate and a donor substrate comprising:
 - A carrier substrate;
 - An active layer made from a single-crystal semiconductor material; and
 - A sacrificial layer made from a material that can be selectively etched with respect to the active layer, the sacrificial layer being interposed between the carrier substrate and the active layer;
 - A silicon oxide layer with a free surface and arranged so that the active layer is interposed between the sacrificial layer and the oxide layer;
- b) Forming a cavity in the oxide layer, the cavity having an opening which lies flush with the free surface so that the oxide layer comprises a first portion having a first thickness e_1 and placed between the cavity and the active layer, and a second portion having a second thickness e_2 greater than the first thickness e_1 , the second portion being placed between the free surface and the active layer;
- c) Forming a polycrystalline silicon filling layer so as to completely fill the cavity and form a continuous and substantially planar second free surface, comprising at least one first polycrystalline silicon surface;
- d) Assembling the receiver substrate and the donor substrate on the second free surface;
- e) Removing the carrier substrate after step d) while preserving the active layer and the sacrificial layer.

According to one embodiment, the process can comprise a step of selectively etching the sacrificial layer while at the same time preserving the active layer, after step e). Moreover, the assembling step d) can comprise a step of bonding by molecular adhesion.

According to one embodiment, the process can also comprise the following steps:

- b0) Forming, before step b) and after step a), a weakened zone in the carrier substrate, the weakened zone being substantially planar and located in the vicinity of the interface between the sacrificial layer and the carrier substrate;
- e0) Fracturing the carrier substrate along the weakened zone, after step d).

Furthermore, the sacrificial layer can be made from a material that can be selectively etched with respect to the material of the carrier substrate. As a result, the remainder of the carrier substrate placed on the sacrificial layer can be selectively etched after the fracturing step e0). The filling layer can also be formed by chemical vapour deposition at a temperature between 150°C and 250°C.

According to one embodiment, the single-crystal silicon active layer can be produced by epitaxy. Moreover, the active layer preserved after step e) can be locally thinned so as to locally reduce the thickness of the active layer.

According to one embodiment, the filling layer can cover the silicon oxide layer. Furthermore, an additional polycrystalline silicon layer can be formed on the second portion of the silicon oxide layer, said additional layer preferentially having a thickness e' of between 1 and 1000 nm, the second free surface formed following step c) being, in this case, entirely made from polycrystalline silicon.

Moreover, step c) can comprise thinning of the filling layer and/or of the oxide layer so that the second free surface also comprises a second silicon oxide surface.

Another aspect of the present invention provides an advanced substrate comprising:

- A receiver substrate;
- An active layer made from single-crystal semiconductor material; and
- An electrically insulating silicon oxide layer interposed between the active layer and the receiver substrate;

characterized in that it comprises a polycrystalline silicon layer placed on the receiver substrate, the polycrystalline silicon layer being coated with the electrically insulating layer so as to define a first portion of the electrically insulating layer having a first thickness e_1 and interposed between the polycrystalline silicon layer and the active layer, and a second portion of the electrically insulating layer having a second thickness e_2 greater than the

CLAIMS

1. Process for producing an advanced substrate, comprising the following steps:
 - a) Providing a receiver substrate and a donor substrate comprising:
 - A carrier substrate;
 - 5 - An active layer made from a single-crystal semiconductor material; and
 - A sacrificial layer made from a material that can be selectively etched with respect to the active layer, the sacrificial layer being interposed between the carrier substrate and the active layer;
 - A silicon oxide layer with a free surface and arranged so that the active layer is
 - 10 interposed between the sacrificial layer and the oxide layer;
 - b) Forming a cavity in the oxide layer, the cavity having an opening which lies flush with the free surface so that the oxide layer comprises a first portion having a first thickness and placed between the cavity and the active layer, and a second portion having a second thickness greater than the first thickness, the second portion being
 - 15 placed between the free surface and the active layer;
 - c) Forming a polycrystalline silicon filling layer so as to completely fill the cavity and form a continuous and substantially planar second free surface, comprising at least one first polycrystalline silicon surface;
 - d) Assembling the receiver substrate and the donor substrate on the second free
 - 20 surface;
 - e) Removing the carrier substrate after step d) while preserving the active layer and the sacrificial layer.
2. Process according to claim 1, comprising a step of selectively etching the sacrificial layer while at the same time preserving the active layer, after step e).
- 25 3. Process according to either of the preceding claims, in which the assembling step d) comprises a step of bonding by molecular adhesion.
4. Process according to one of the preceding claims, comprising the following steps:
 - b0) Forming, before step b) and after step a), a weakened zone in the carrier substrate, the weakened zone being substantially planar and located in the vicinity
 - 30 of the interface between the sacrificial layer and the carrier substrate;
 - e0) Fracturing the carrier substrate along the weakened zone, after step d).
5. Process according to claim 4, in which the carrier substrate is made from a material which can be selectively etched with respect to the material of the sacrificial layer, the process also comprising selectively etching the rest of the carrier substrate placed on the
- 35 sacrificial layer, after the fracturing step e0).

6. Process according to either of claims 4 and 5, in which the filling layer is formed by chemical vapour deposition at a temperature between 150°C and 250°C.
7. Process according to one of the preceding claims, in which the single-crystal silicon active layer is produced by epitaxy.
- 5 8. Process according to one of the preceding claims, in which the filling layer covers the silicon oxide layer.
9. Process according to claim 8, in which a polycrystalline silicon layer is formed on the second portion of the silicon oxide layer, the layer having a thickness of between 1 and 1000 nm, the second free surface formed following step c) being entirely made from polycrystalline silicon.
- 10 10. Process according to one of claims 1 to 8, in which step c) comprises the thinning of the filling layer and/or of the oxide layer so that the second free surface also comprises a second silicon oxide surface.
11. Process according to one of the preceding claims, in which the active layer preserved after step e) is locally thinned so as to locally reduce the thickness of the active layer.
- 15 12. Advanced substrate comprising:
- A receiver substrate;
 - An active layer made from single-crystal semiconductor material; and
 - 20 - An electrically insulating silicon oxide layer interposed between the active layer and the receiver substrate;
- characterized in that it comprises a polycrystalline silicon layer placed on the receiver substrate, the polycrystalline silicon layer being coated with the electrically insulating layer so as to define a first portion of the electrically insulating layer having a first thickness and interposed between the polycrystalline silicon layer and the active layer, and a second portion of the electrically insulating layer having a second thickness greater than the first thickness, the second portion being placed between the receiver substrate and the active layer.
- 25 13. Substrate according to the preceding claim, characterized in that it comprises an additional layer made from polycrystalline silicon, interposed between the receiver substrate and the assembly formed by the electrically insulating layer and the polycrystalline silicon layer.
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14. Substrate according to the preceding claim, characterized in that it comprises an additional electrically insulating layer interposed between the additional layer and the receiver substrate.
15. Substrate according to the preceding claim, characterized in that the receiver
5 substrate comprises an epitaxially grown and doped layer, configured to form microelectronic components in said epitaxially grown layer.
16. Substrate according to either of claims 14 and 15, characterized in that the receiver substrate comprises integrated circuits.