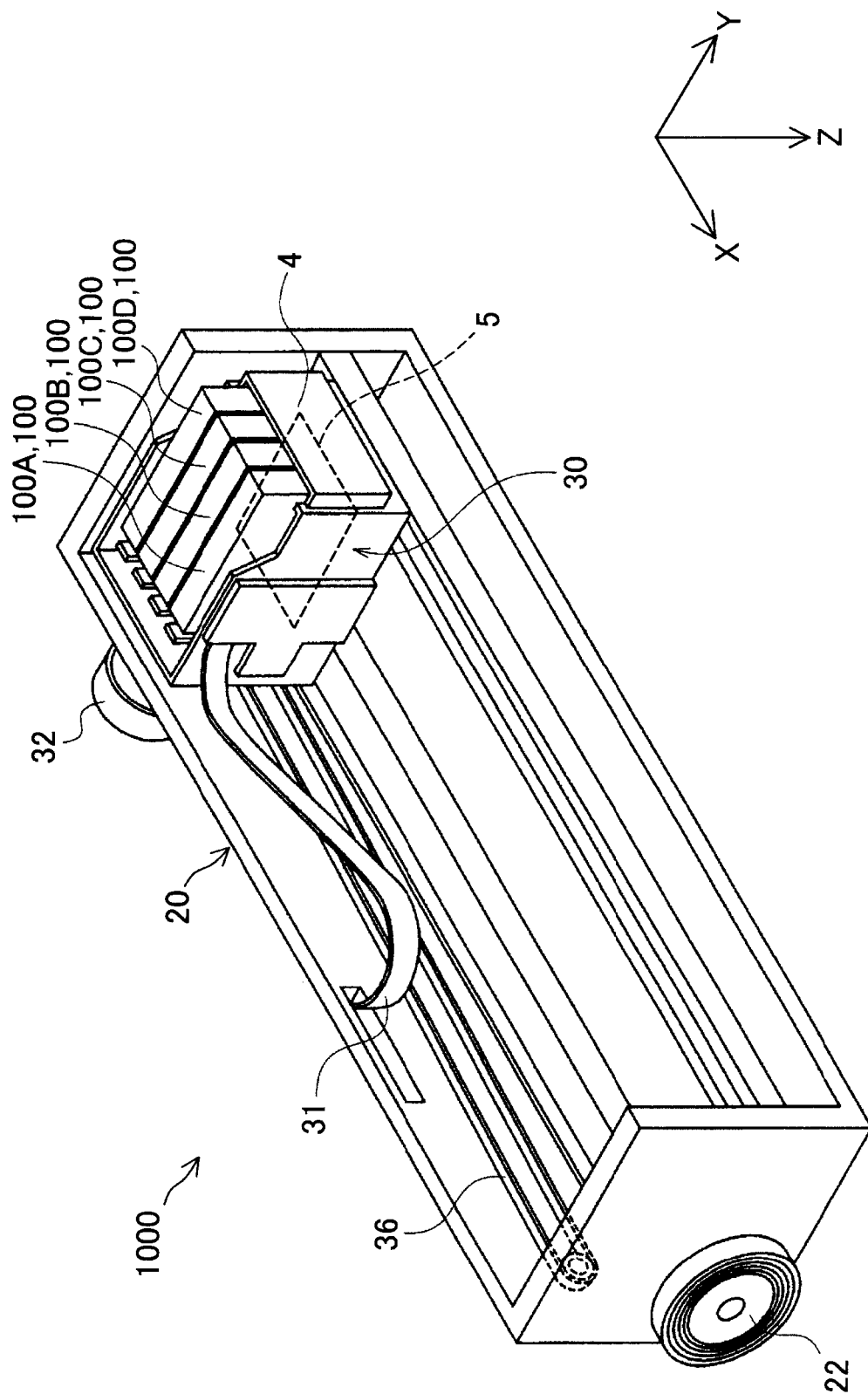
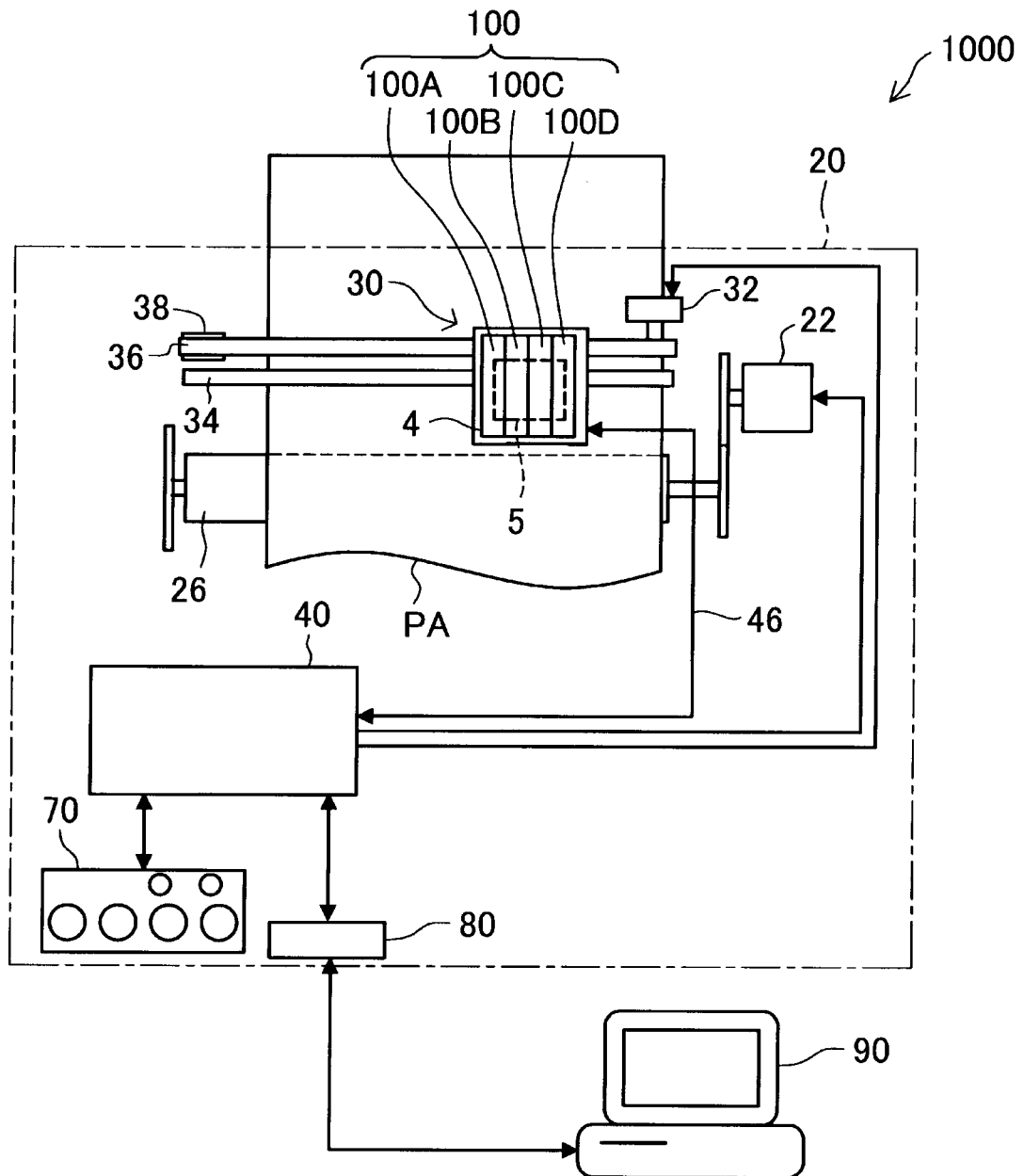


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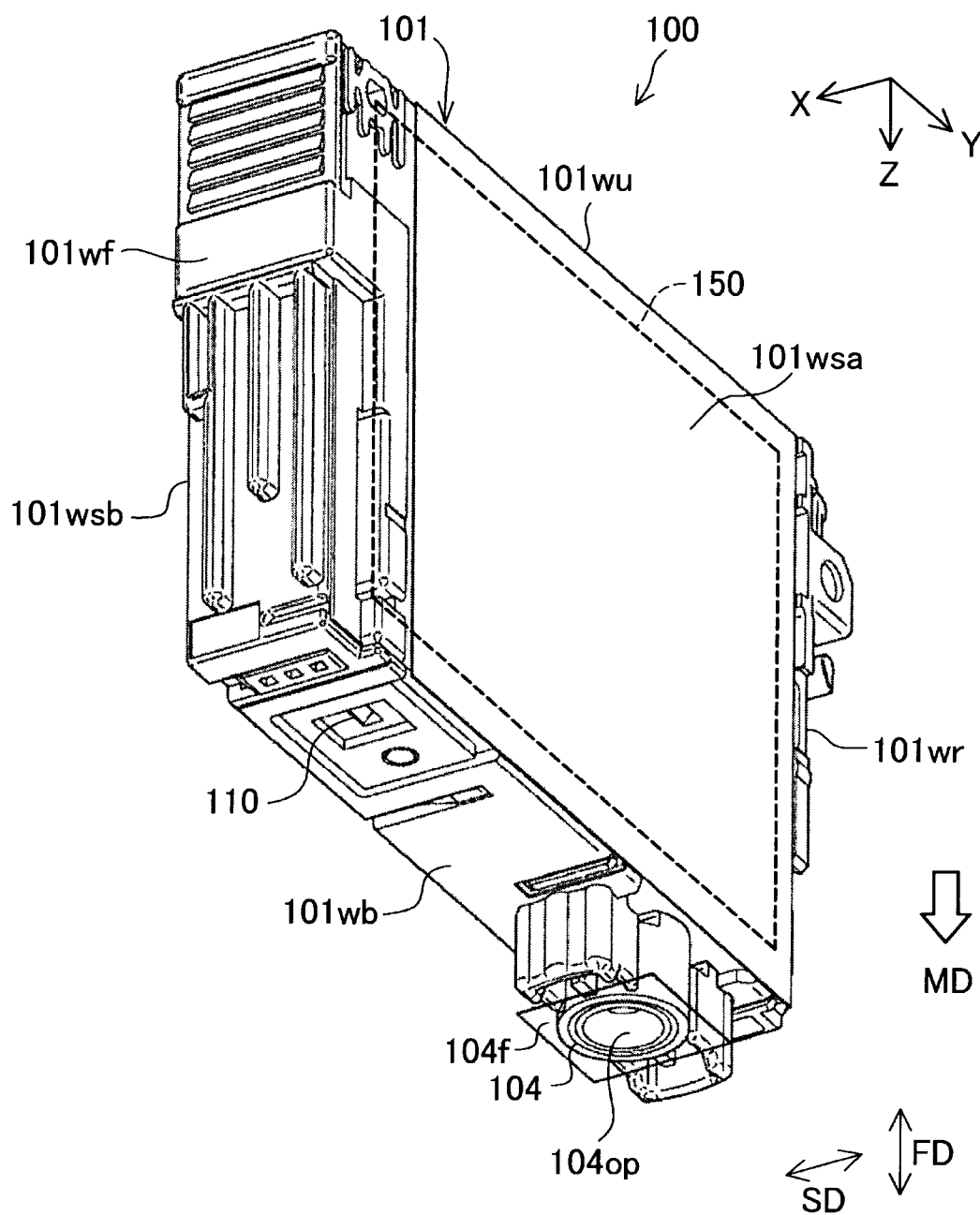
FIG. 1

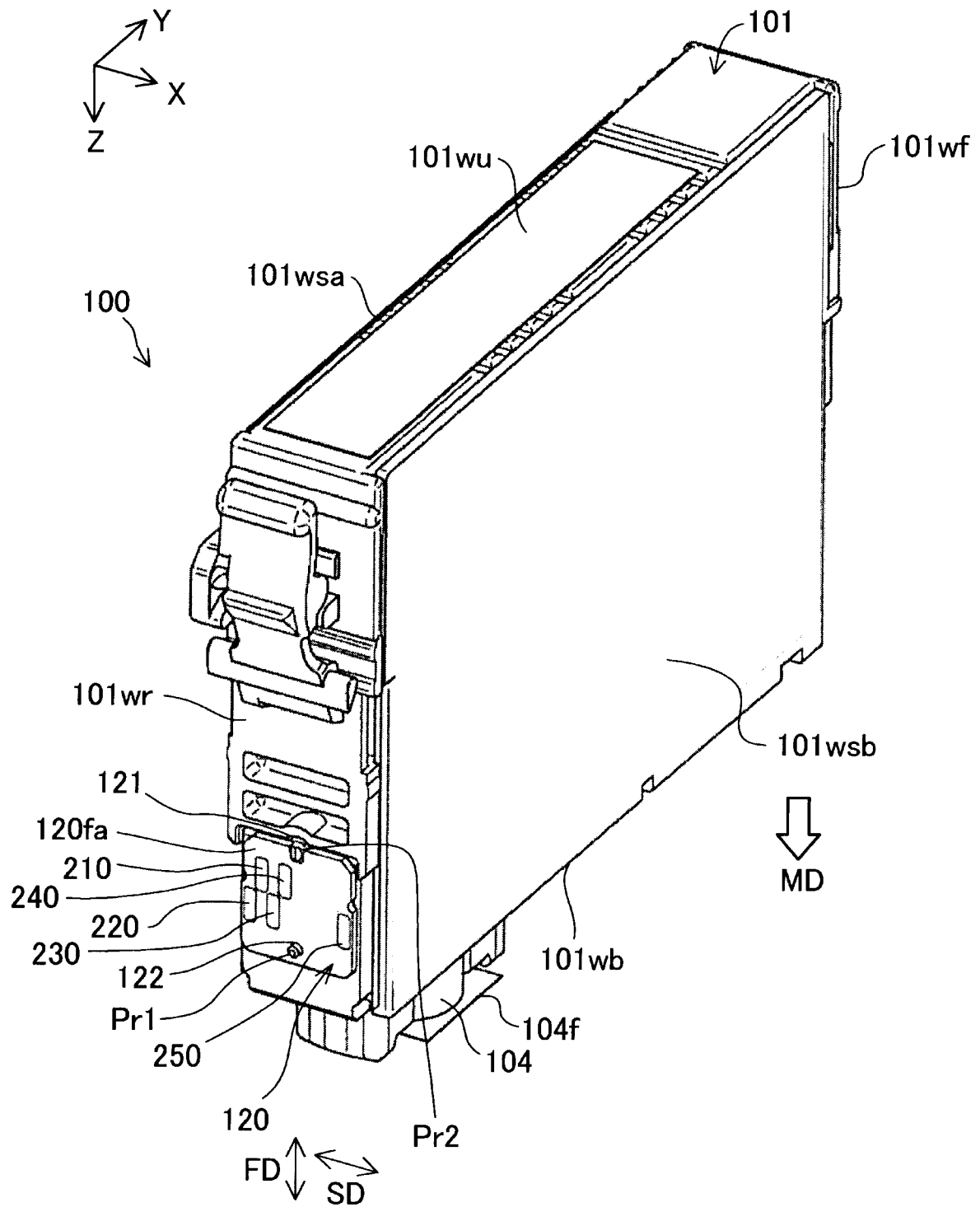




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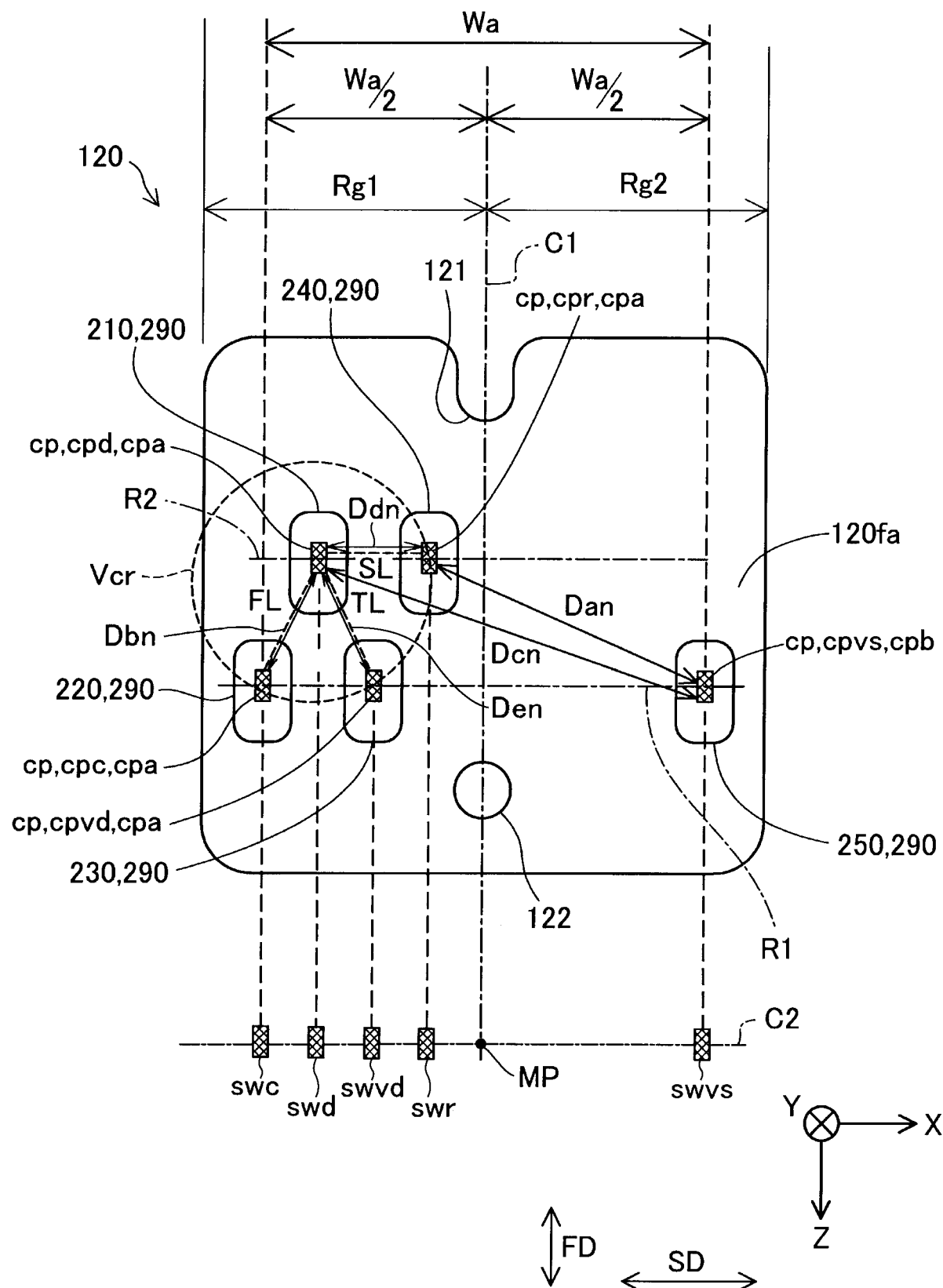
FIG. 3





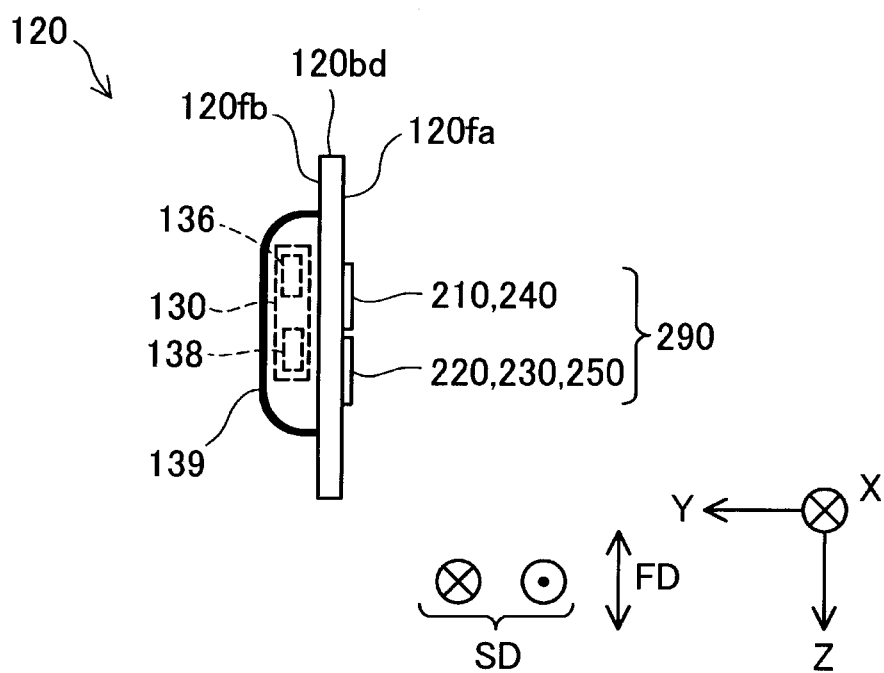
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FIG. 5

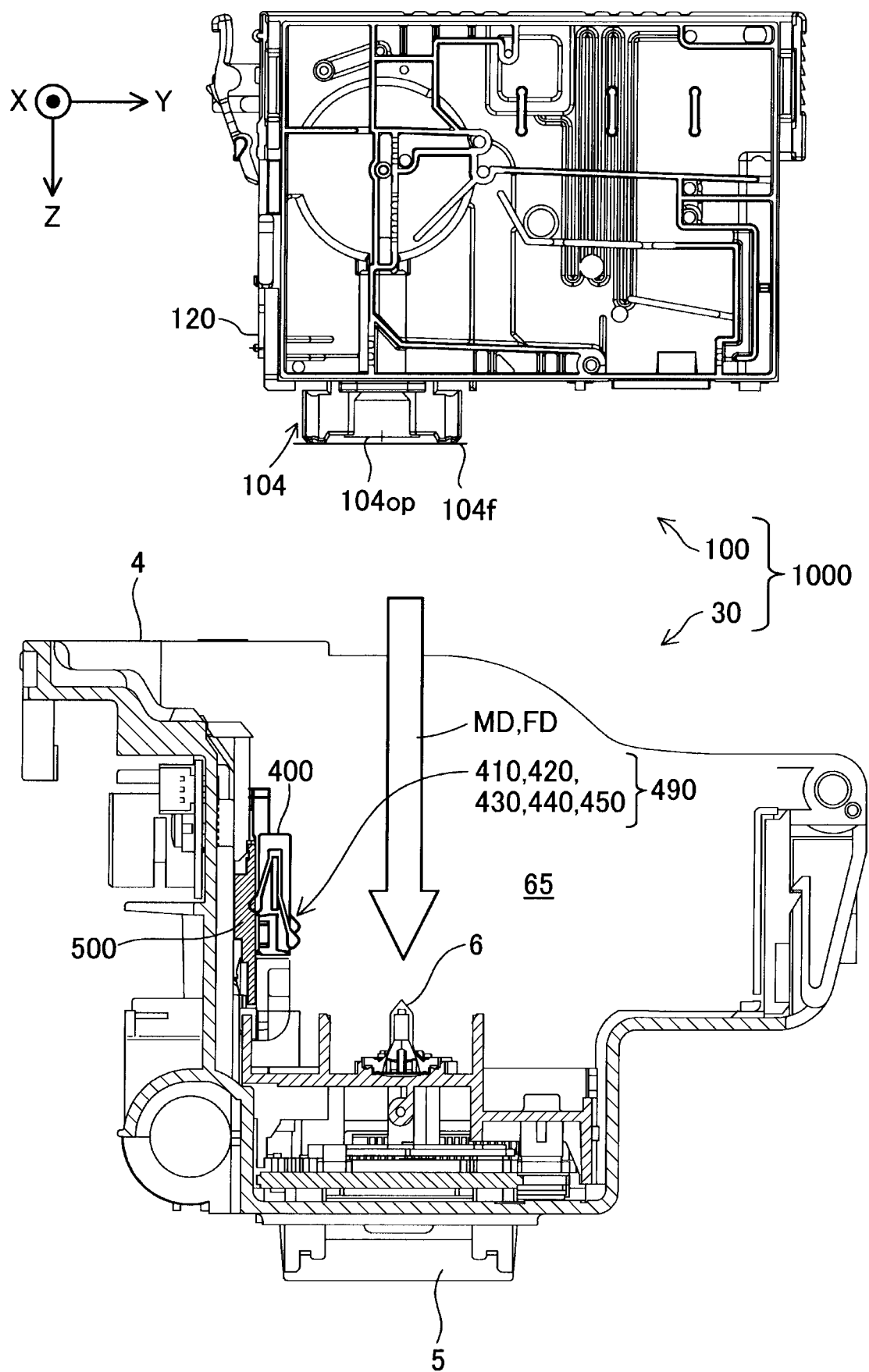


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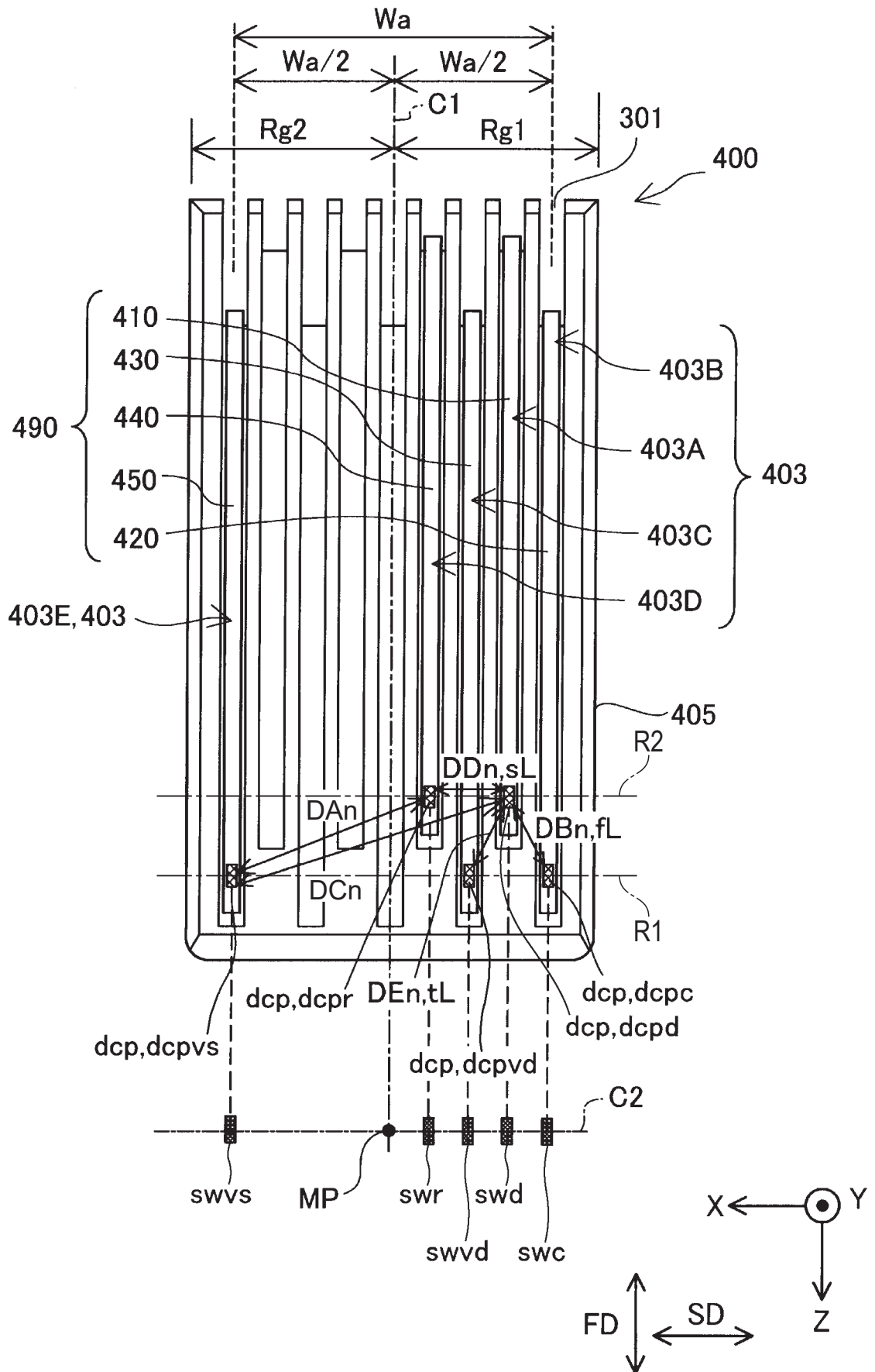
FIG. 6



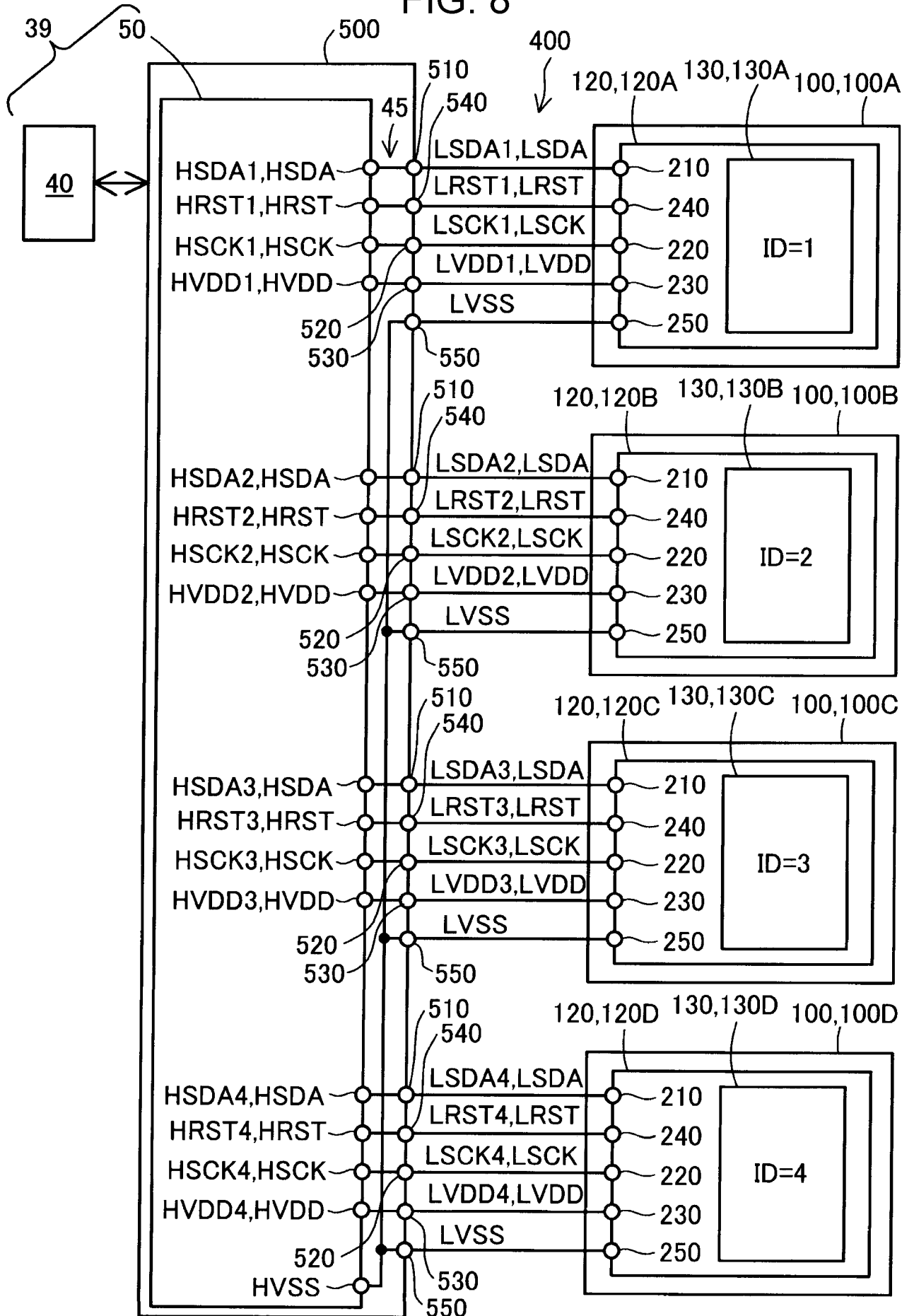
7/61
FIG. 7A



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FIG. 7B

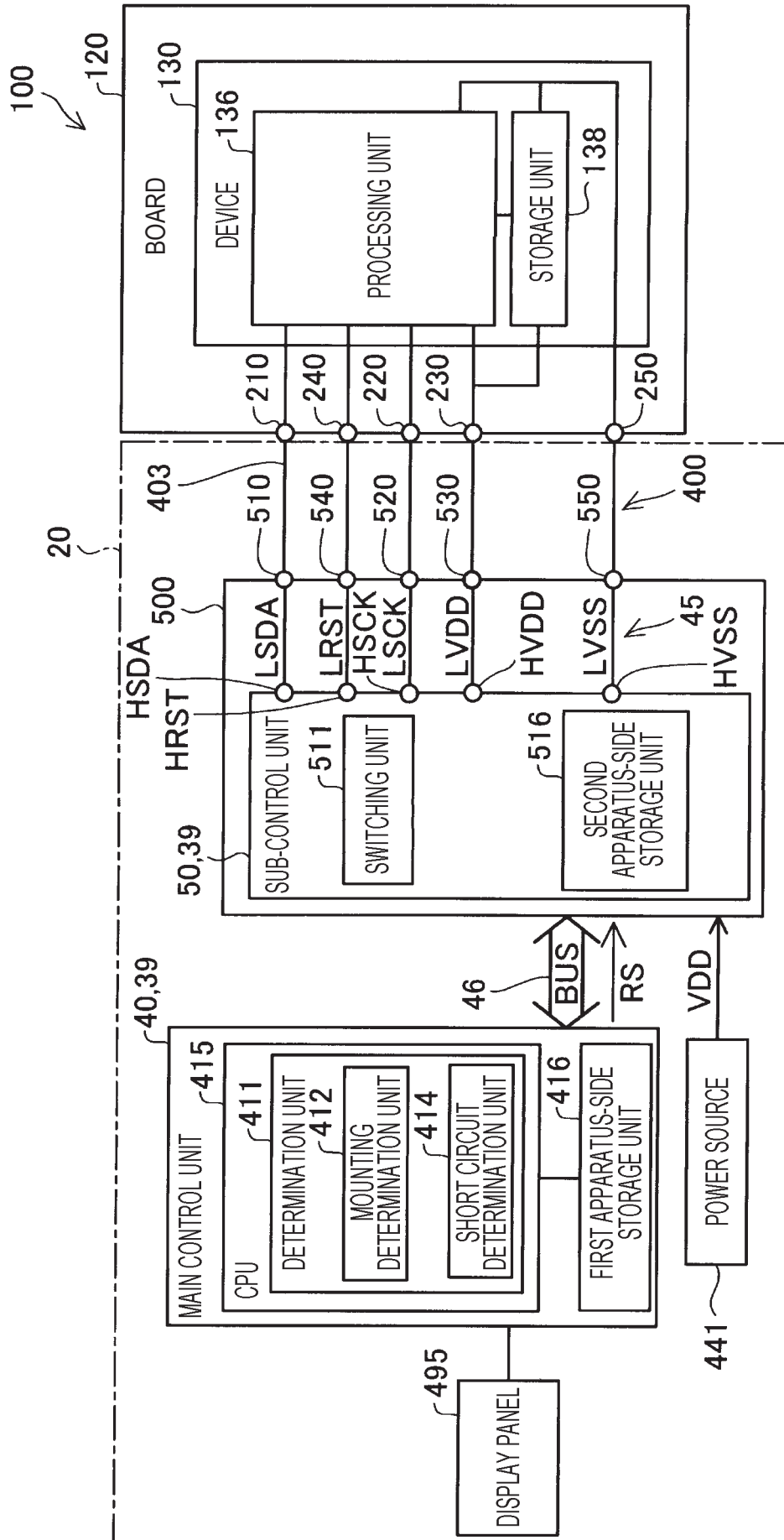


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FIG. 8



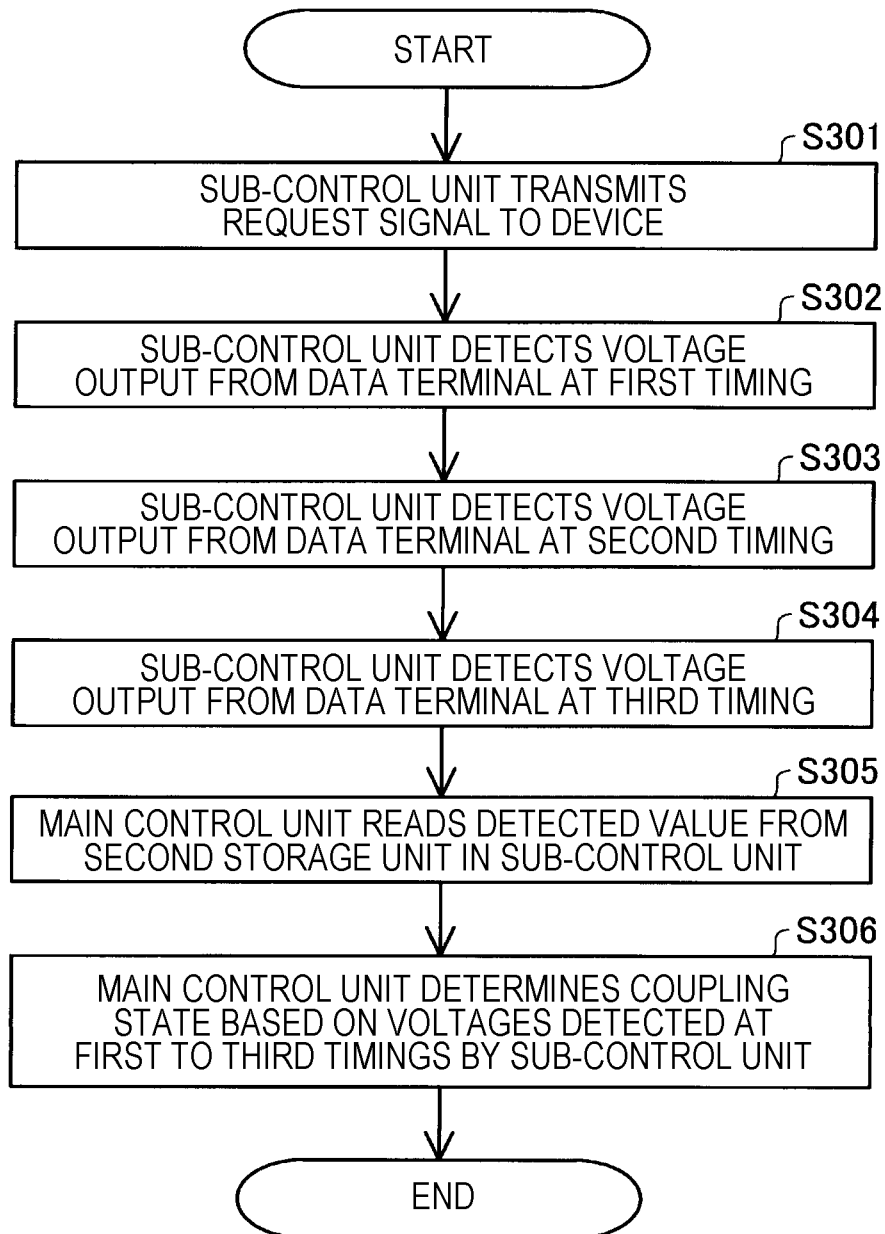
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FIG. 9



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FIG. 10A



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FIG. 10B

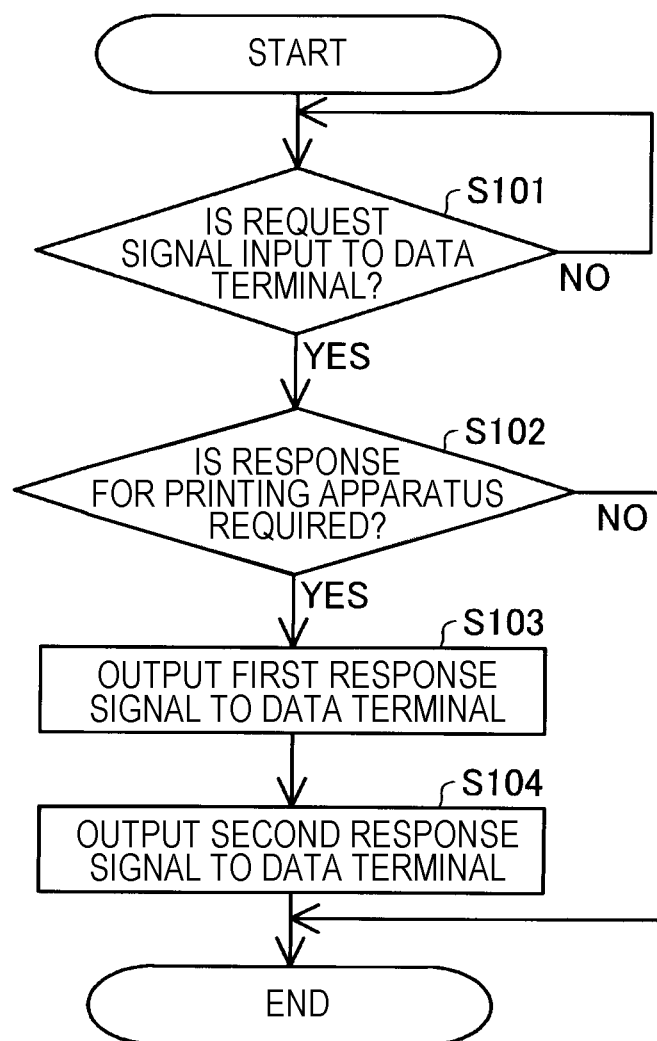


FIG. 11A

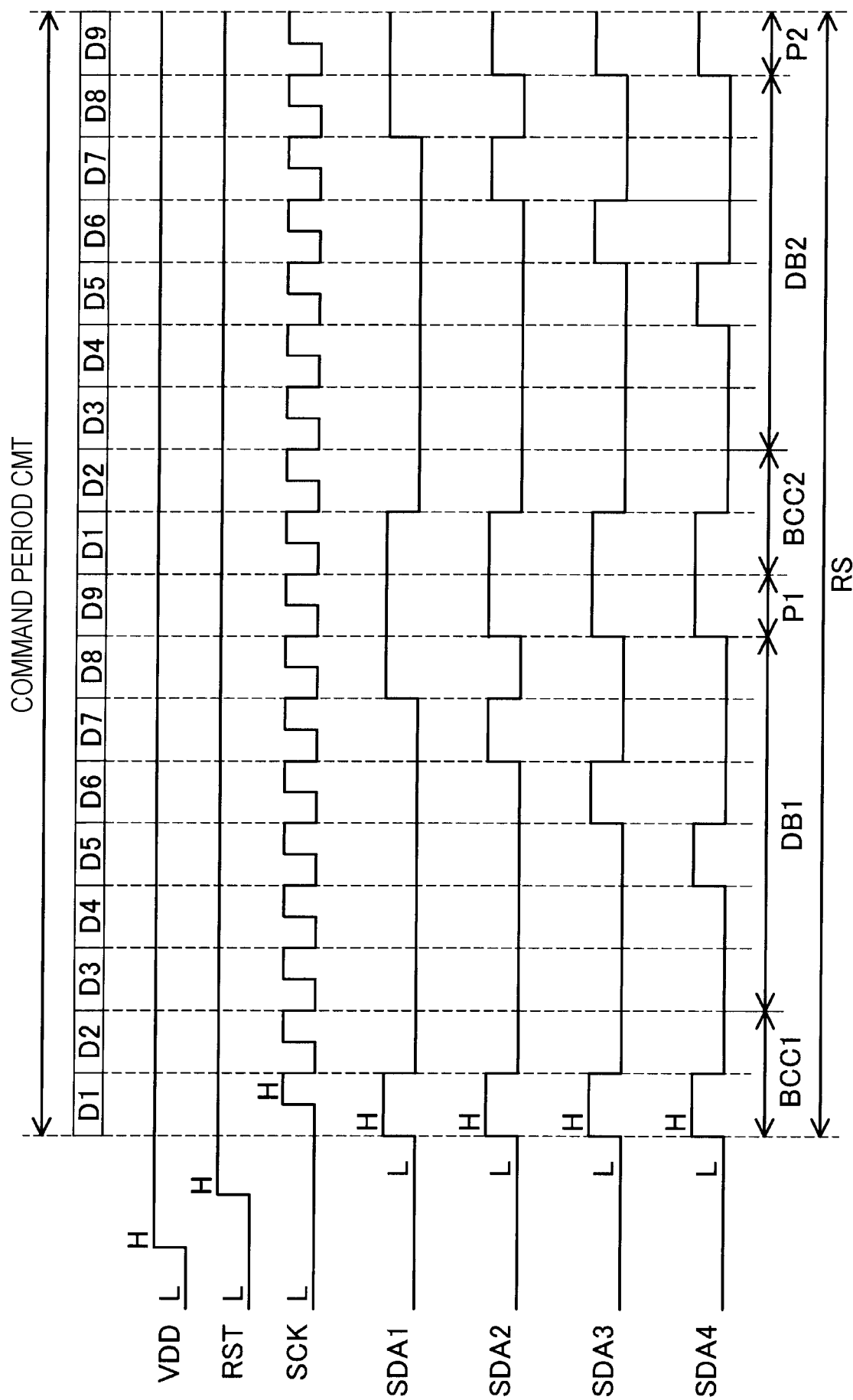
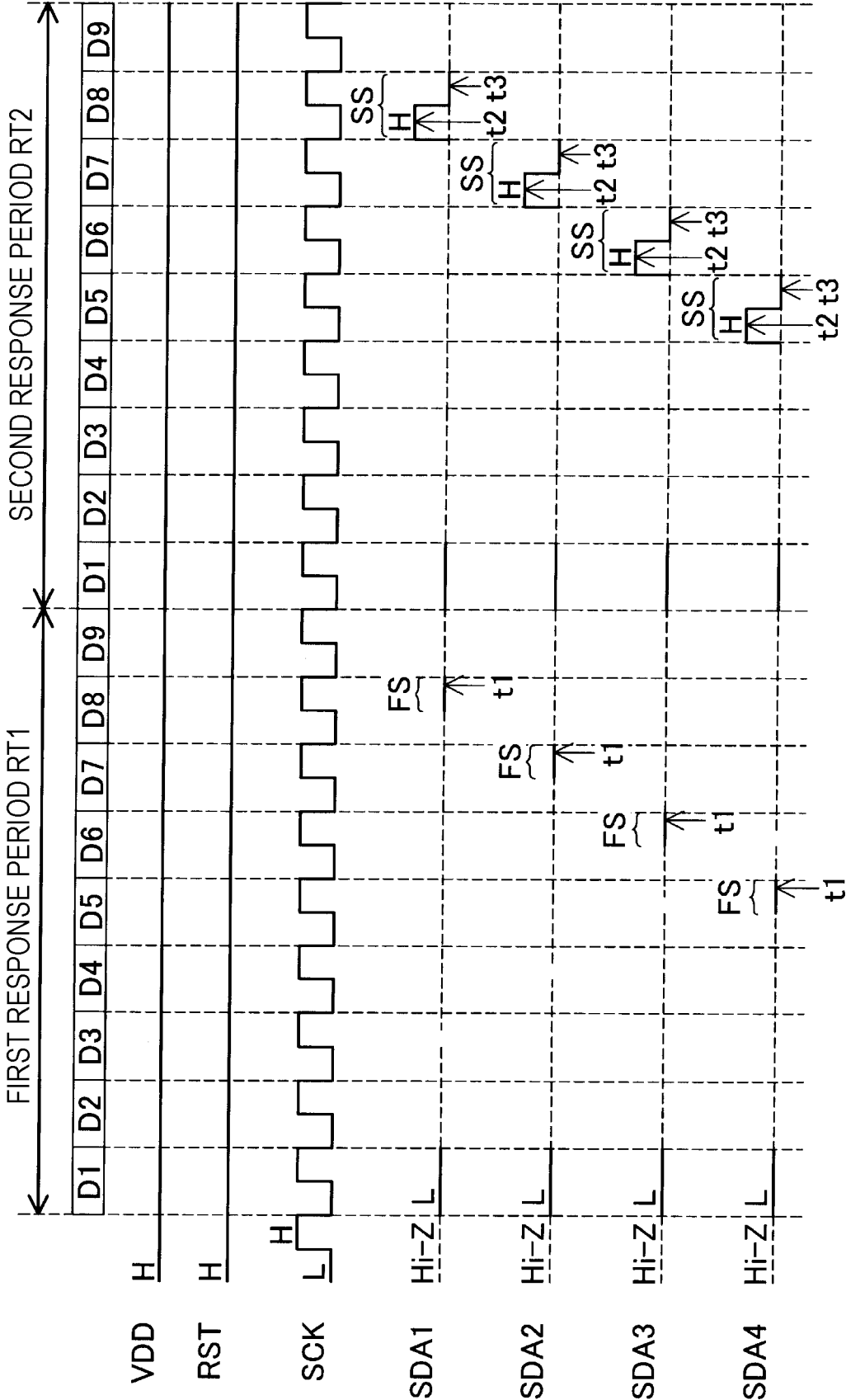
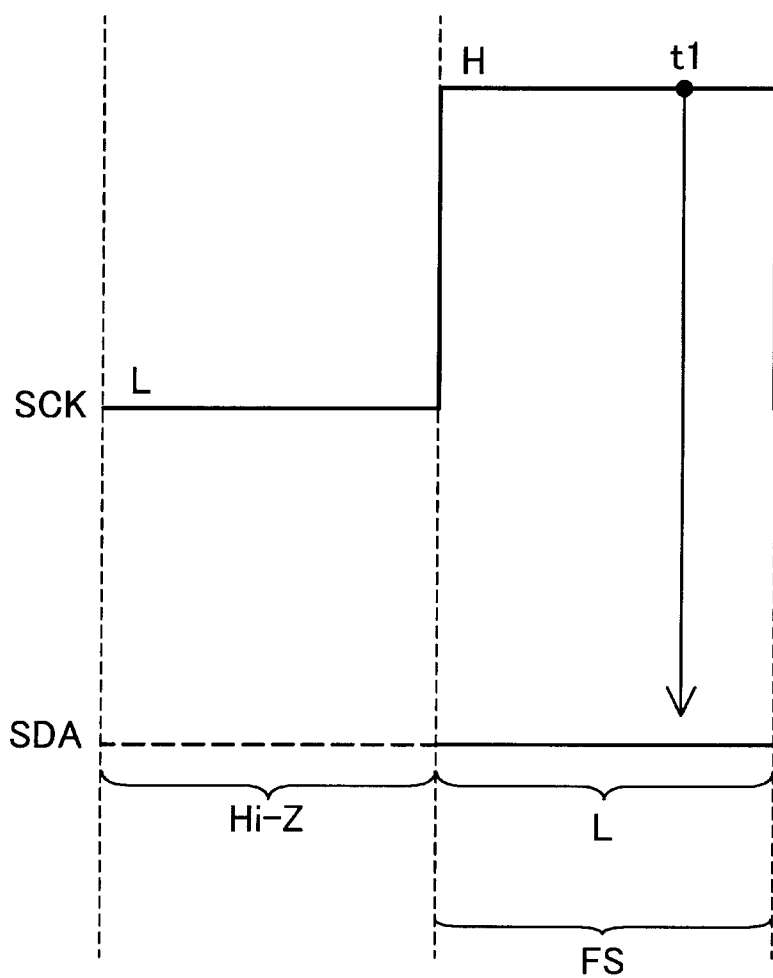


FIG. 11B



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FIG. 11C



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FIG. 11D

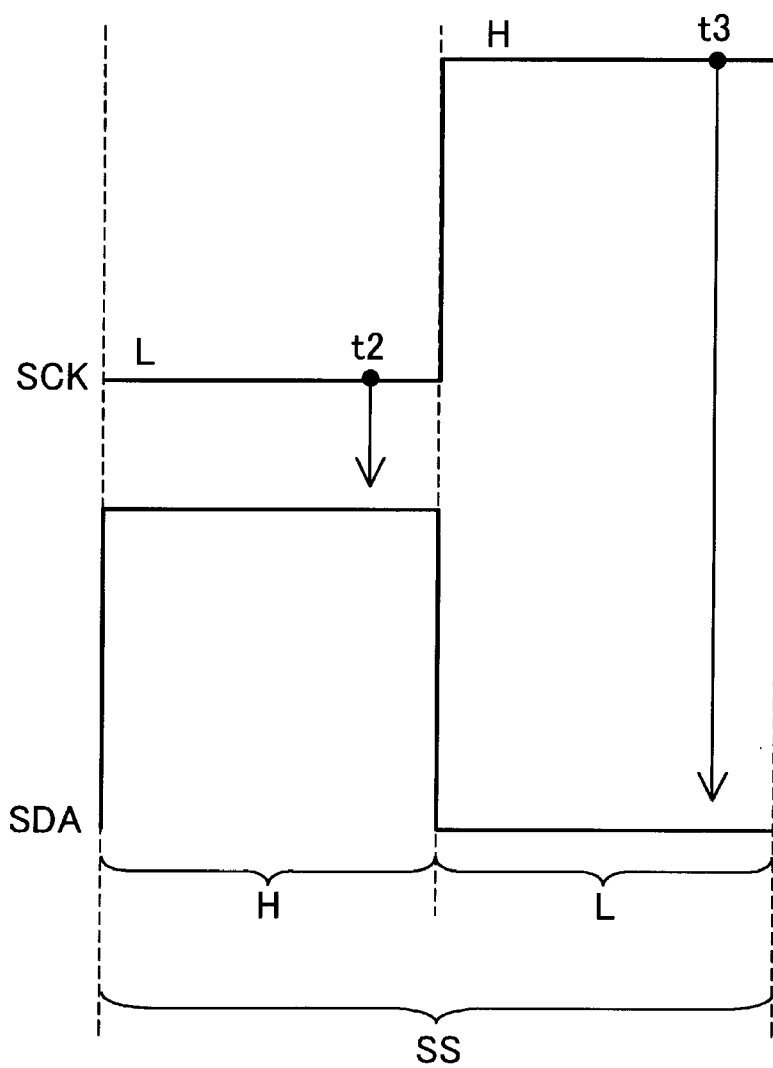


FIG. 12

	FIRST TIMING t1	SECOND TIMING t2	THIRD TIMING t3	COUPLING STATE	DETERMINATION RESULT
EXPECTED VALUE	L (FIRST EXPECTED VALUE)	H (SECOND EXPECTED VALUE)	L (THIRD EXPECTED VALUE)	—	—
DETECTED VALUE	L	H	L	MOUNTING-COMPLETED STATE	CONTAINER PROVIDED
	L	L	L	NON-MOUNTING-COMPLETED STATE	NO CONTAINER
	H	L	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND CLOCK TERMINAL	SHORT CIRCUIT OCCURRING
	H	H	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND POWER SOURCE TERMINAL OR STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND RESET TERMINAL	SHORT CIRCUIT OCCURRING

FIG. 13B

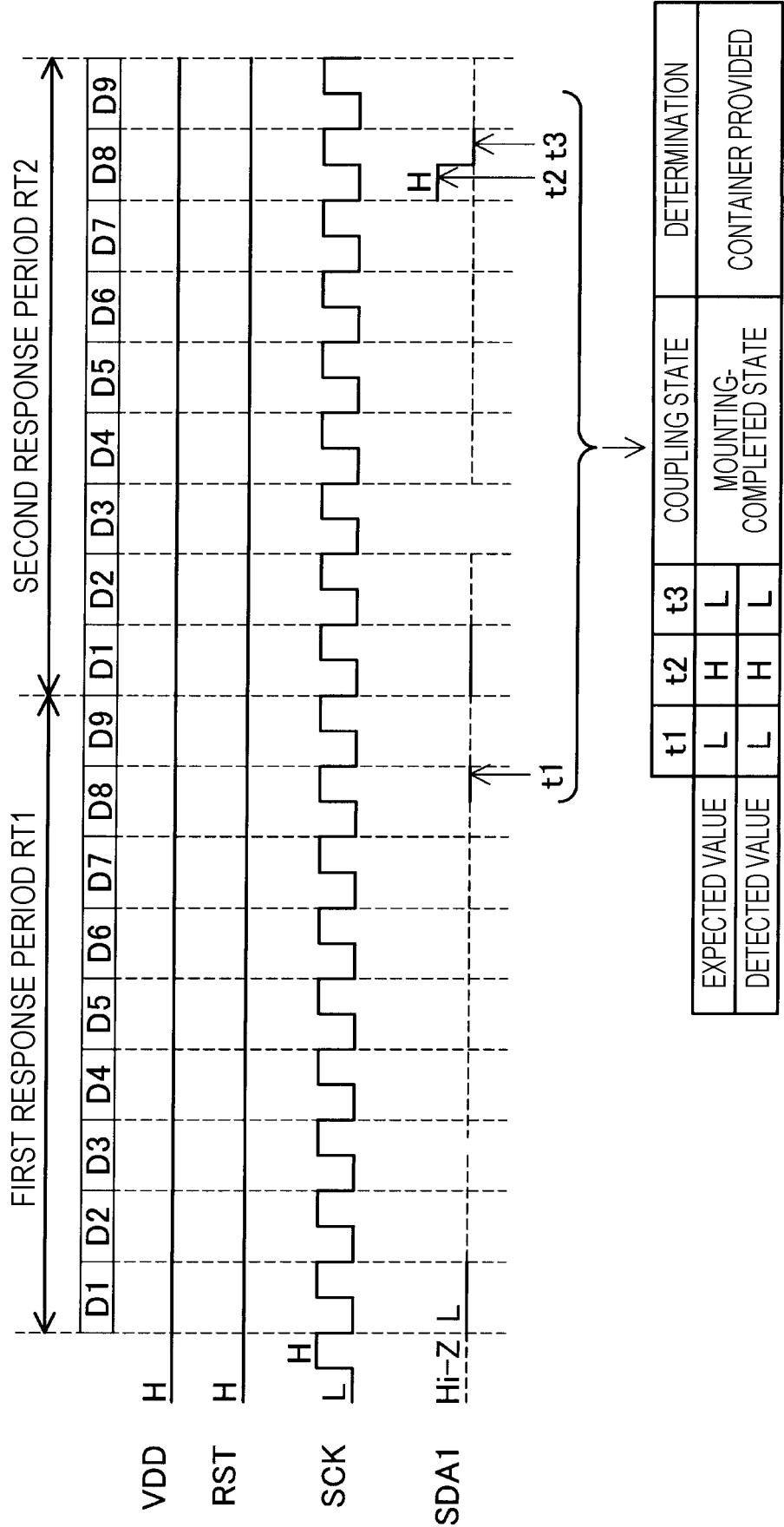


FIG. 14A

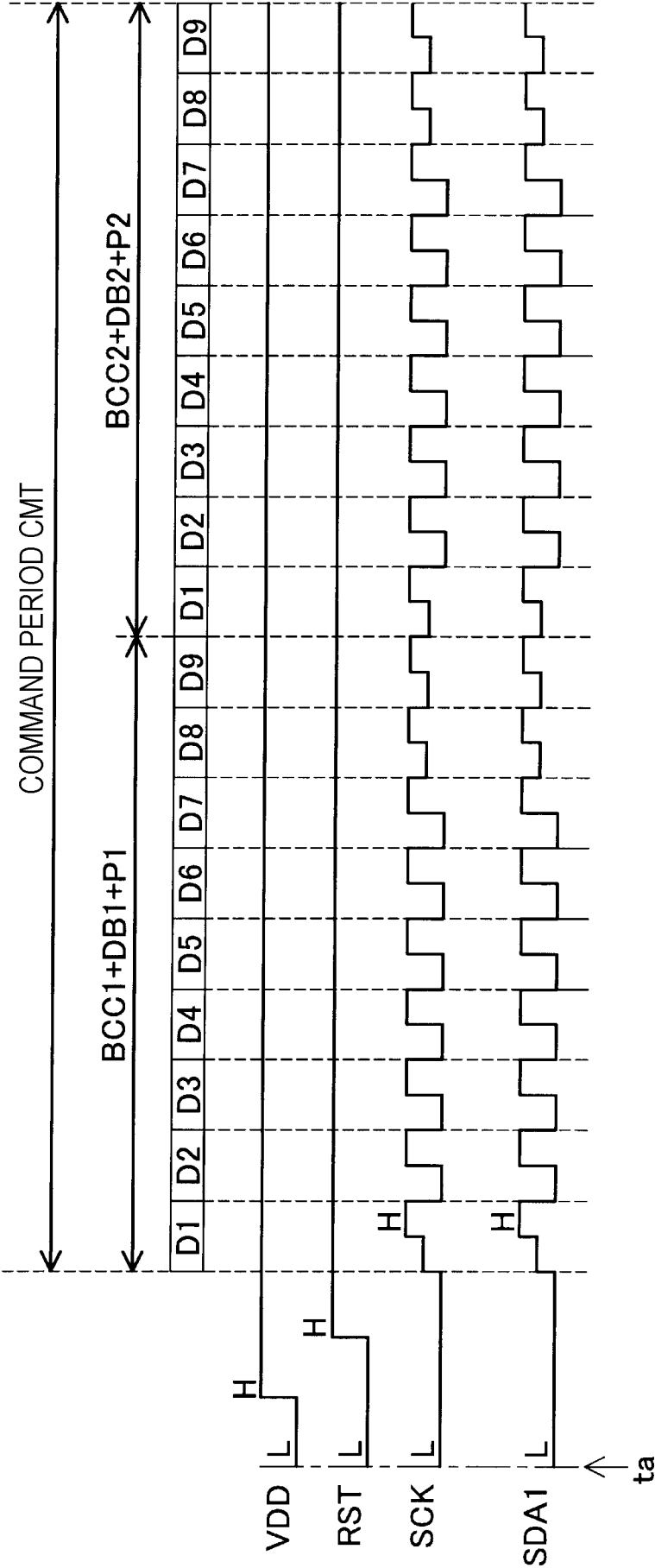


FIG. 14B

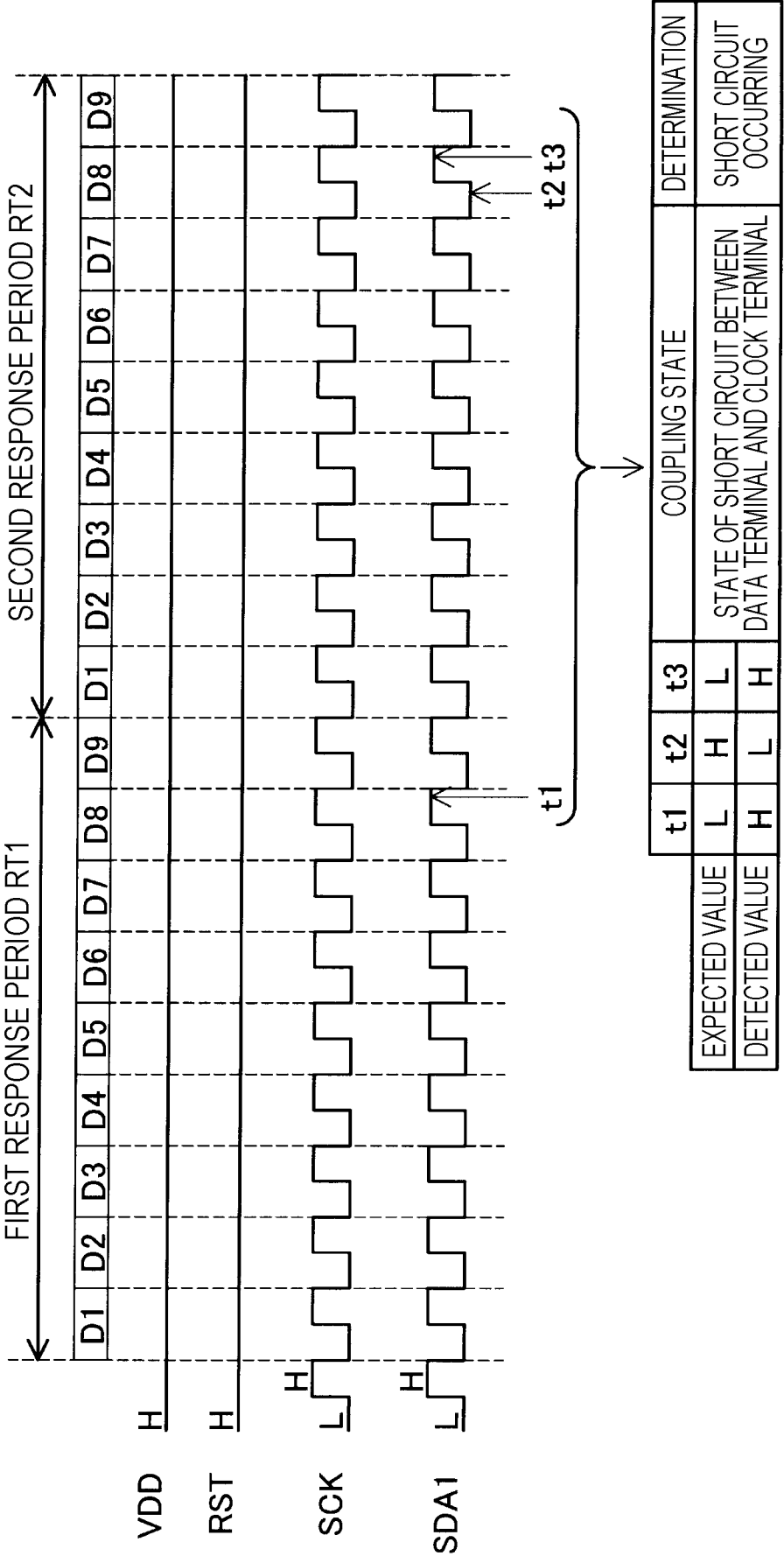


FIG. 15

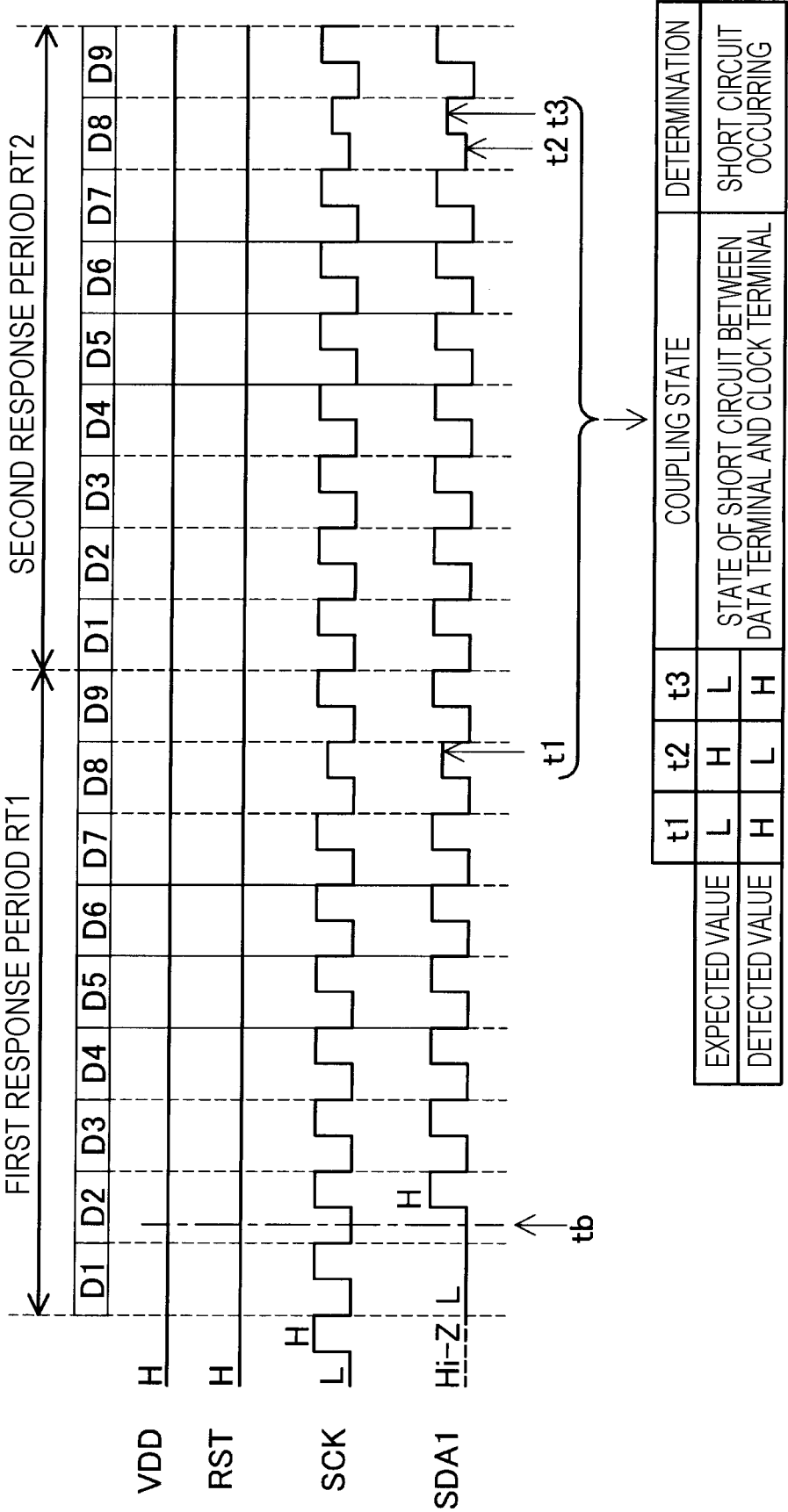


FIG. 16A

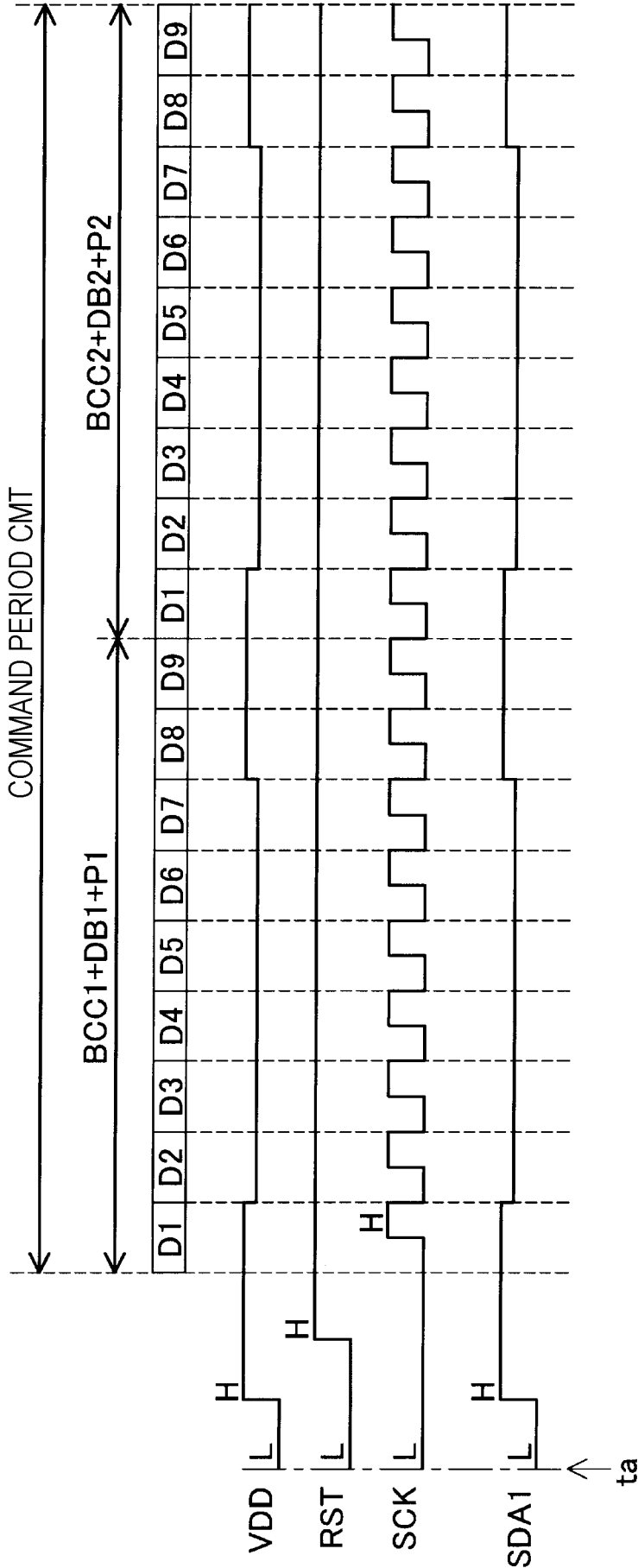


FIG. 16B

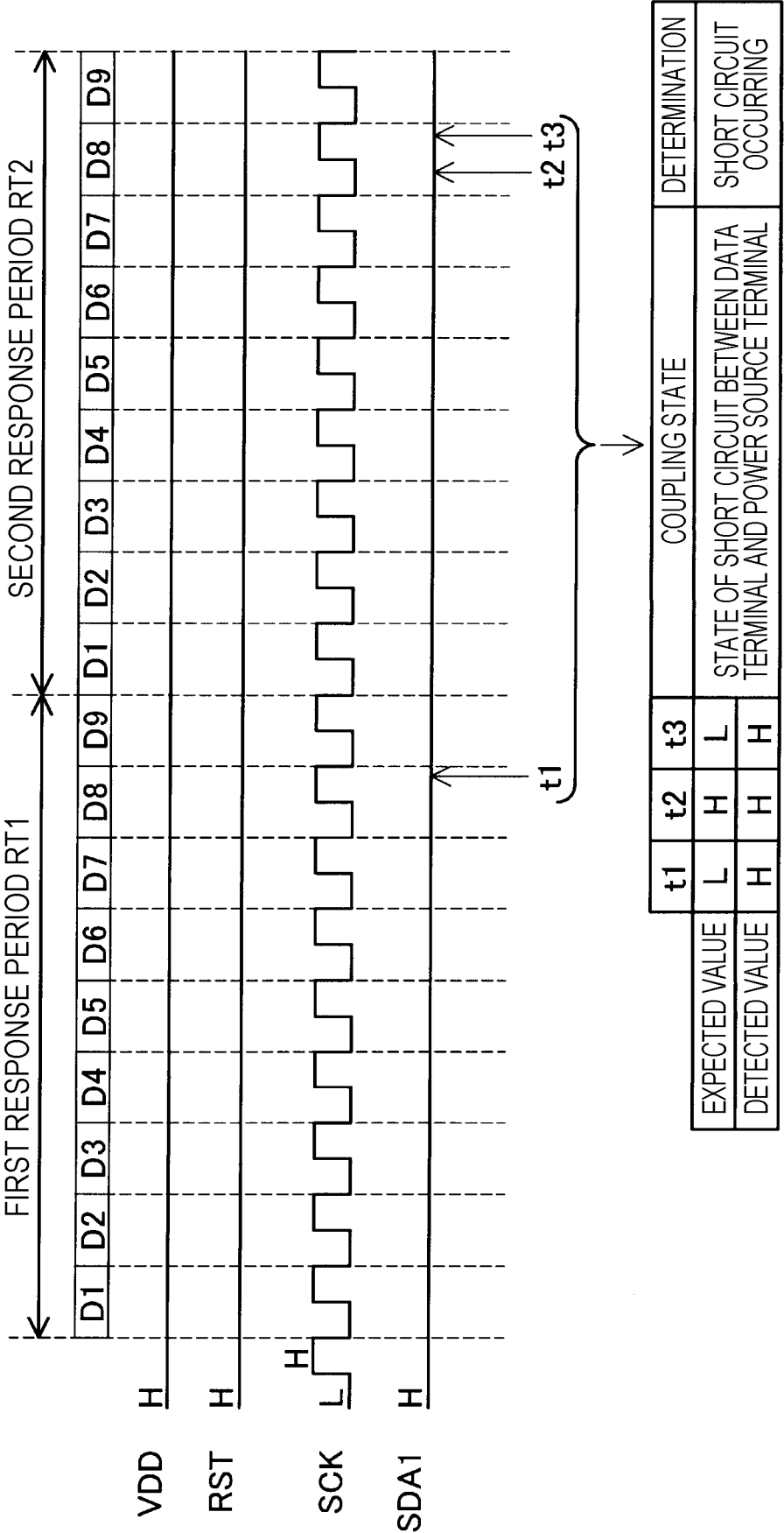


FIG. 17

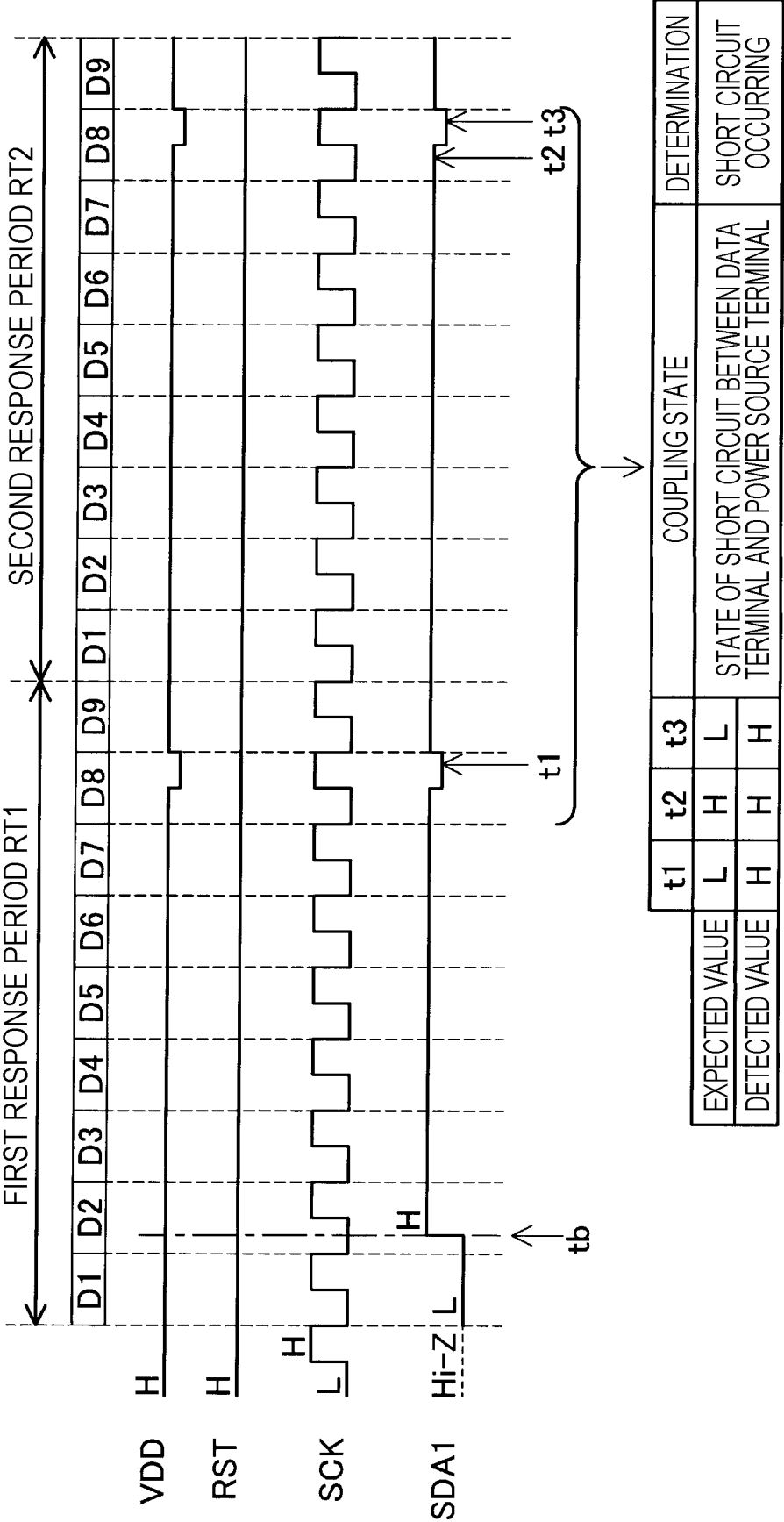


FIG. 18A

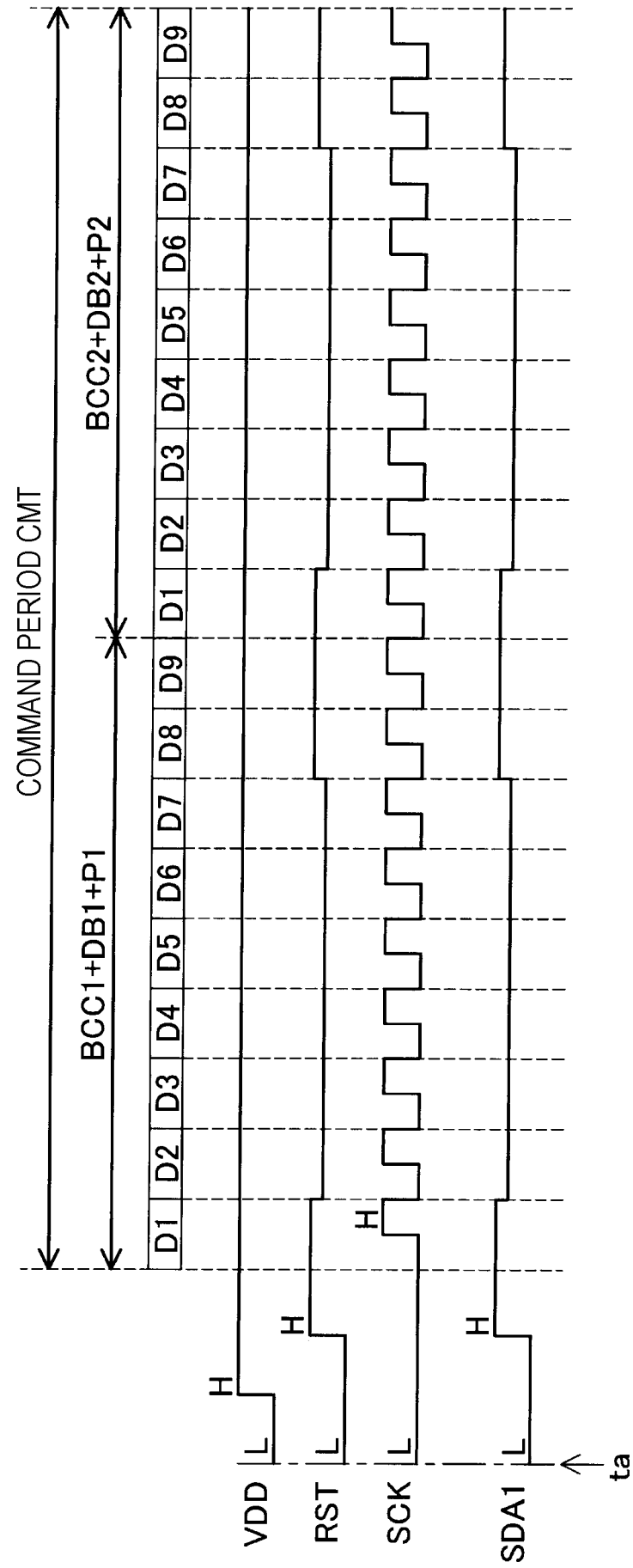


FIG. 18B

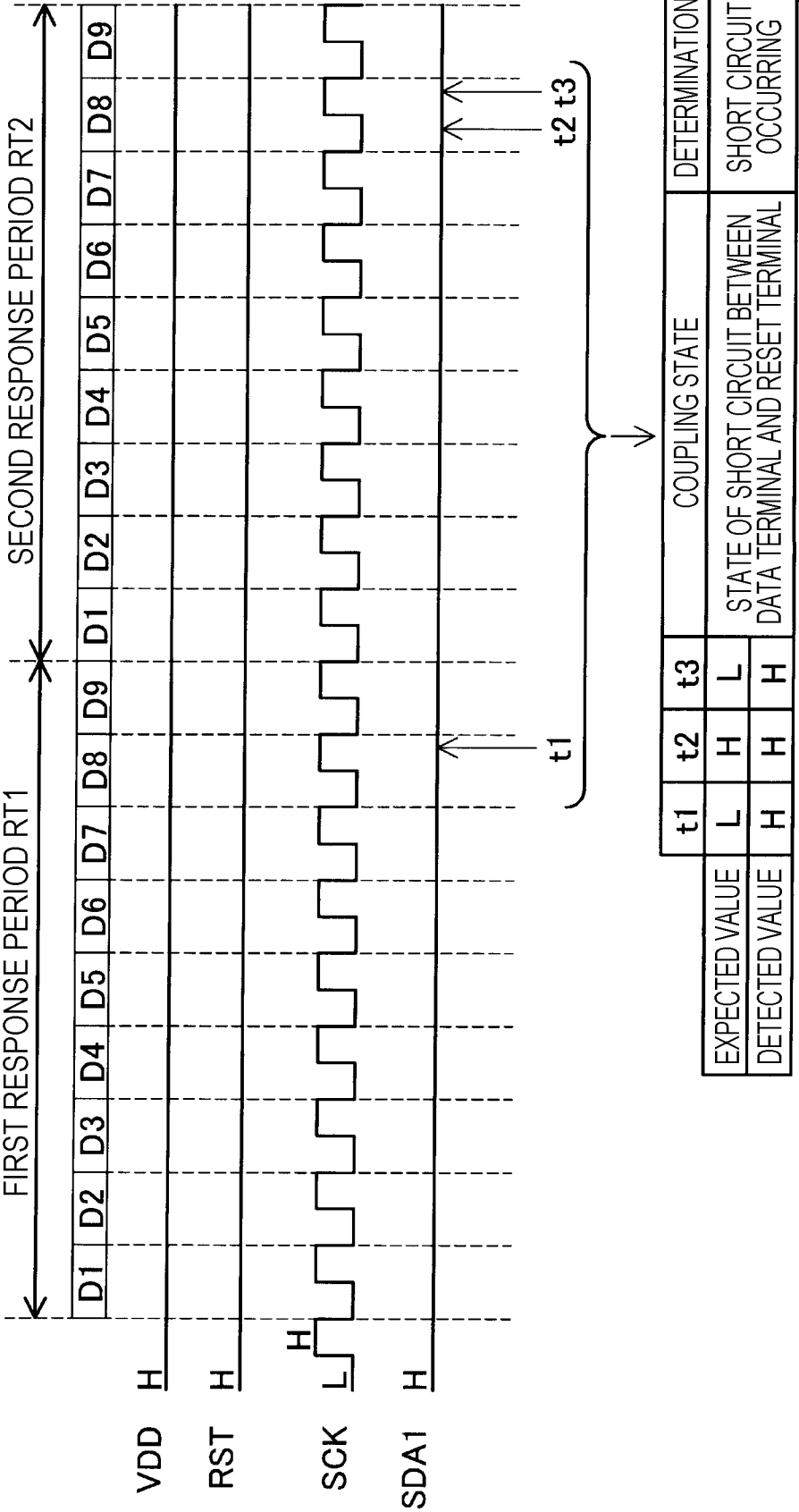


FIG. 19

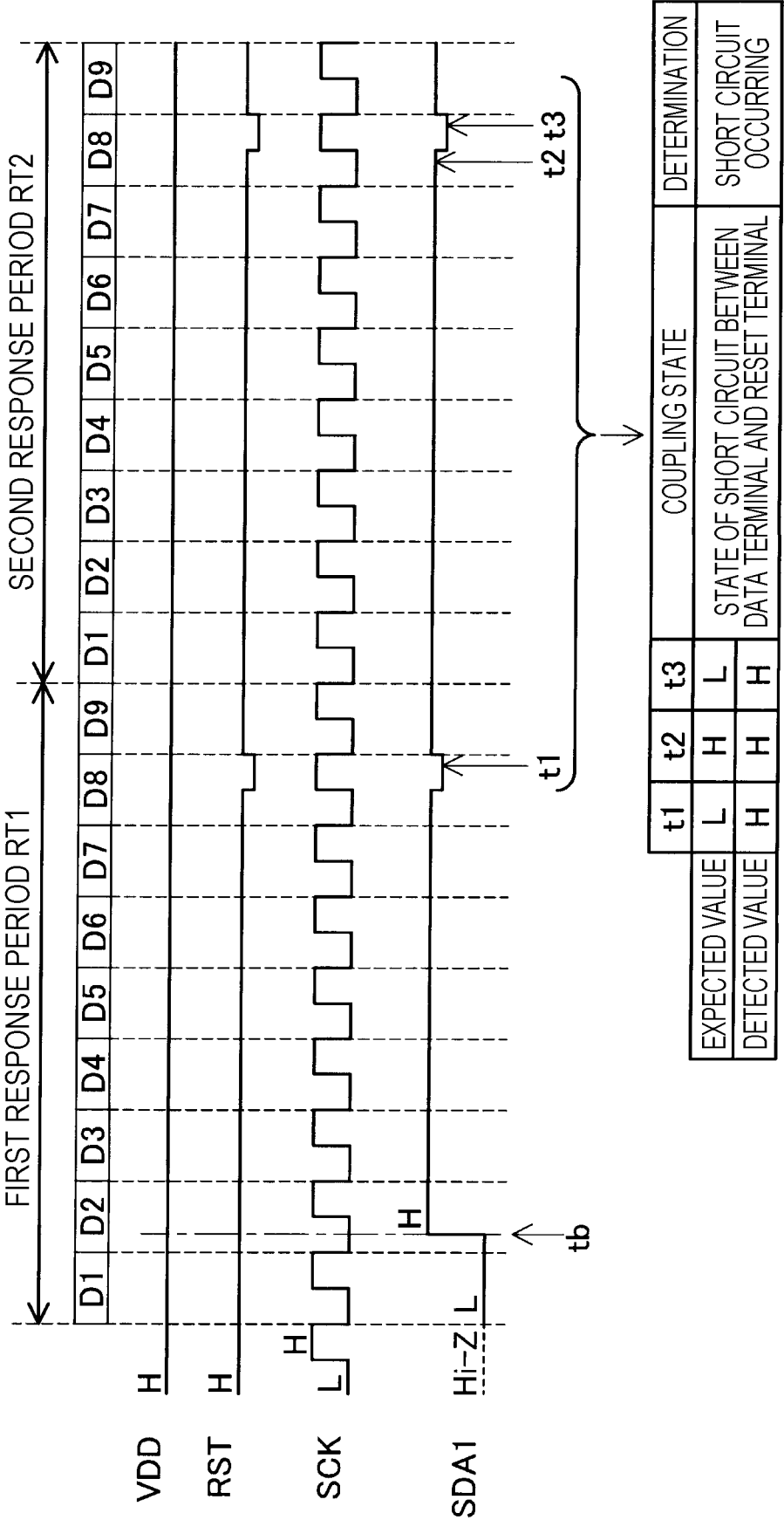


FIG. 20A

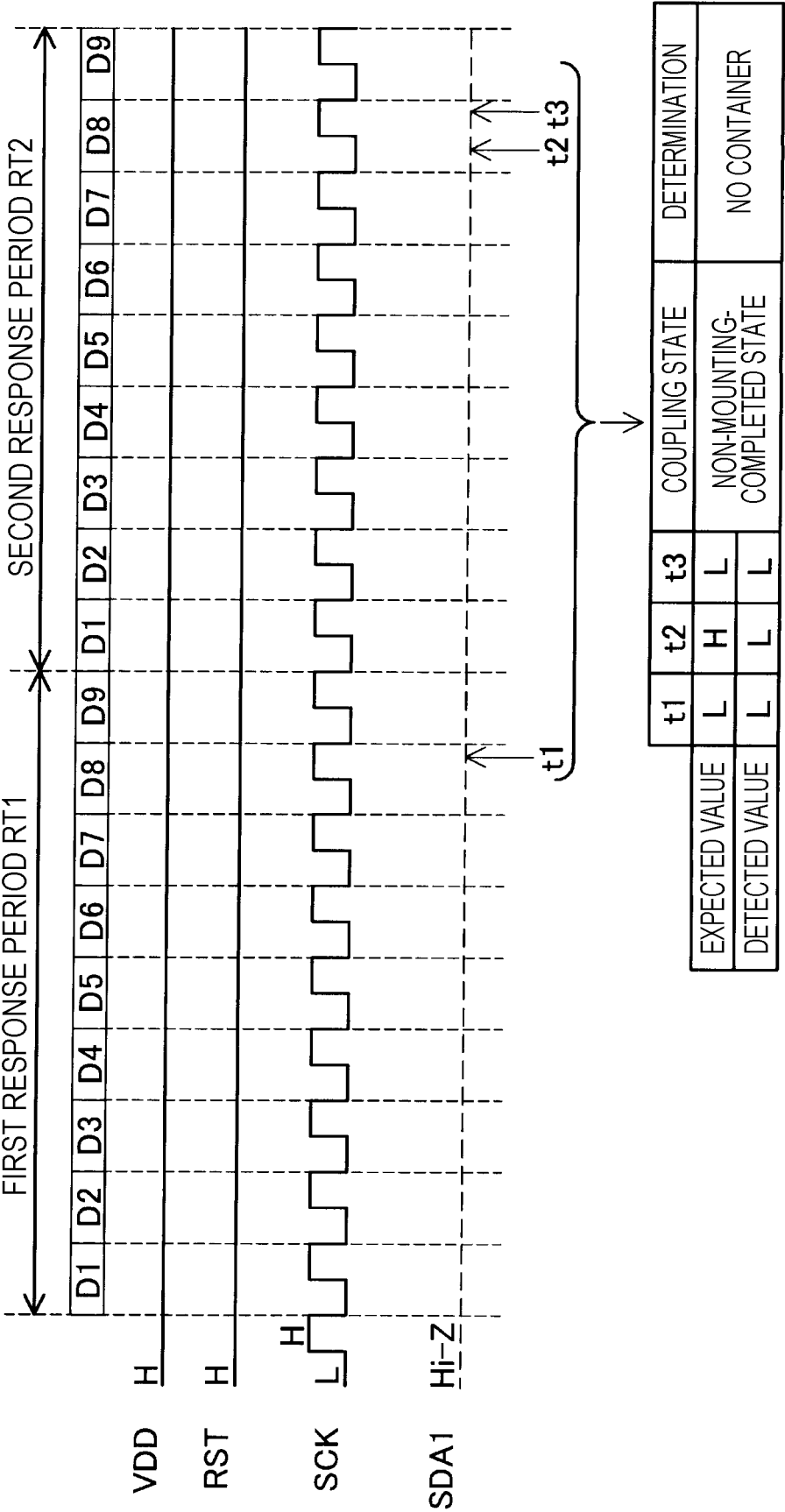
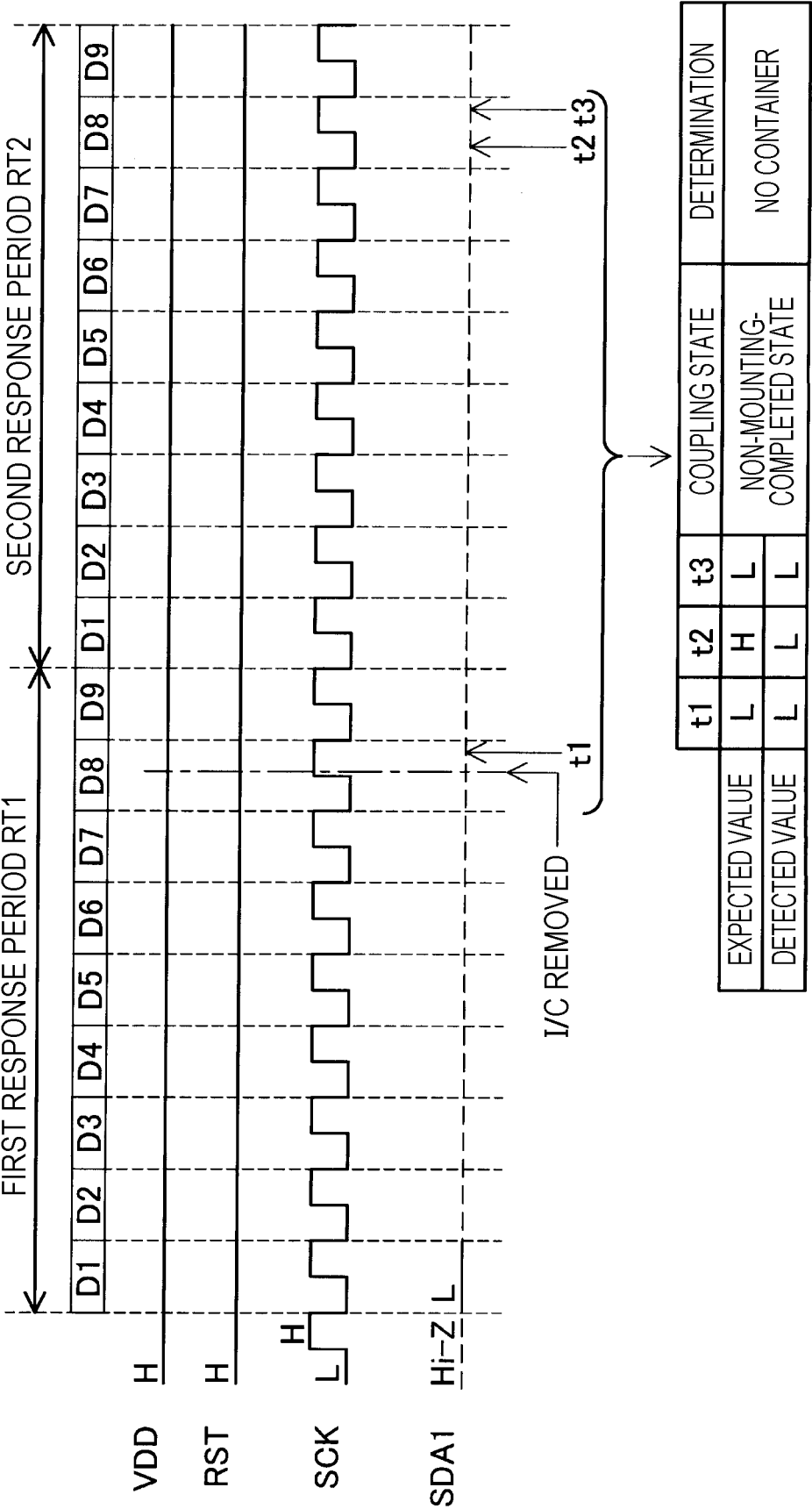


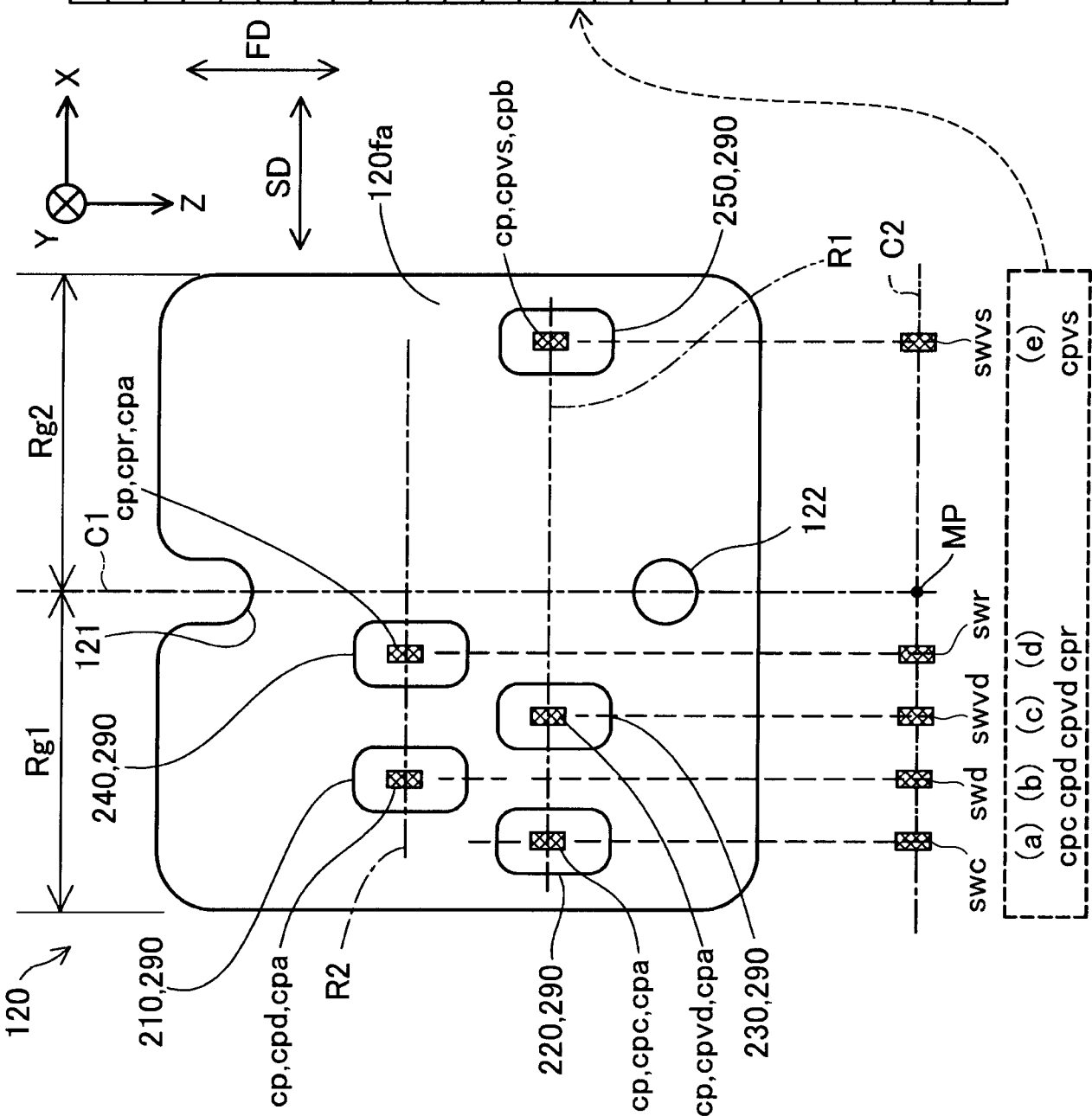
FIG. 20B



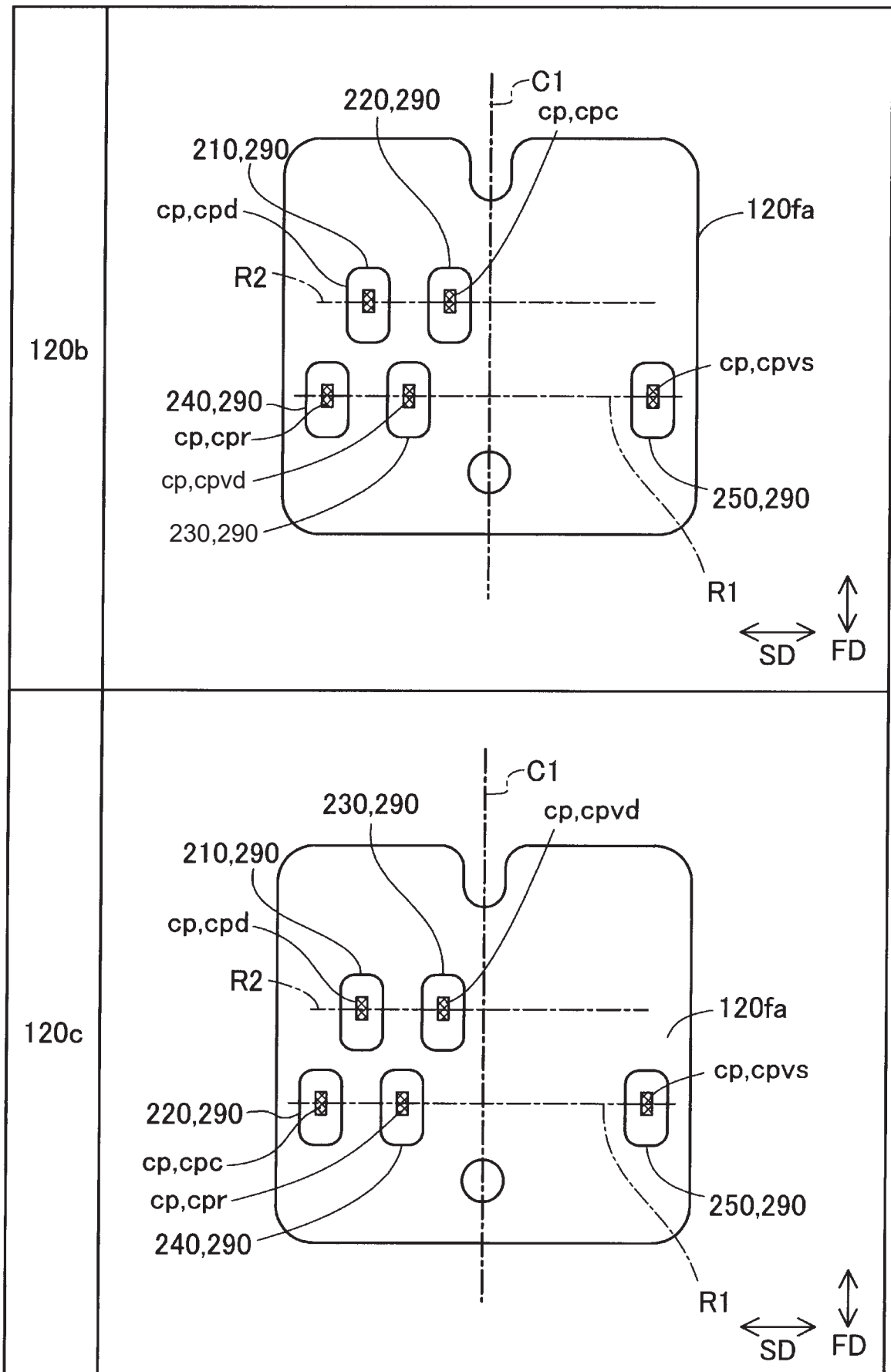
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FIG. 20C

	TIMING			COUPLING STATE	DETERMINATION	No.
	t1	t2	t3			
EXPECTED VALUE	L	H	L	—		
DETECTED VALUE	H	L	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND CLOCK TERMINAL OCCURS AT $t < t_1$	SHORT CIRCUIT OCCURRING	1
	L	L	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND CLOCK TERMINAL OCCURS AT $t_1 < t < t_2$	SHORT CIRCUIT OCCURRING	2
	L	H	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND CLOCK TERMINAL OCCURS AT $t_2 < t < t_3$	SHORT CIRCUIT OCCURRING	3
	H	H	L	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND CLOCK TERMINAL IS ELIMINATED AT $t_1 < t < t_2$	SHORT CIRCUIT OCCURRING	4
	H	L	L	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND CLOCK TERMINAL IS ELIMINATED AT $t_2 < t < t_3$	SHORT CIRCUIT OCCURRING	5
	H	H	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND POWER SOURCE TERMINAL OR BETWEEN DATA TERMINAL OR RESET TERMINAL OCCURS AT $t < t_1$	SHORT CIRCUIT OCCURRING	6
	L	H	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND POWER SOURCE TERMINAL OR BETWEEN DATA TERMINAL OR RESET TERMINAL OCCURS AT $t_1 < t < t_2$	SHORT CIRCUIT OCCURRING	7
	L	H	H	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND POWER SOURCE TERMINAL OR BETWEEN DATA TERMINAL OR RESET TERMINAL OCCURS AT $t_2 < t < t_3$	SHORT CIRCUIT OCCURRING	8
	H	H	L	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND POWER SOURCE TERMINAL OR BETWEEN DATA TERMINAL OR RESET TERMINAL IS ELIMINATED AT $t_1 < t < t_2$	SHORT CIRCUIT OCCURRING	9
	H	H	L	STATE OF SHORT CIRCUIT BETWEEN DATA TERMINAL AND POWER SOURCE TERMINAL OR BETWEEN DATA TERMINAL OR RESET TERMINAL IS ELIMINATED AT $t_2 < t < t_3$	SHORT CIRCUIT OCCURRING	10

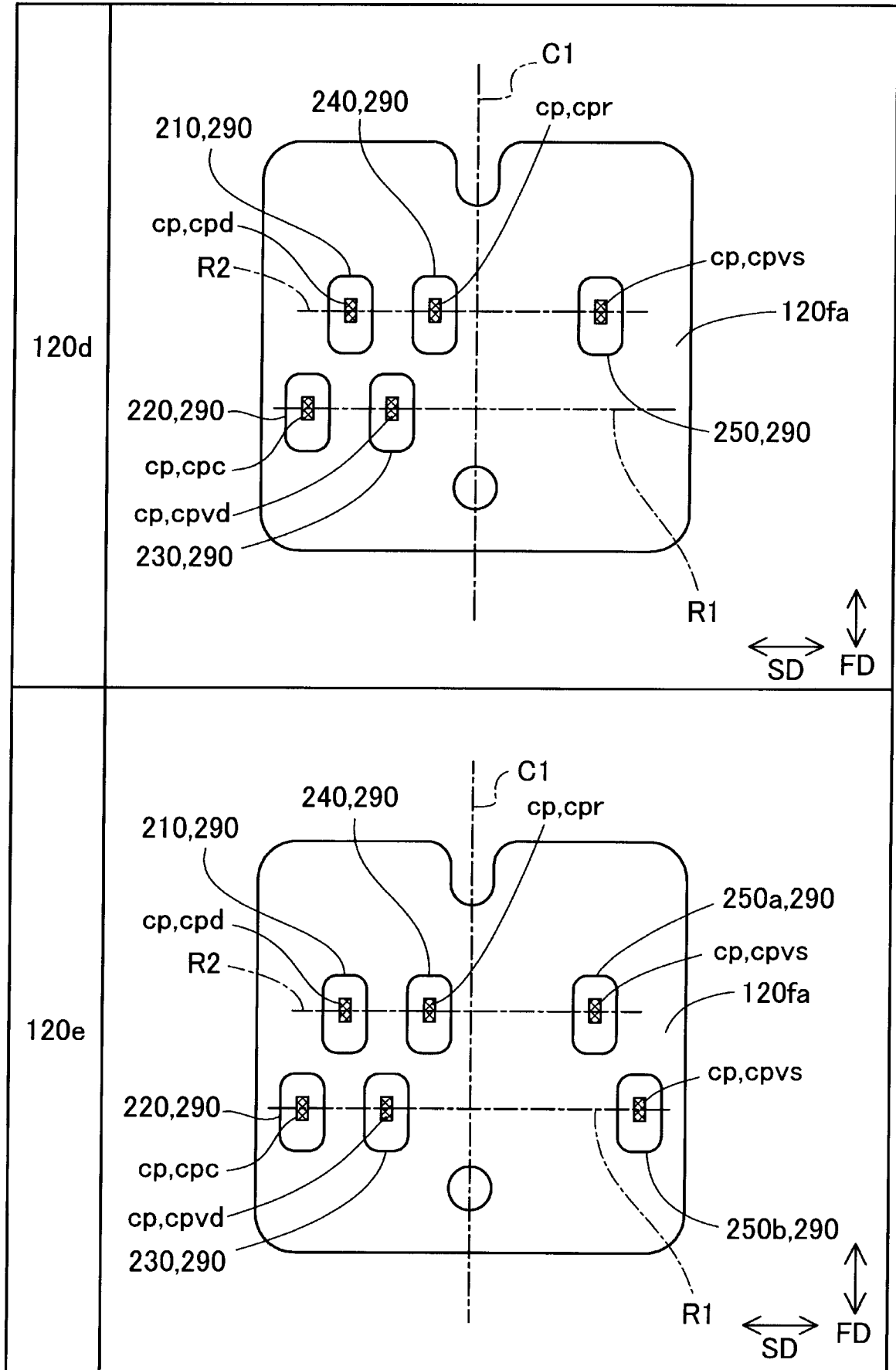
FIG. 21A



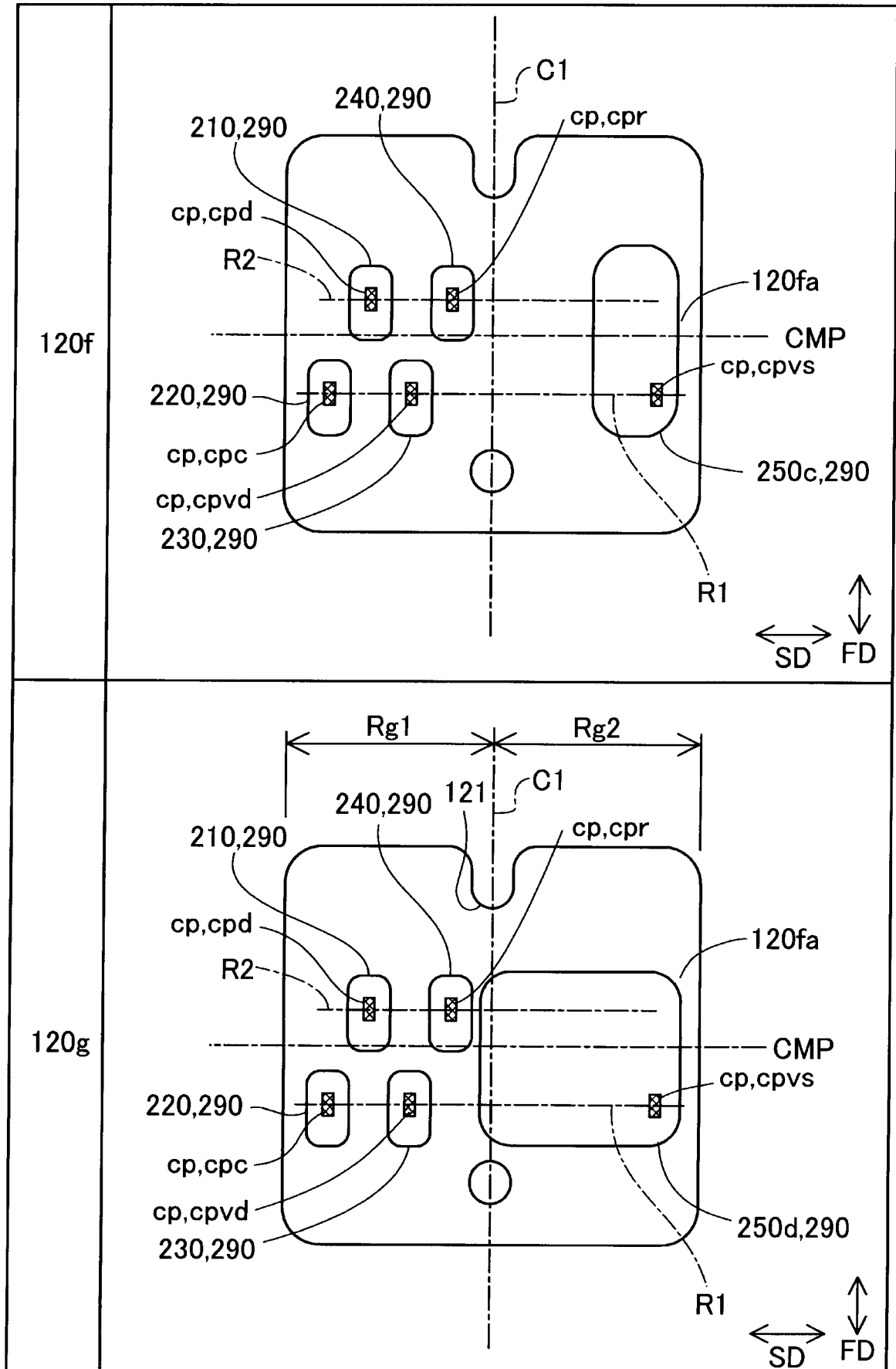
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FIG. 21B



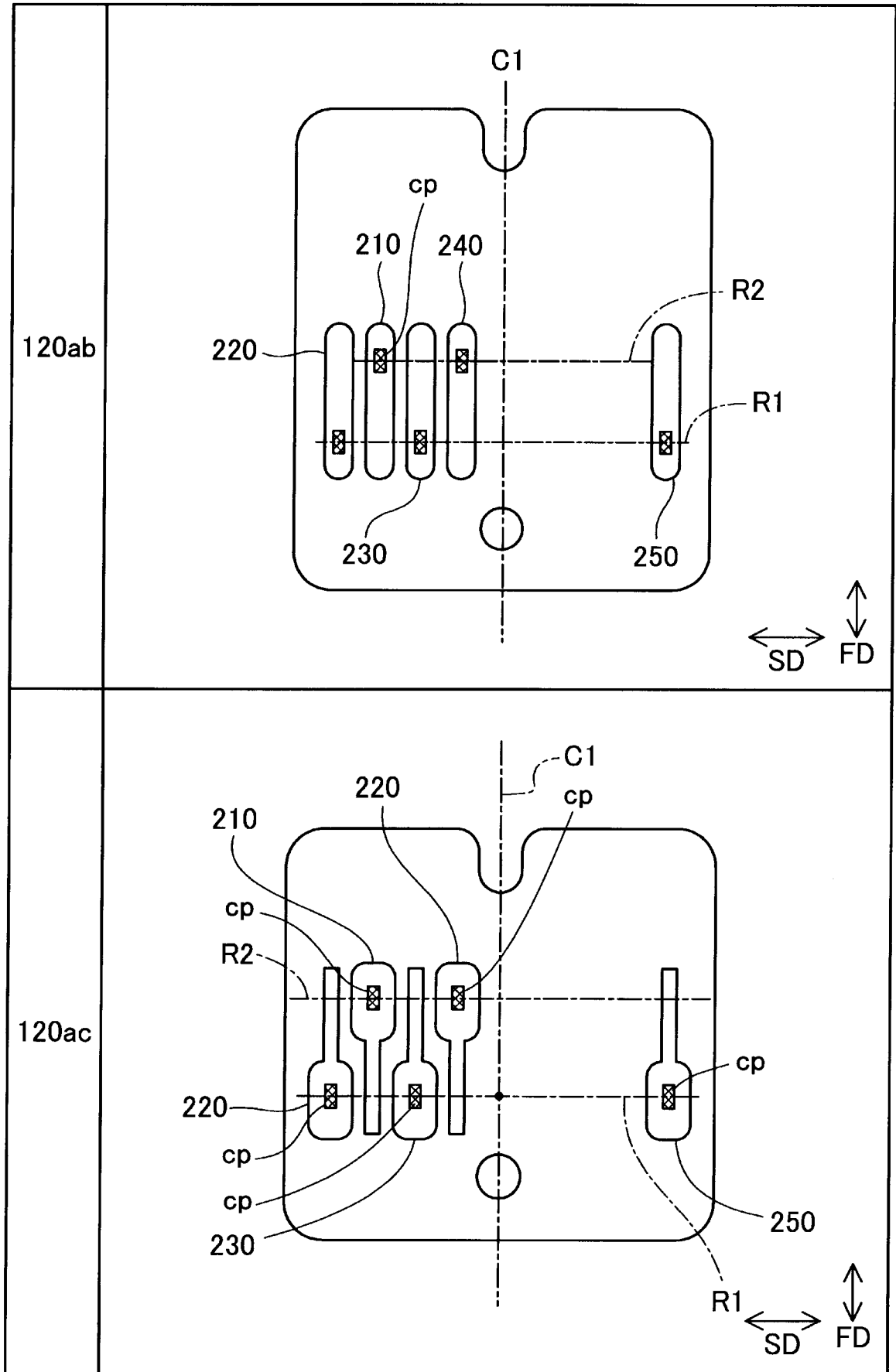
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FIG. 22



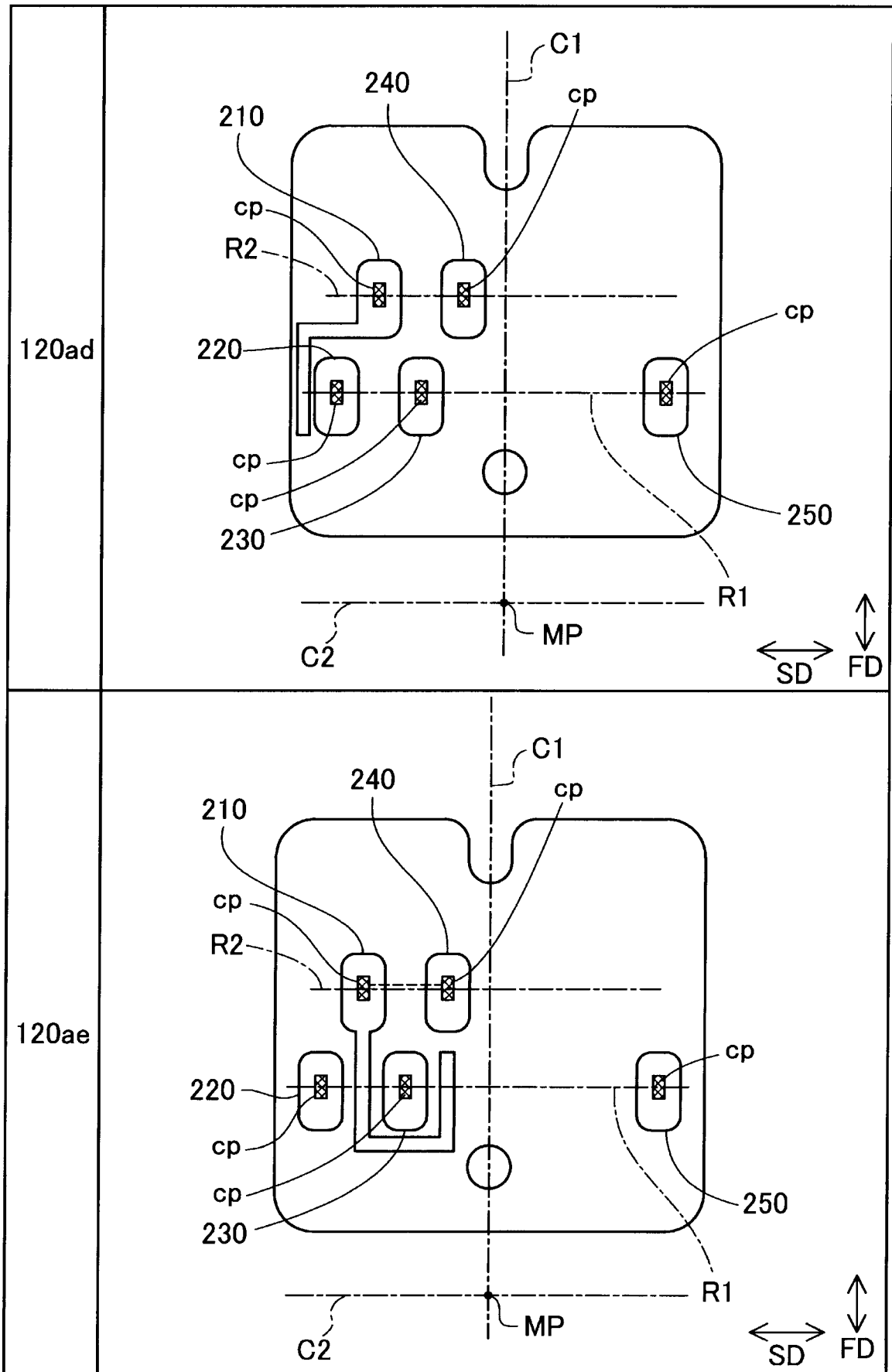
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FIG. 23



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FIG. 24



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FIG. 25



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FIG. 26

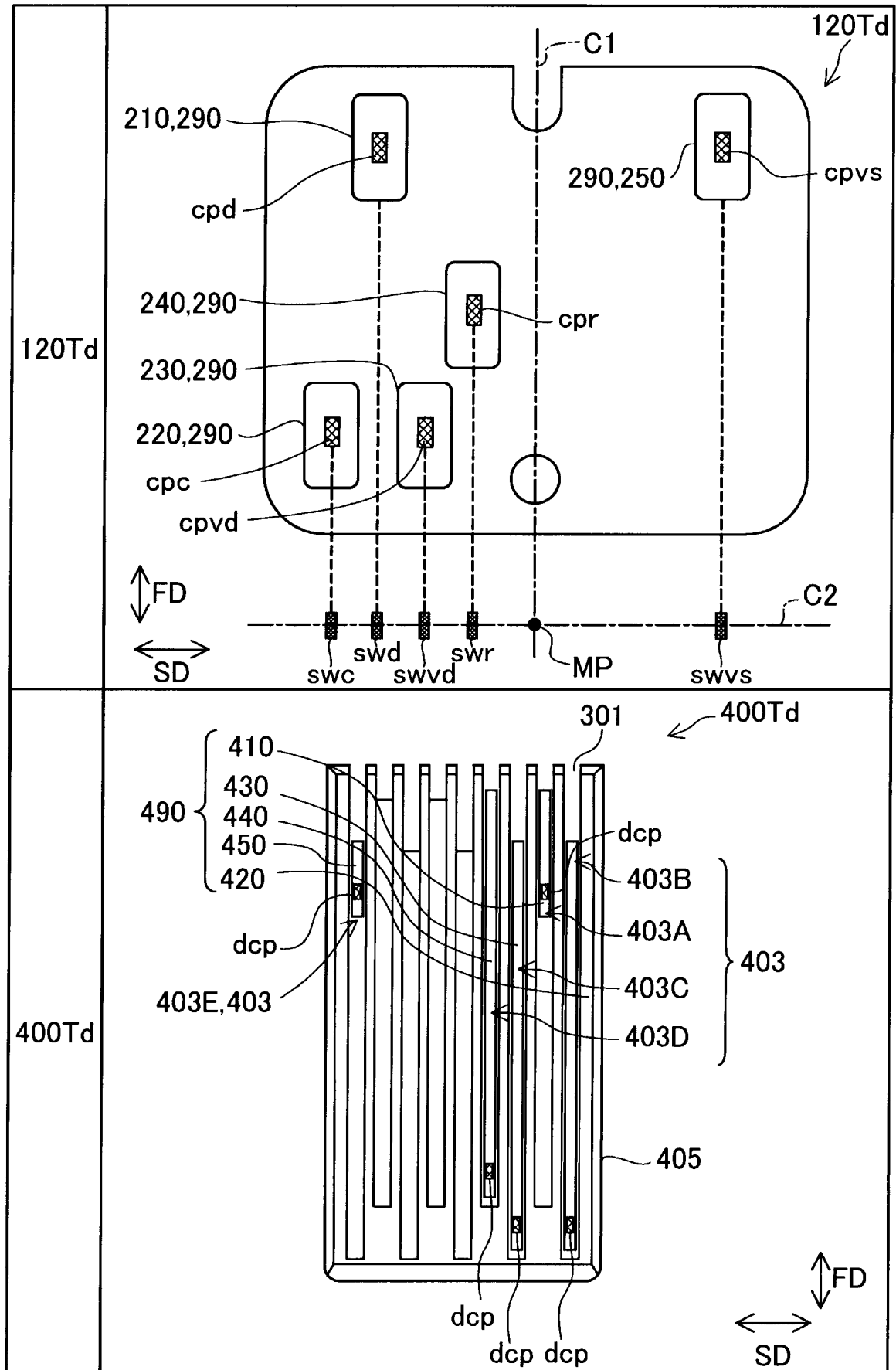
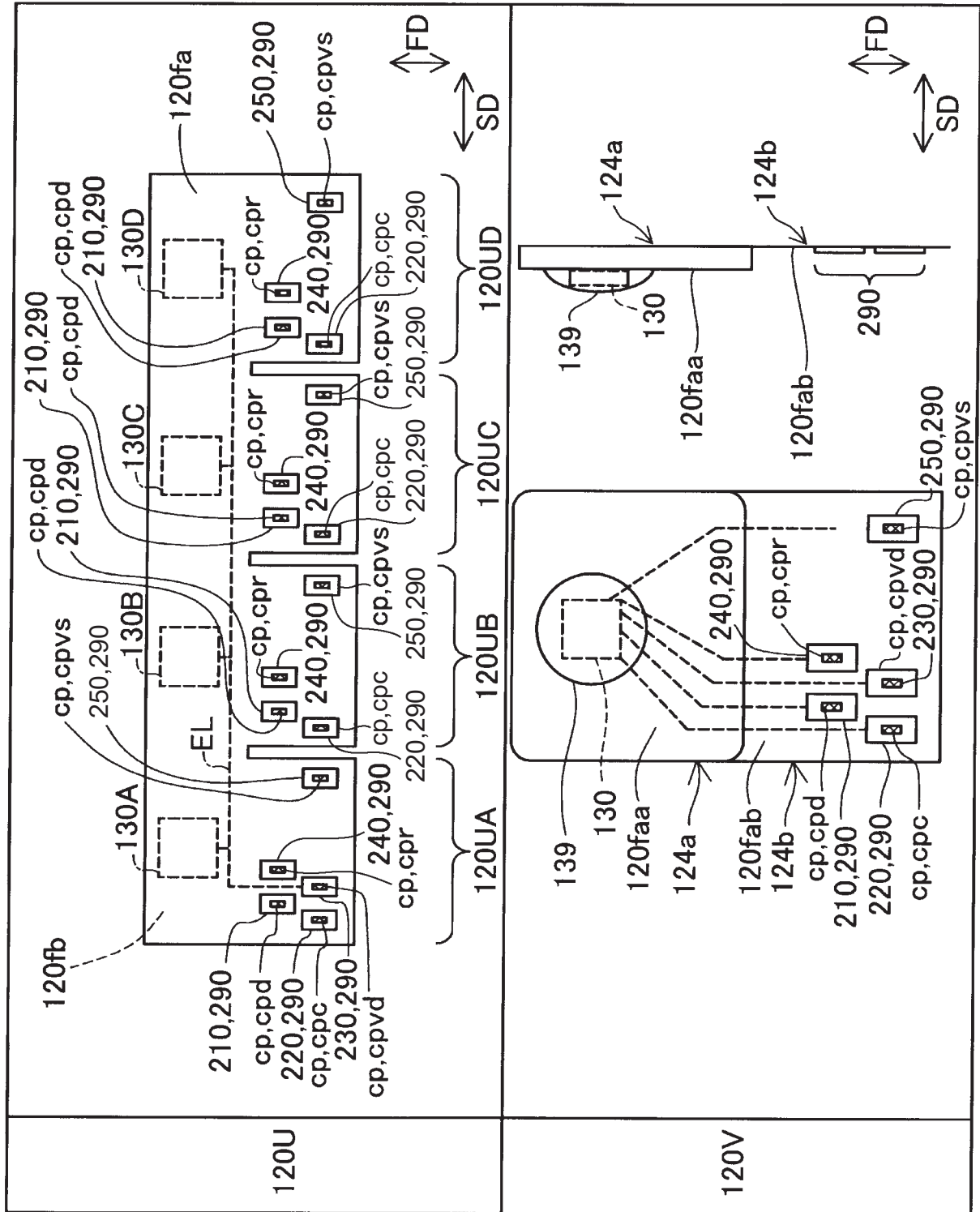
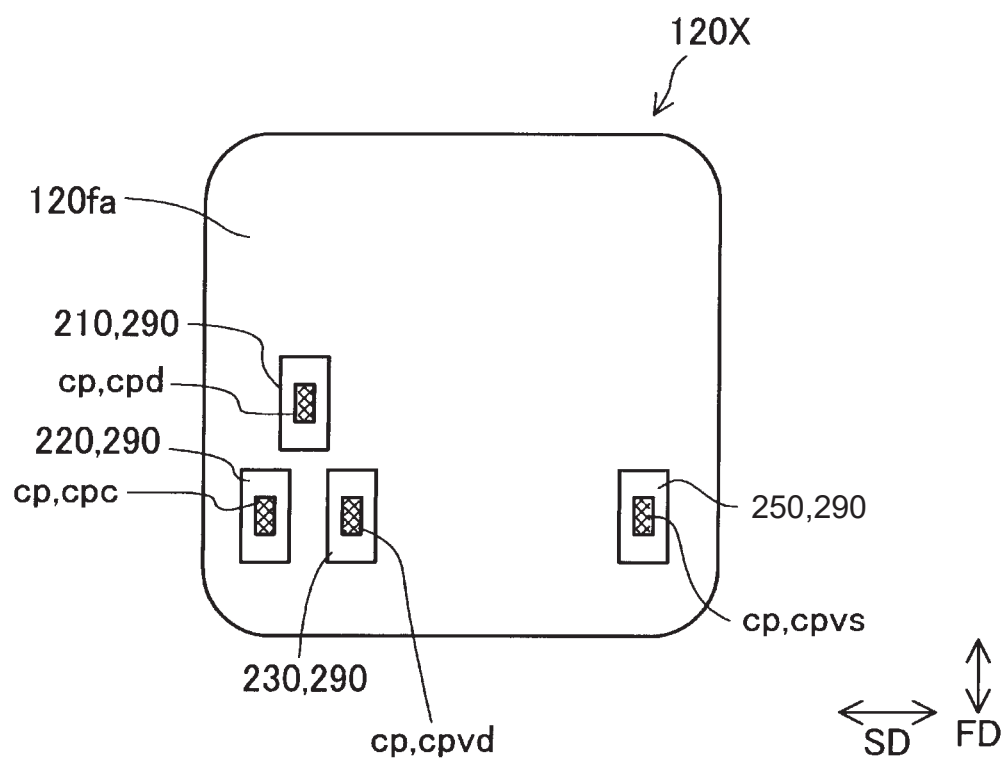


FIG. 27



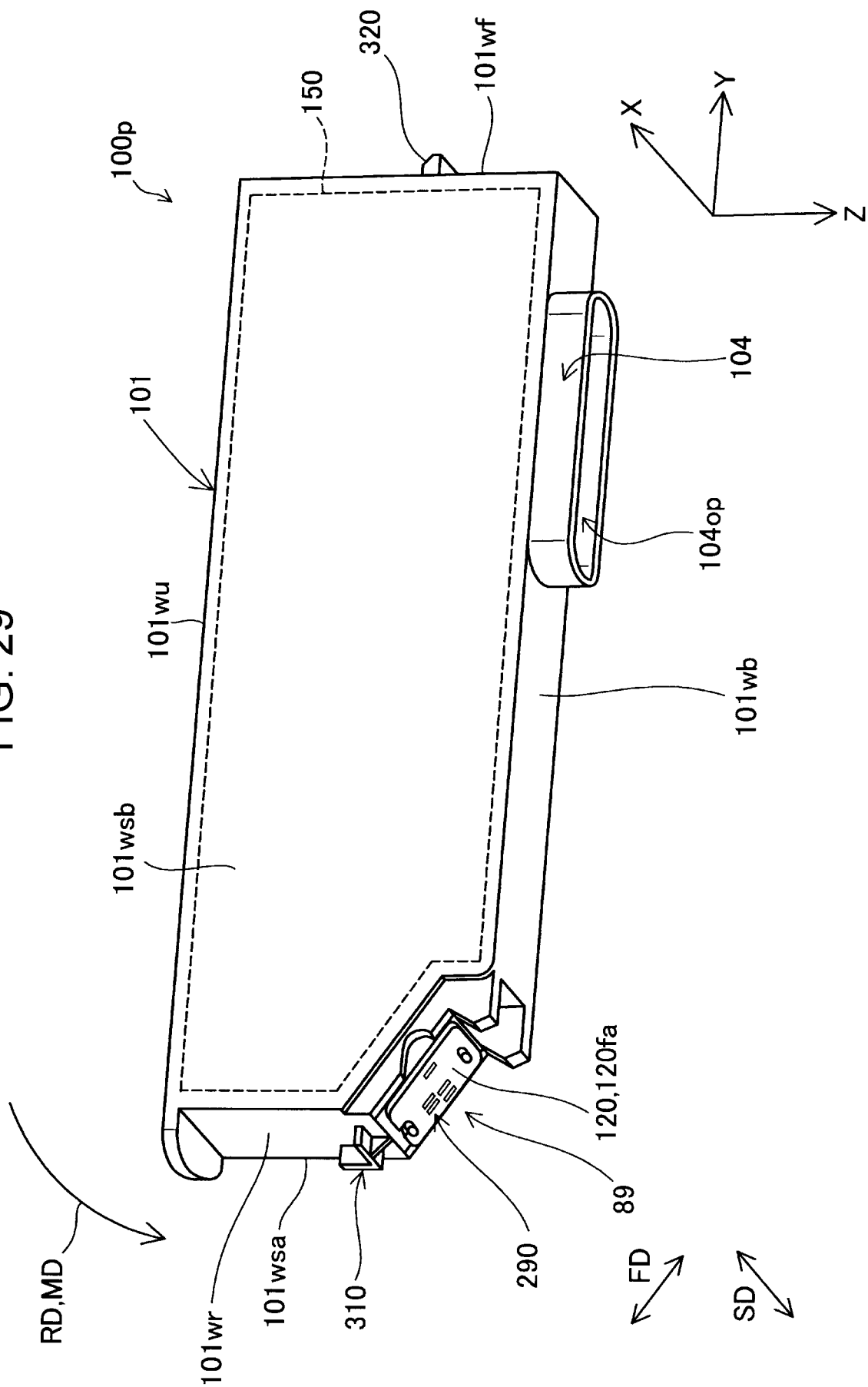
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FIG. 28



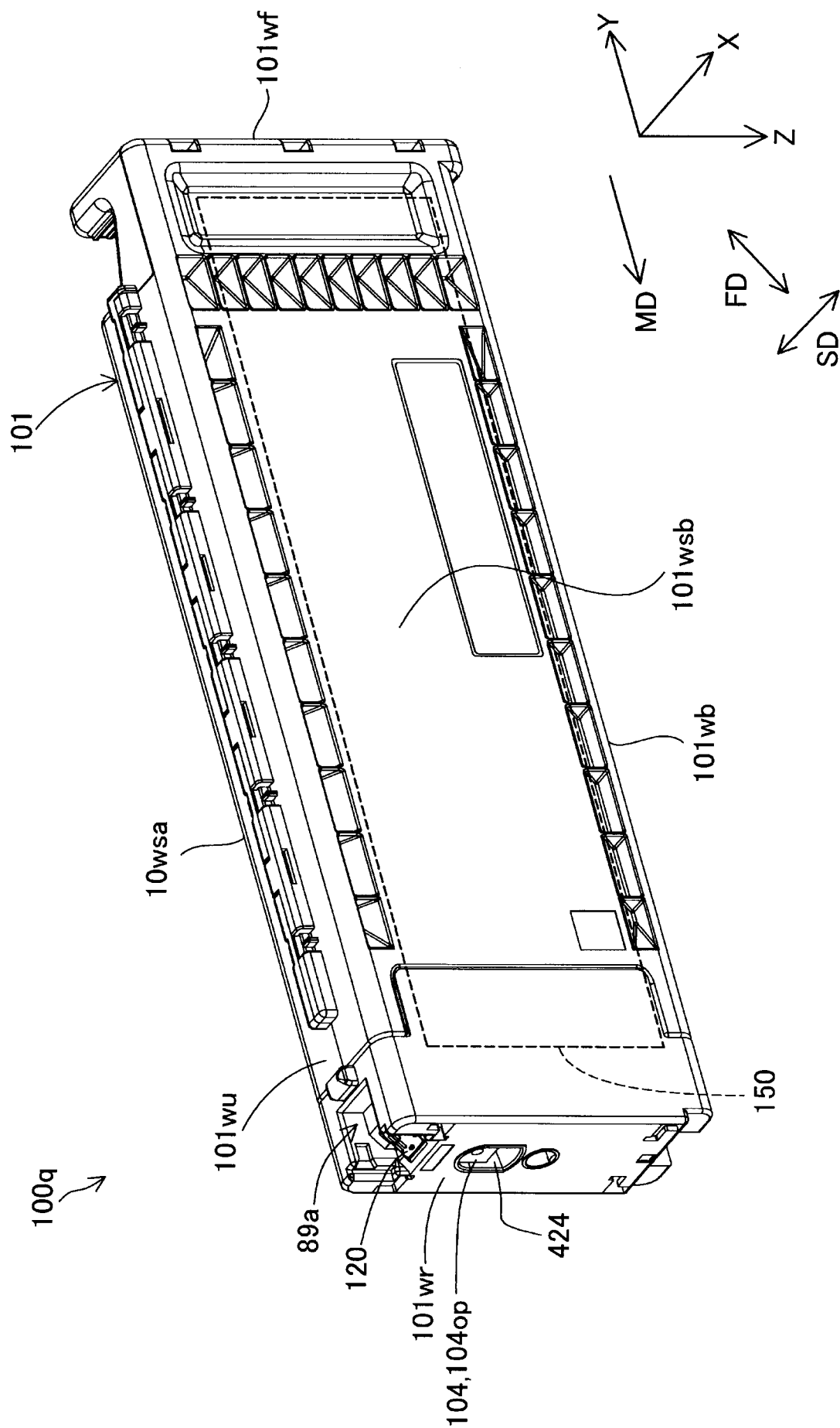
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FIG. 29



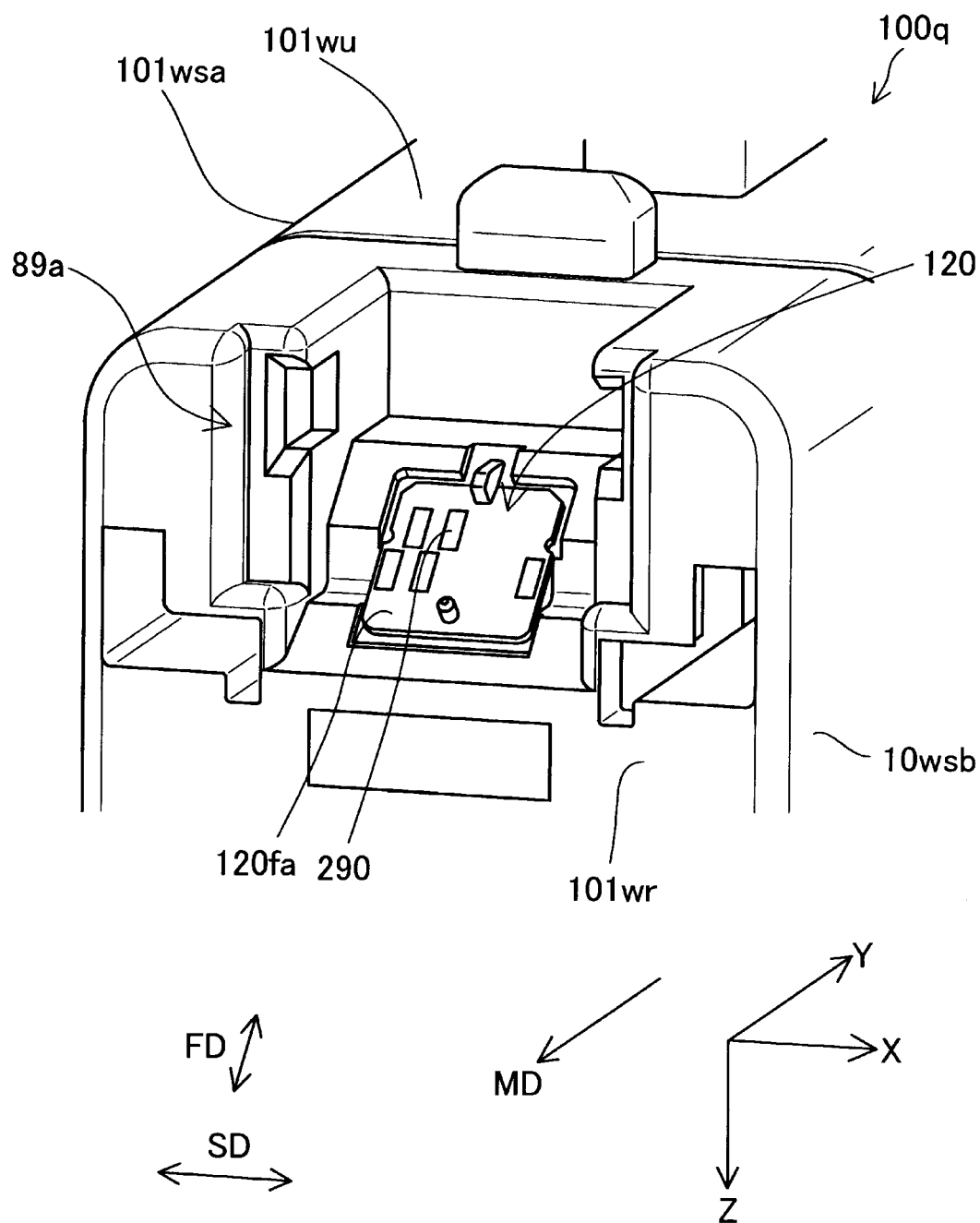
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FIG. 30



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FIG. 31



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FIG. 32

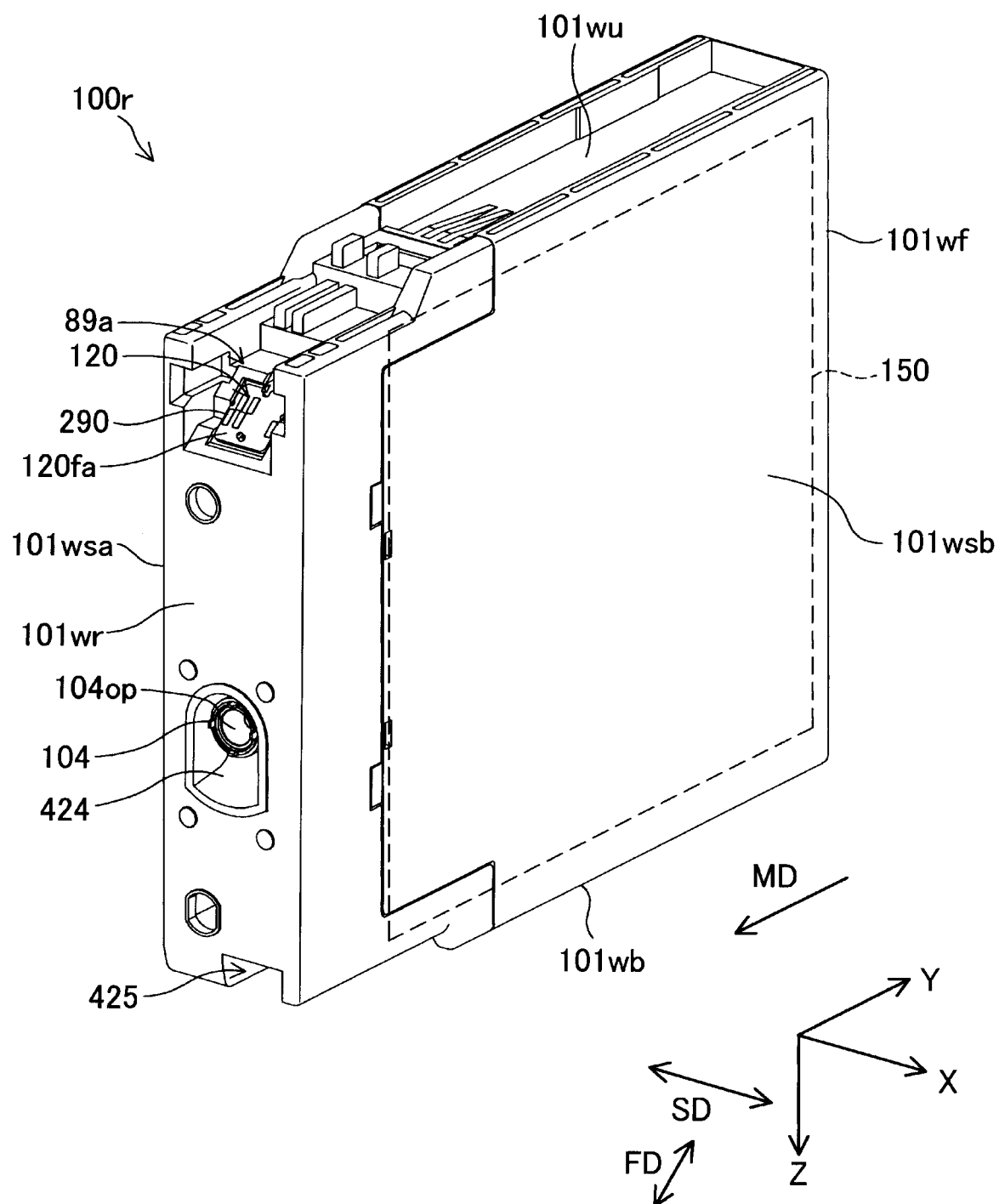
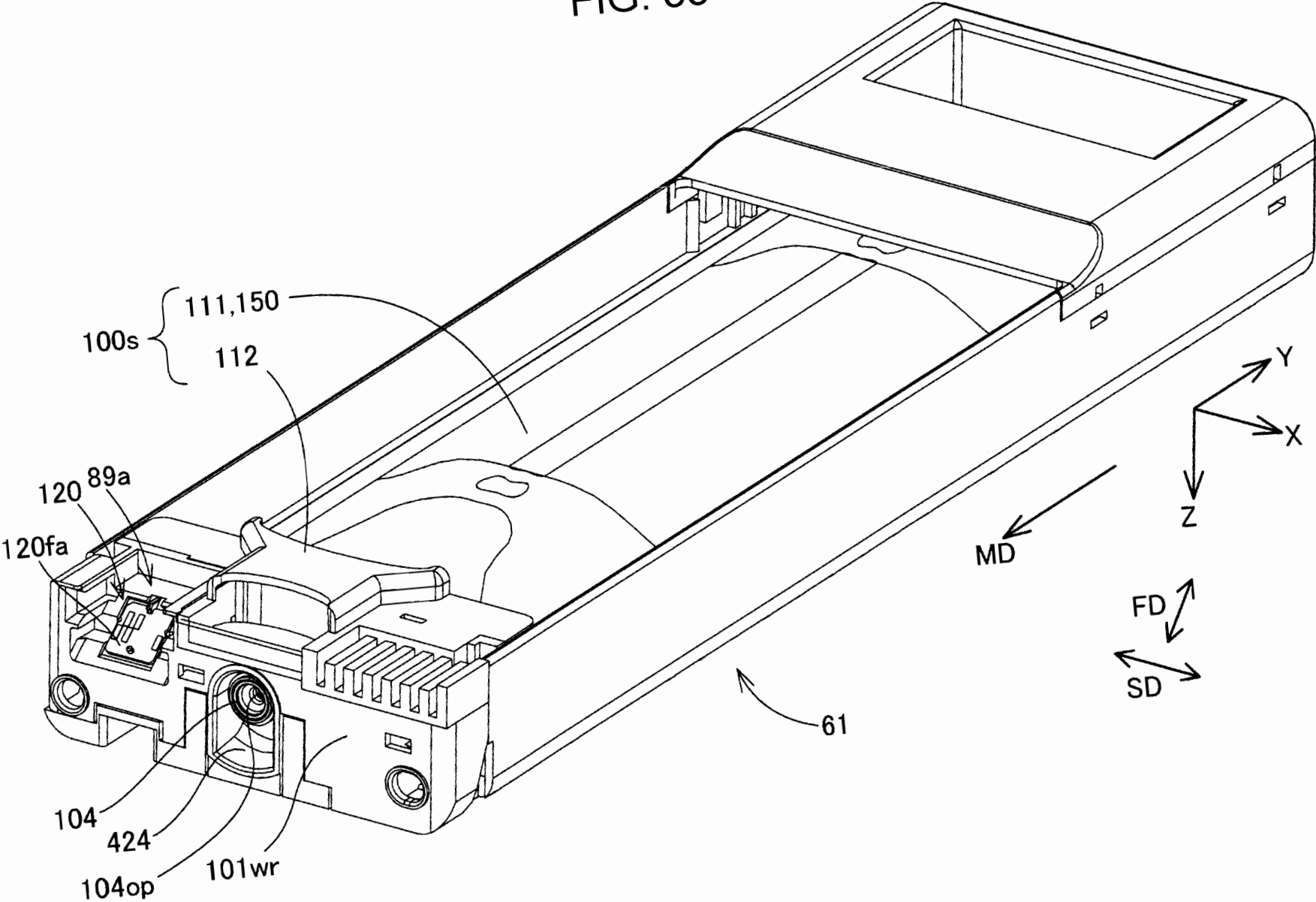


FIG. 33



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FIG. 34

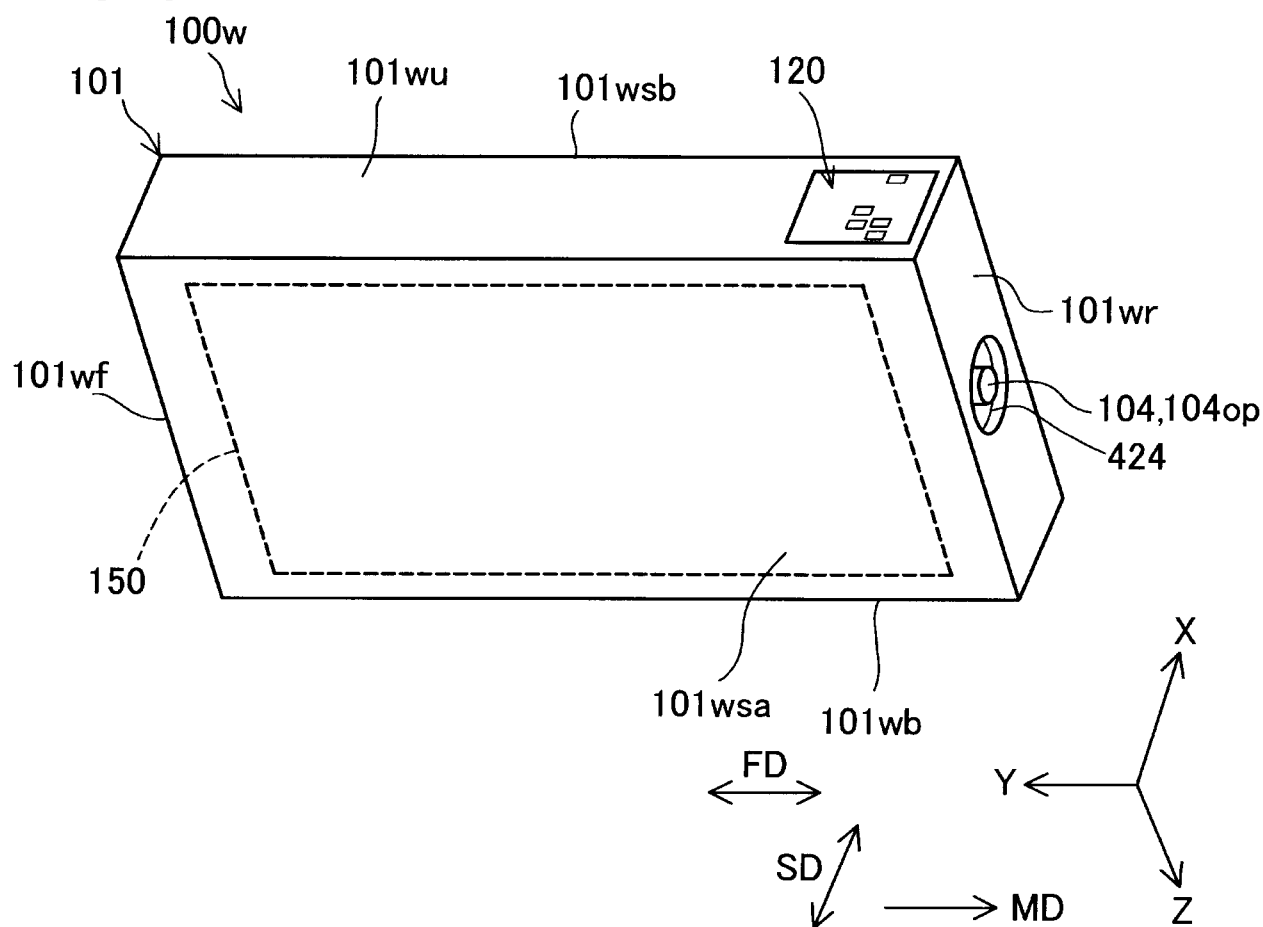
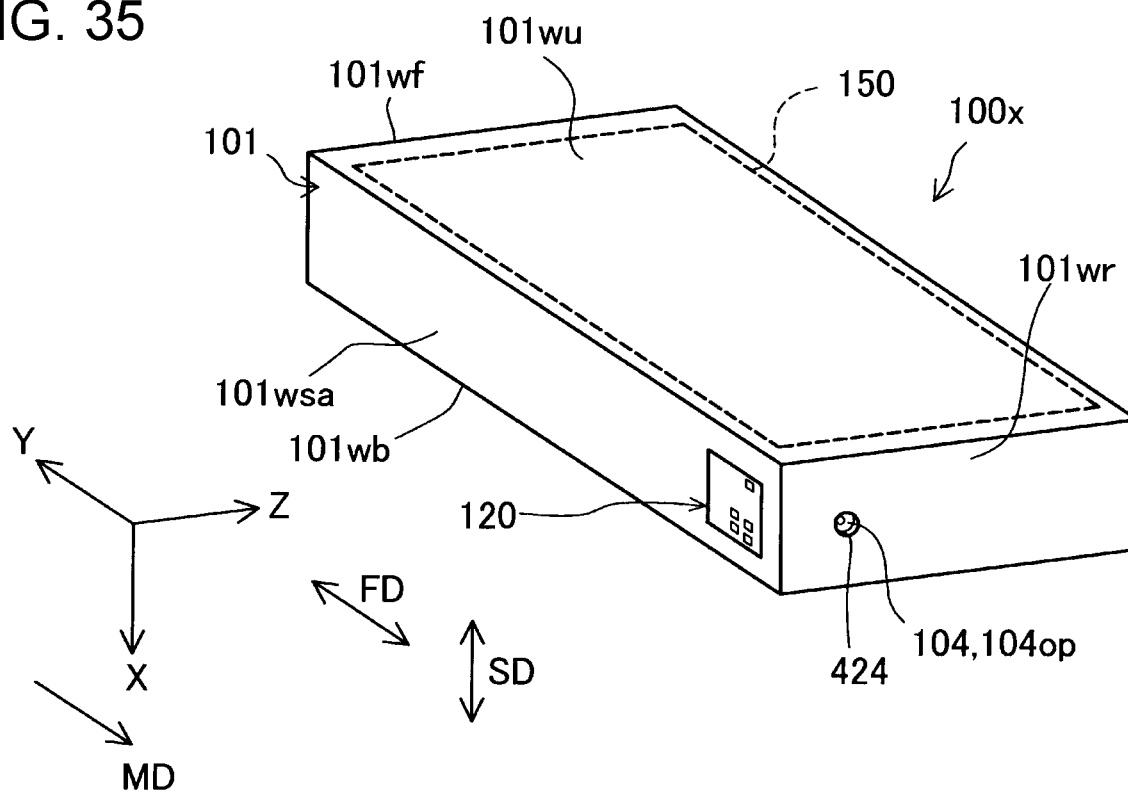
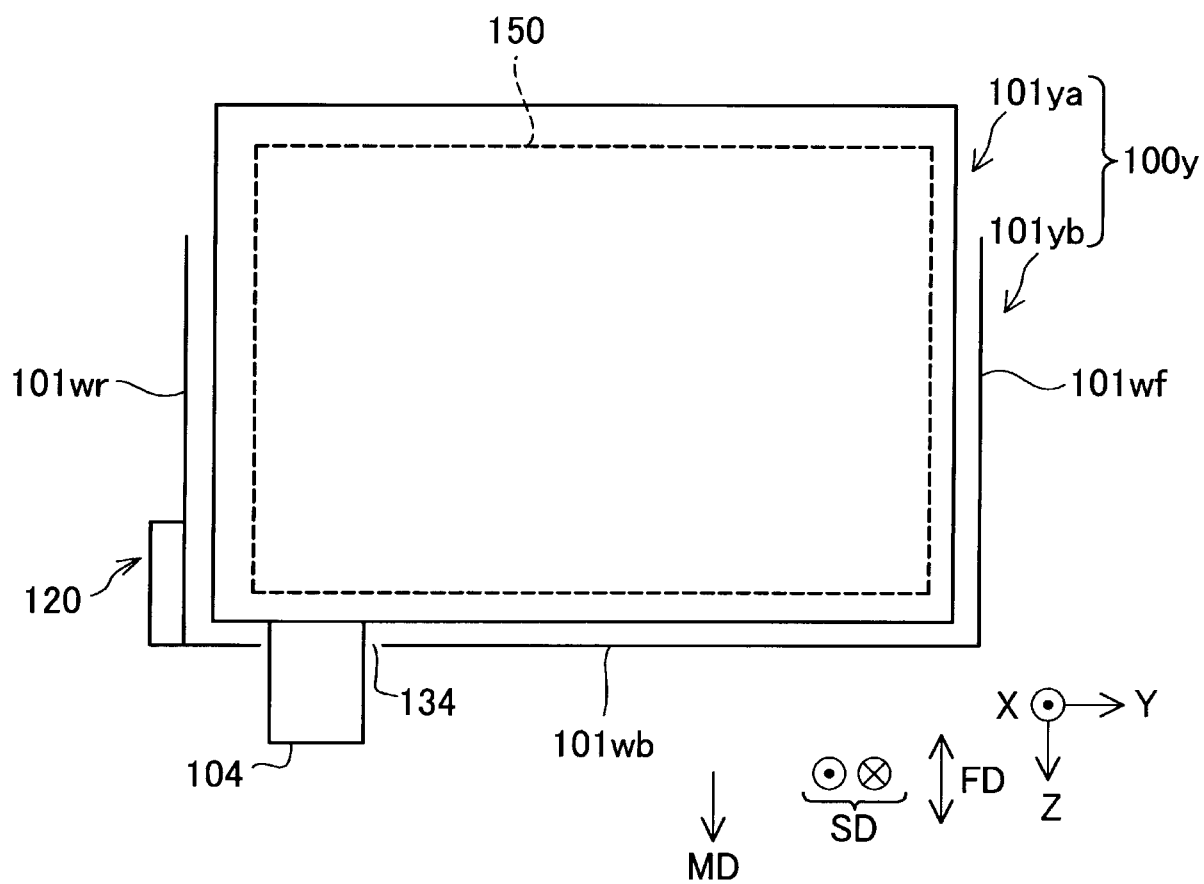


FIG. 35

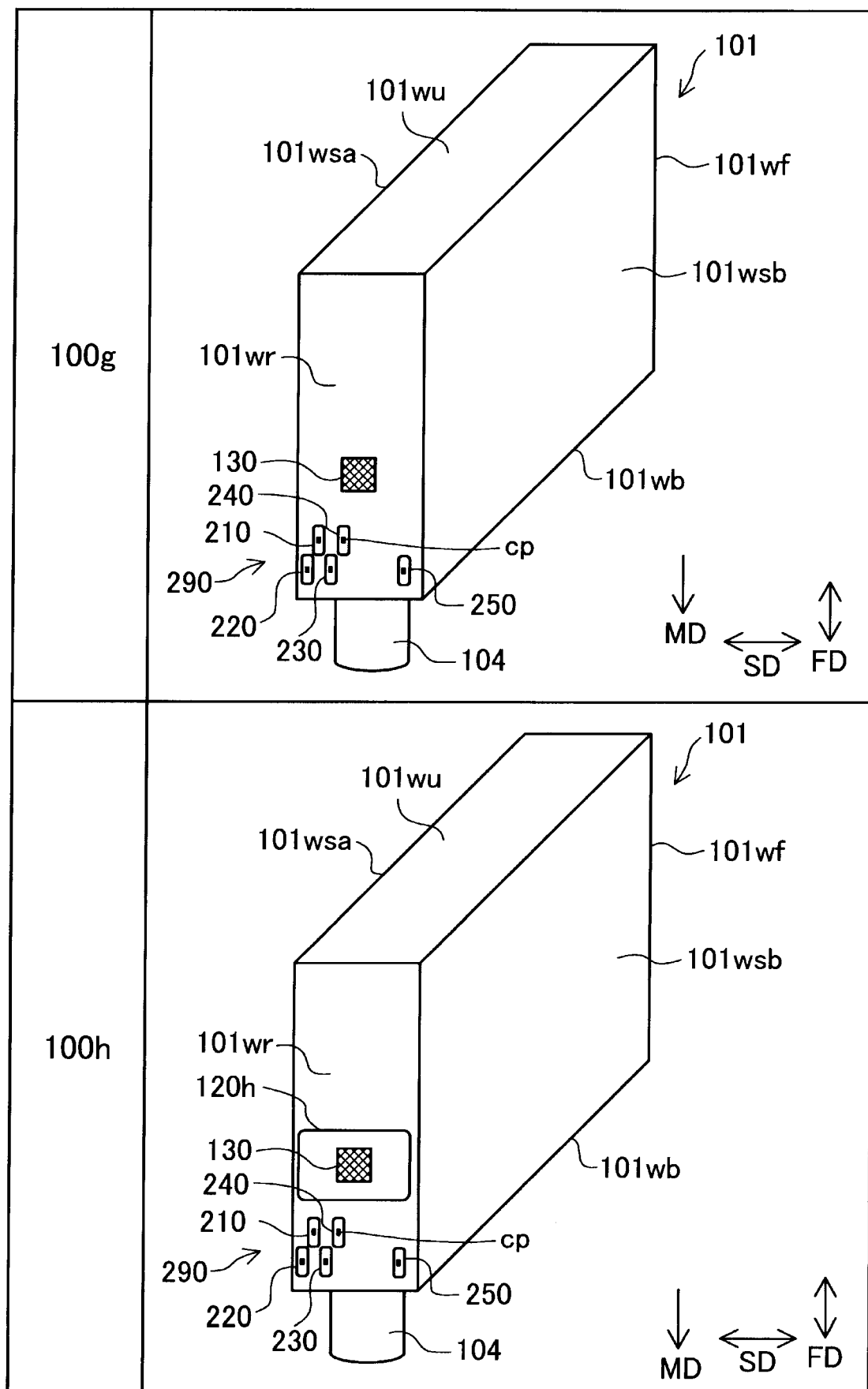


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FIG. 36

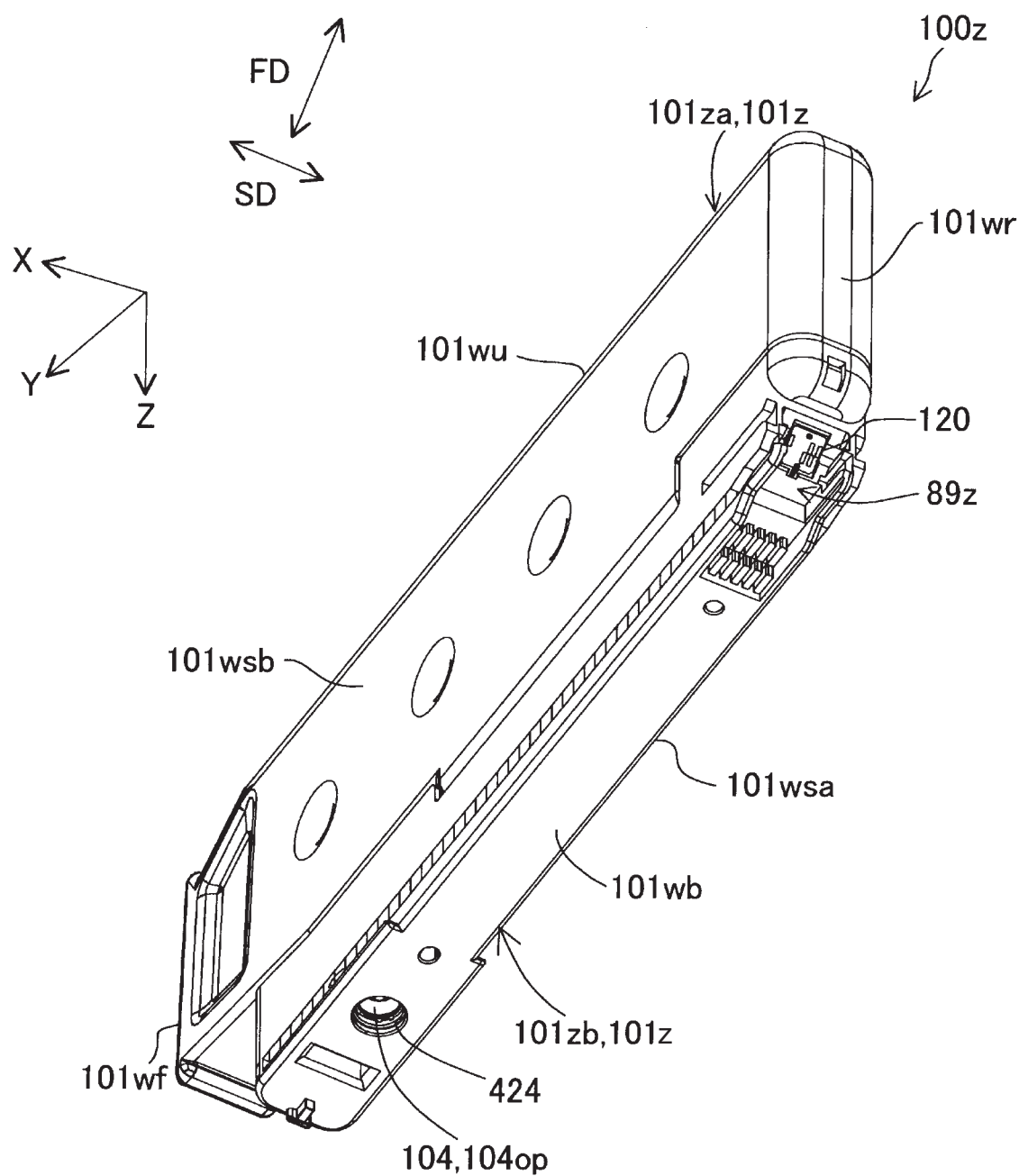


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FIG. 37



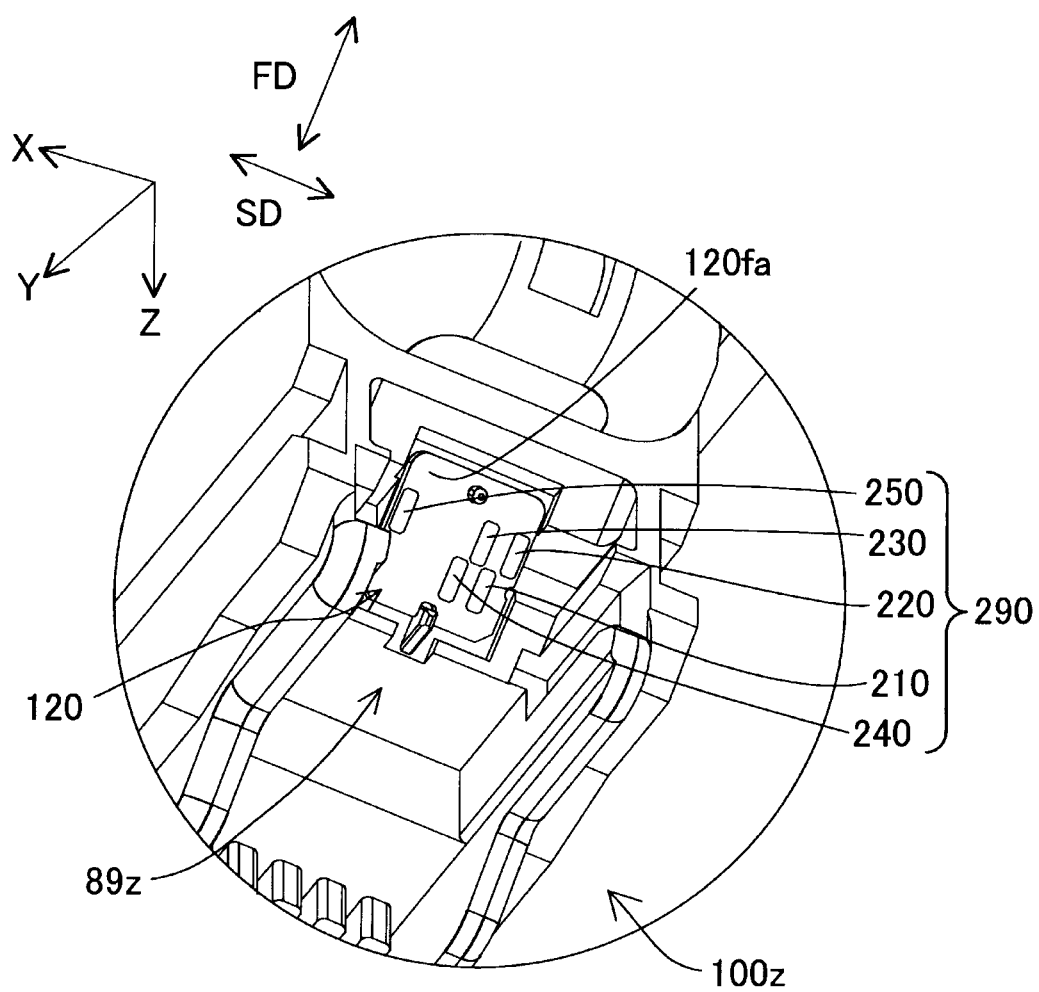
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FIG. 38



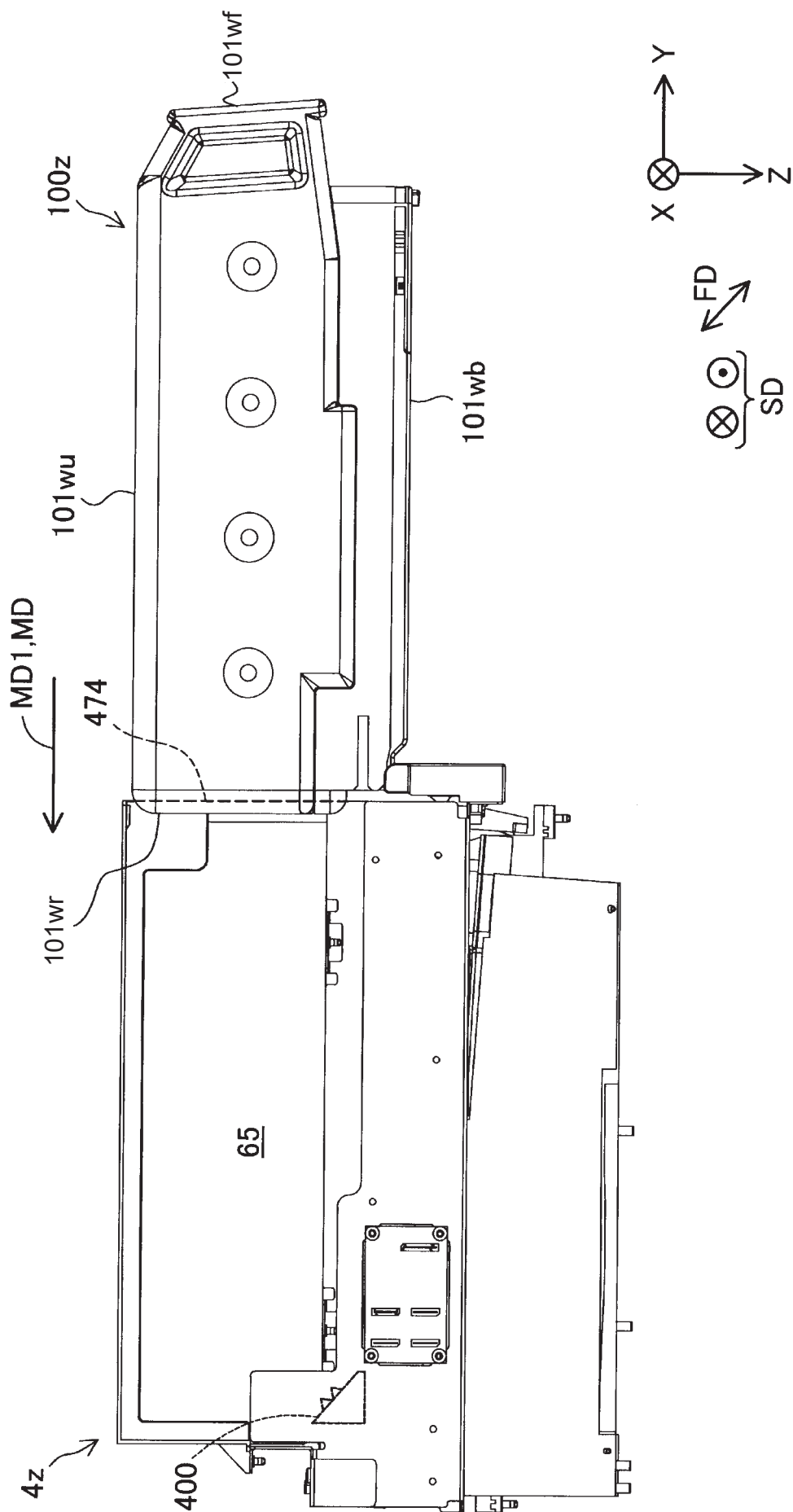
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FIG. 39



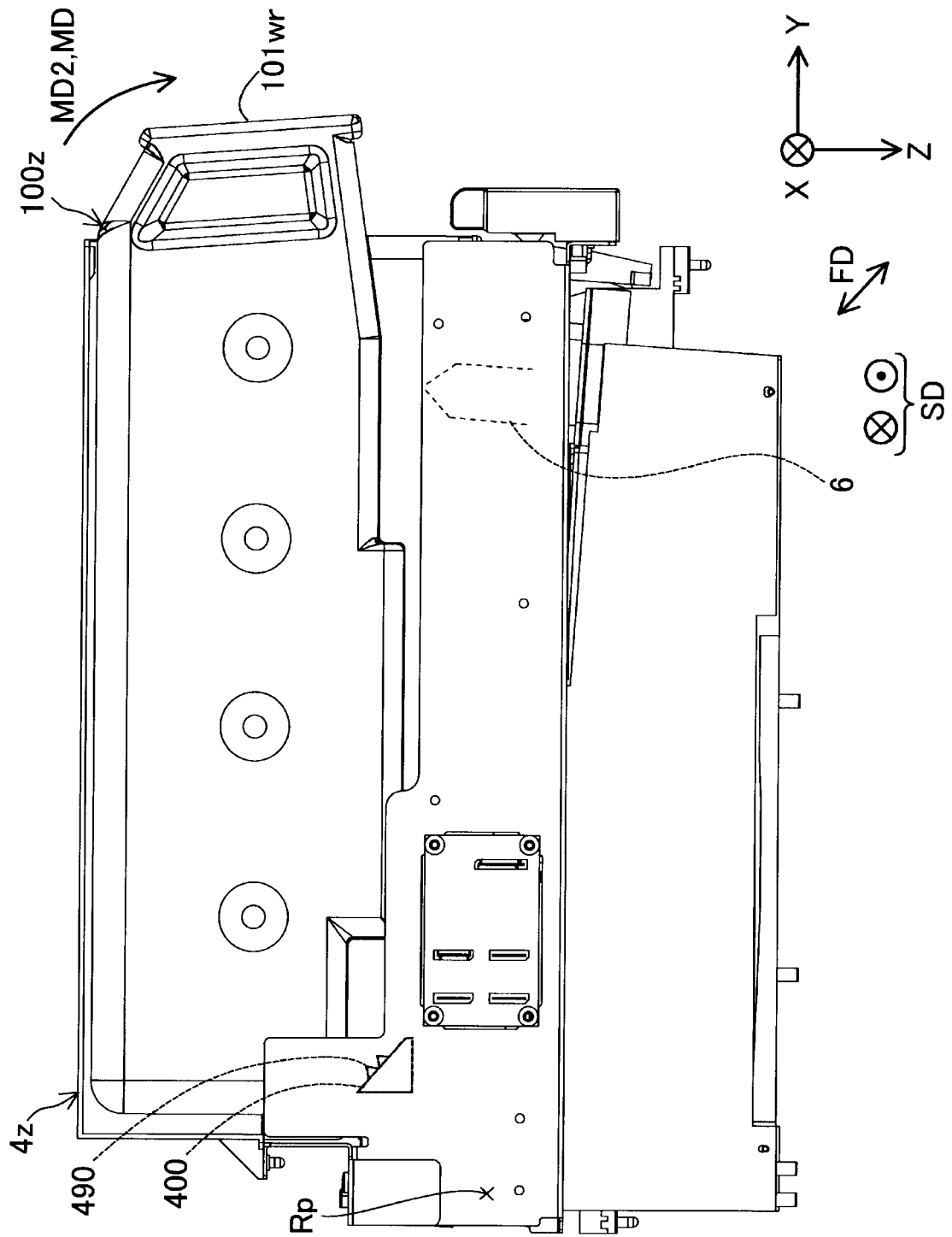
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FIG. 40



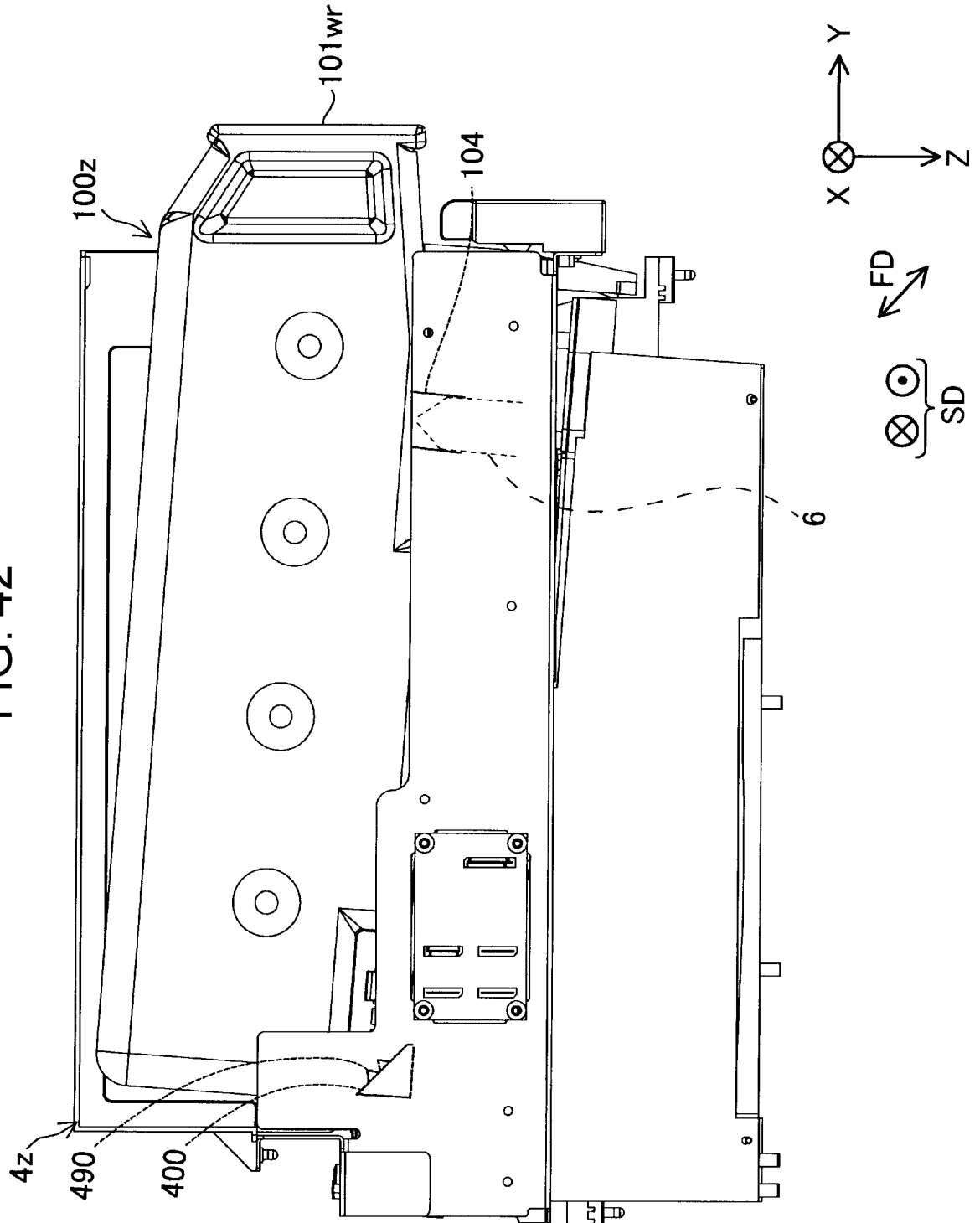
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FIG. 41



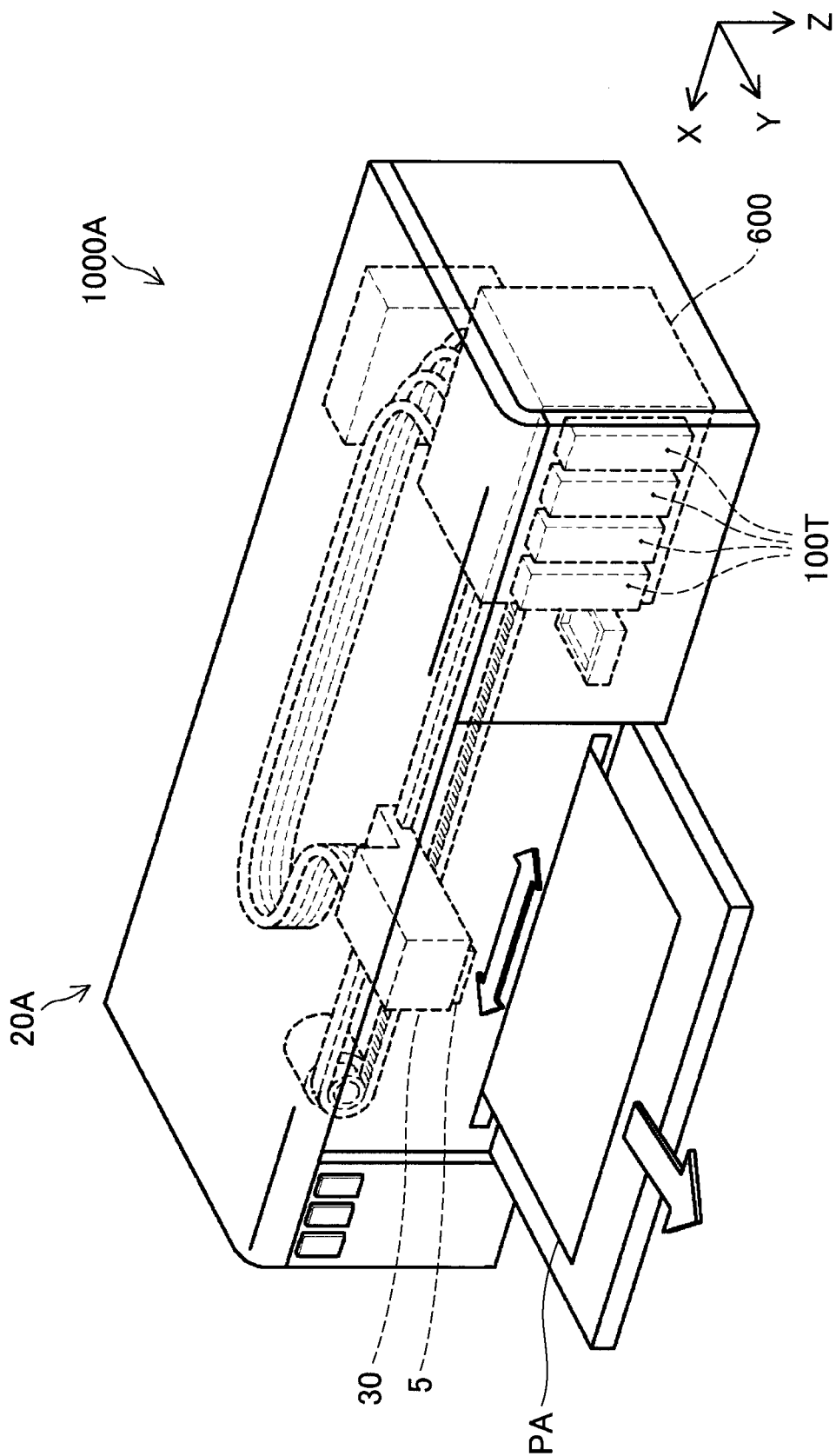
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FIG. 42



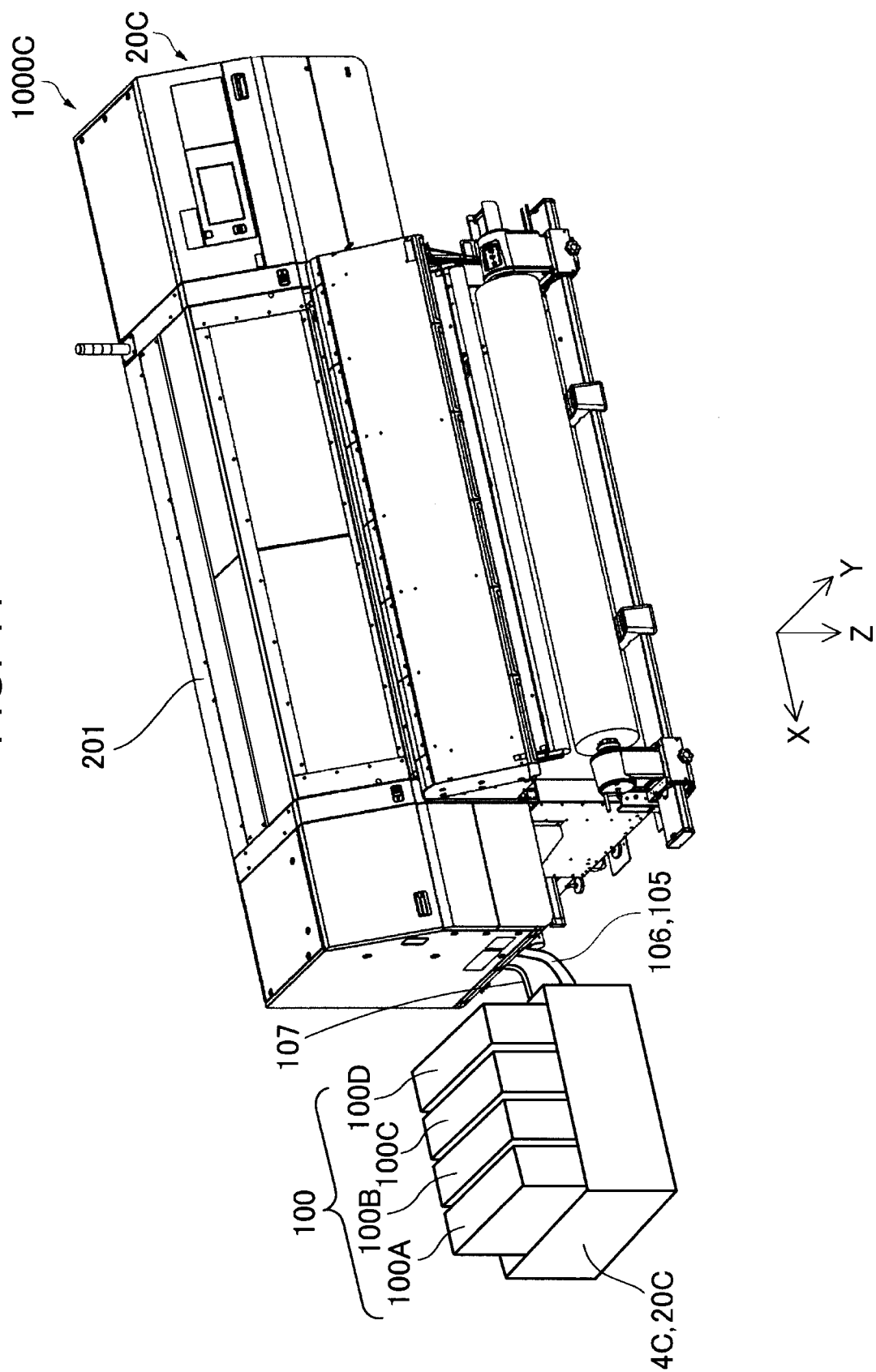
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FIG. 43



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FIG. 44



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FIG. 45

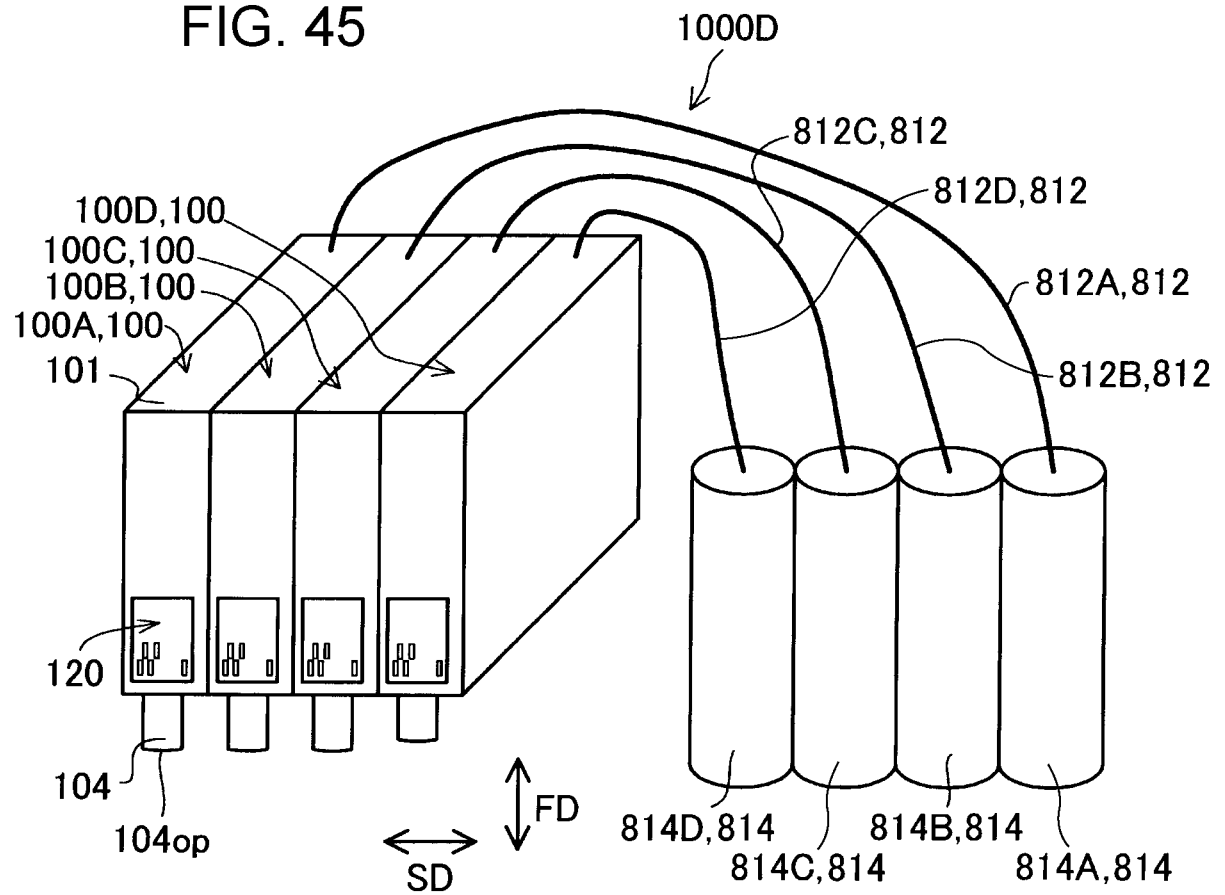


FIG. 46

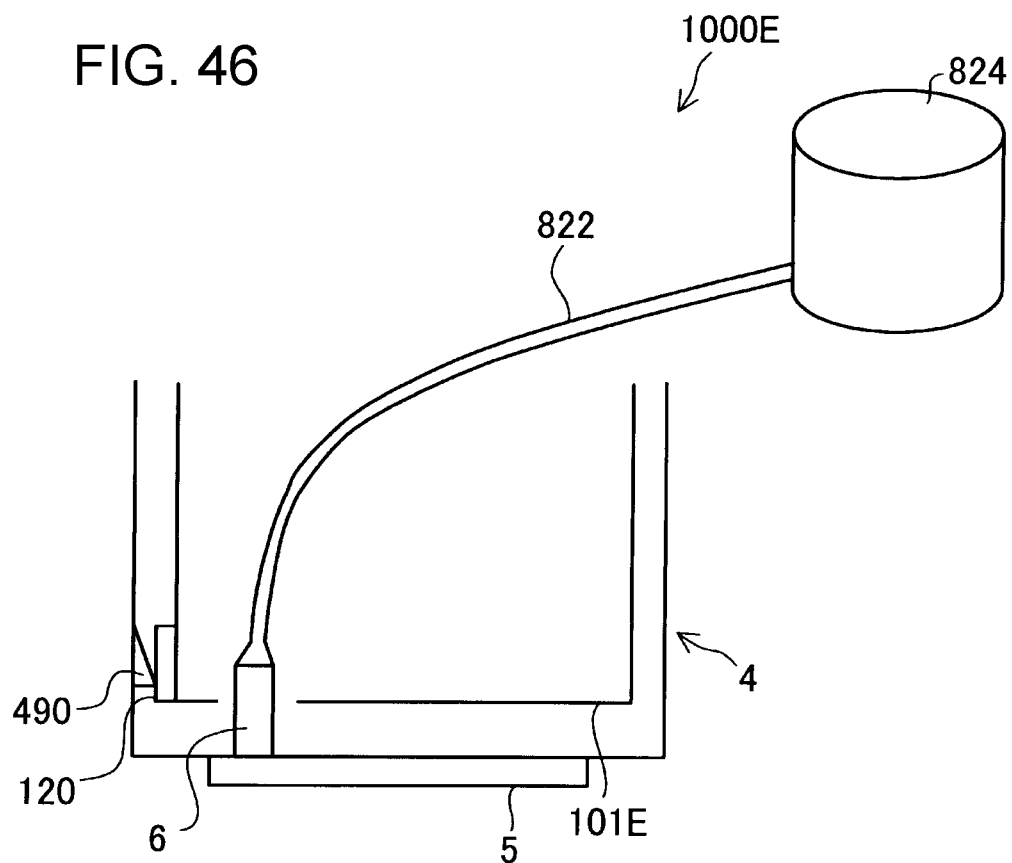


FIG. 47A

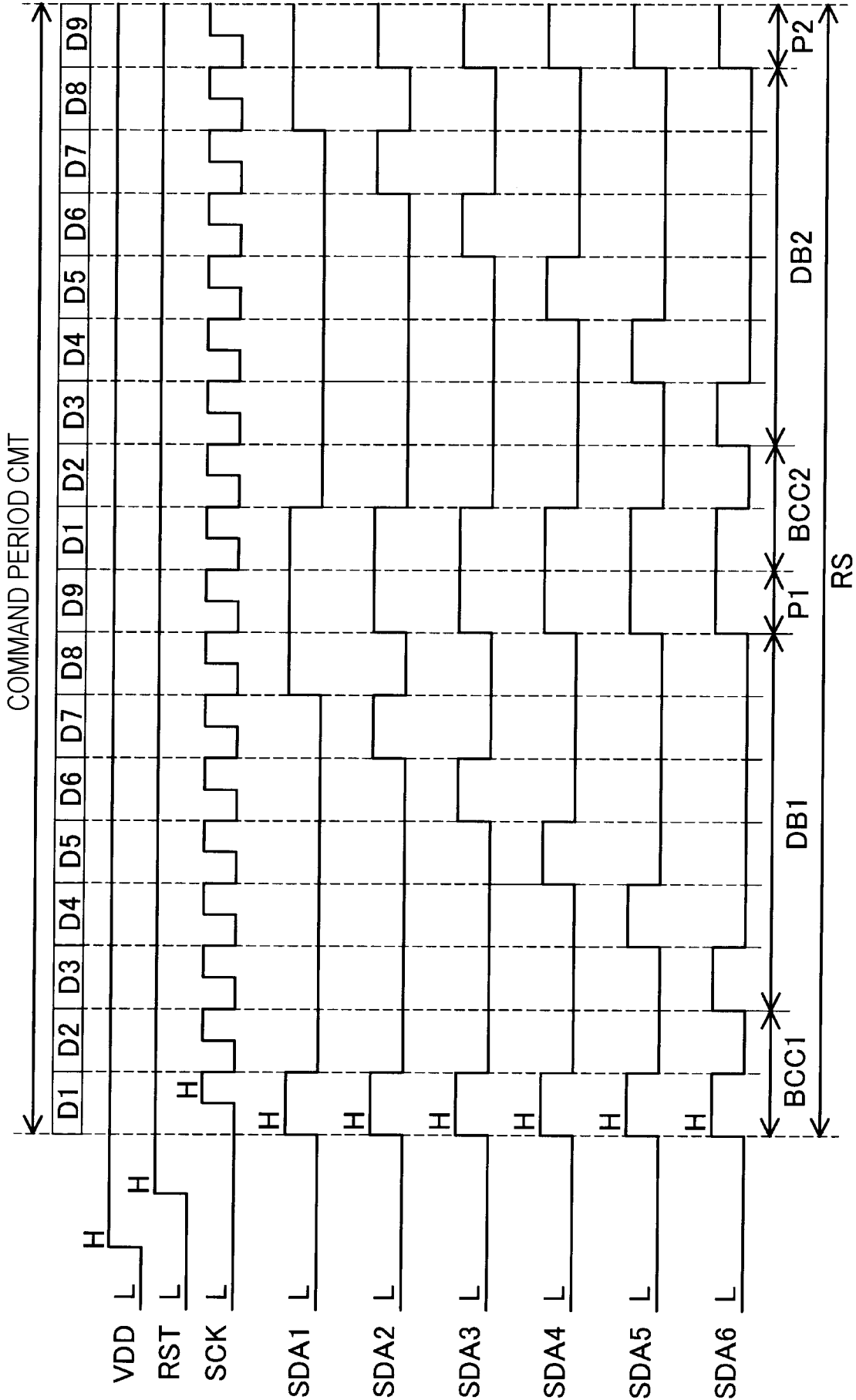


FIG. 47B

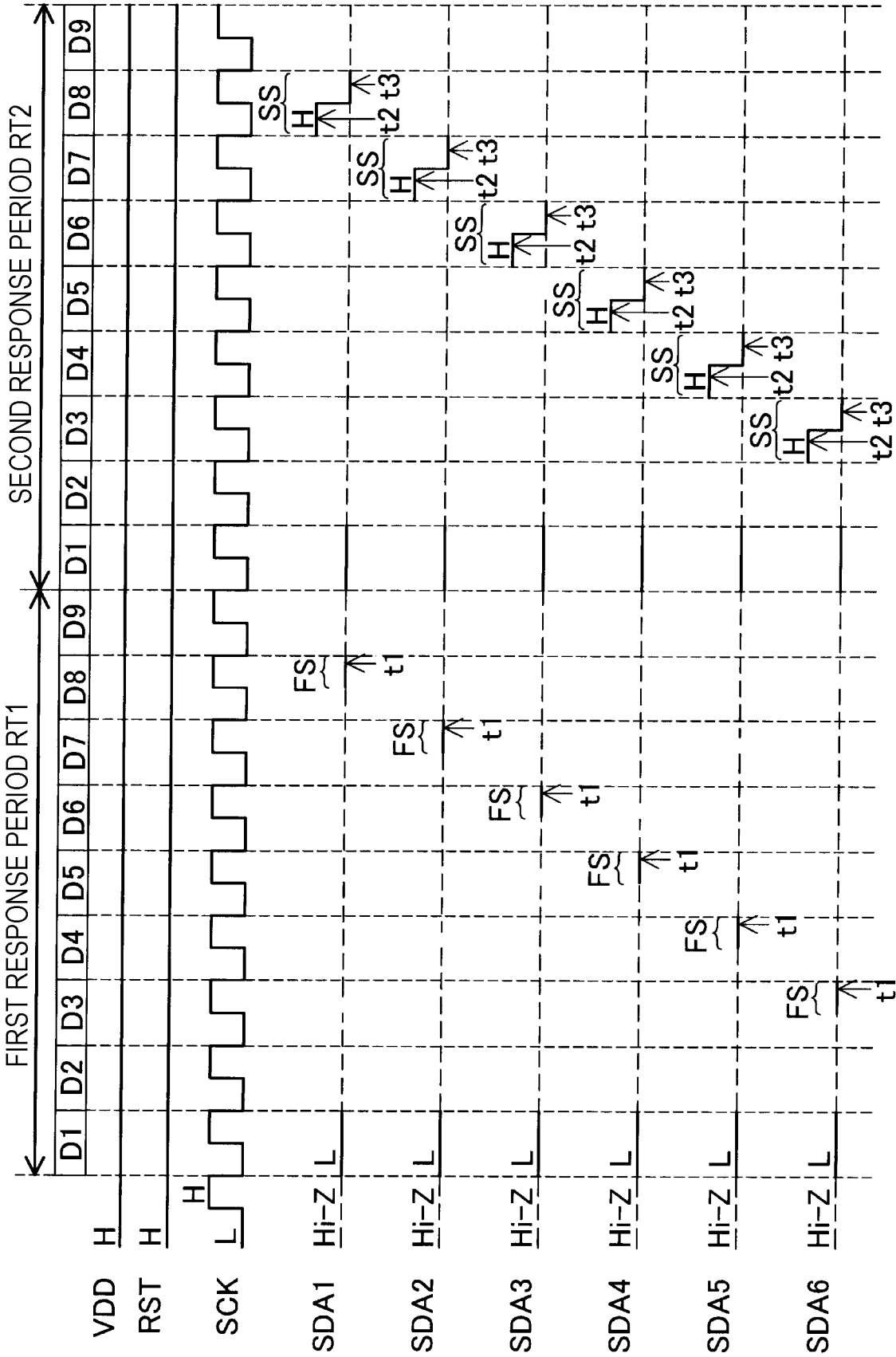
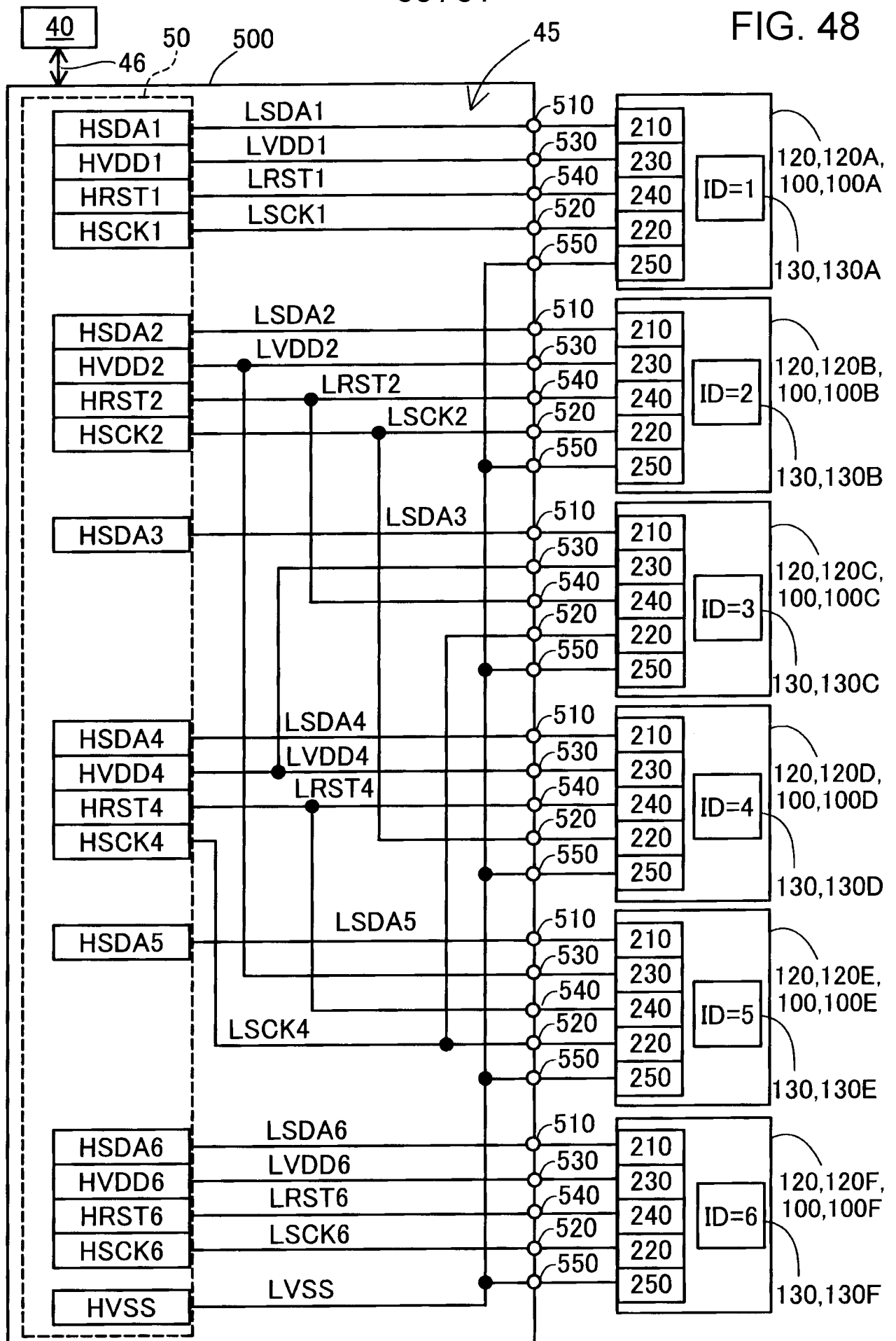


FIG. 48



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FIG. 49

