

Description

The invention relates to a Delta-Sigma modulator as set forth in the preamble of claim 1.

A modulator of this kind is disclosed in "IRE Transactions Space Electronics Telemetry", Vol. SET-8, pp. 204-209 (September 1962). In this paper the prior art, basically analog, delta-sigma modulator is presented and its utility as an improvement over the prior art Delta modulator is described.

The authors of the paper have pointed out that in the still earlier, so-called Delta modulation system, pulses are sent over a transmission line carrying information corresponding to the derivative of the input signal amplitude. At the receiving end, those pulses are integrated to obtain the original waveform. Transmission disturbances such as noise, etc., result in a cumulative error as a transmitted signal is integrated at the receiving end.

The so-called Delta-sigma modulation system provides for integration of the input signal before it enters the modulator itself so that the output transmitted pulses carry information corresponding to the amplitude of the input signal.

In a basically analog implementation, the behaviour of a Delta-Sigma modulator depends on the absolute value of capacitors and resistors in the circuits and, therefore, sensitivity to the detrimental effects of aging and temperature is encountered. Further, operational amplifiers included in analog implementations must be of superior quality, the gain and bandwidth of such amplifiers should not be such as to affect the transfer function of the integrator within the input circuitry of the device. Still further, in an analog implementation the waveform at the output of the digital to analog converter has to be precise and not pattern sensitive, that is a, pulse for an isolated "1" must be substantially identical to pulses imbedded in a series of "1-s". The circuit intricacies of analog Delta-Sigma modulator implementations are often the result of that requirement.

In view of the disadvantages of the prior art basically analog Delta-Sigma modulator, it is the general objective of the present invention to provide a Delta-Sigma modulator in which performance does not depend on the absolute value of capacitors and resistors as is the case with the prior art analog implementations. This object is attained as set forth in claim 1. Advantageous aspects and preferred embodiments are apparent from the subclaims.

The Delta-Sigma modulating characteristics are affected only by the ratio of capacitors. These ratios are relatively unaffected by temperature variations and aging. Absolute values of capacitors can be chosen so that the design of operational amplifiers is more flexible. For example, the larger the value of a capacitor, the larger is the slew rate requirement on the operational amplifier which is charging the

capacitor. However, the stray capacitance will be more effectively swamped. Conversely, a small capacitance is more easily charged, but the effect of stray capacitance is more pronounced. By leaving the absolute value of the capacitor as a design parameter, greater design latitude is possible in the overall Delta-Sigma modulator design.

Further, according to the switched capacitor implementation of the invention, operational amplifiers employed need only be able to charge and discharge circuit capacitors in a nominal time (on the order of one-half the sampling interval). This results in insensitivity to drift of element values caused by temperature and aging.

Further, a switched capacitor has an inherent sample and hold function at its input. Actually, the signals at all nodes in the circuit change at discrete instants of time. Consequently, the input to the comparator of the circuit is stable when the comparator makes a decision.

"ELECTRONIC ENGINEERING", Vol. 50, No. 602, February 1978, Pages 17 to 19, Fig. 2, discloses a circuit which has a few features in common with the circuit of the present invention. It has a clocked one-bit analog-to-digital converter at the output and a subcircuit at the input which consists of switches and capacitors. The circuit, referred to there as a delta-sigma converter, serves to measure very small AC currents, while the circuit of the present invention serves to digitally encode an analog input signal. The switches and capacitors do not form a sampling circuit because the switches are operated in the rhythm of the AC currents to be measured. By contrast, switches of a sampling circuit are typically operated with a sampling clock which is not correlated with the input signal and whose frequency is substantially higher than the highest frequency component of the input signal.

Basic circuitry, parameter identification and operational considerations are set forth in the detailed description of a preferred embodiment of the invention hereinafter presented.

Fig. 1 is a schematic block diagram representative of typical analog implementations according to the prior art.

Fig. 2 is a schematic block diagram basically representative of switched capacitor implementations.

Fig. 3 is a schematic diagram of an implementation of the Delta-Sigma modulator according to the invention employing +V and -V reference voltages.

Fig. 4 is a timing waveform presentation for the circuit of Fig. 3.

Fig. 5 shows a portion of a circuit of Fig. 4 with circuitry adapted to the use of a single reference voltage +V.

Fig. 6 illustrates the substitution of the single reference voltage circuitry of Fig. 5 into the device of Fig. 3.

At the outset, it should be pointed out that the term Delta-Sigma modulator is sometimes called a Sigma-Delta modulator, the transposition of the

sigma and delta terms being a matter of author's preference, the same device going under either name. Fig. 1 is prior art as aforementioned and substantially self-explanatory. In Fig. 1 herewith, the D/A converter would be a pulse shaper providing one of the two different pulses in accordance with whether the digital signal is high or low, mathematically $+A$ or $-A$, the quantity A being related to the conversion between a number and a voltage. The basically lowpass (integrating) device labelled $H(s)$ determines the order of the Delta-Sigma modulator. $H(s)$ is typically a first order filter if $H(s)$ is $=g/s$ and second order if

$$H(s) = \frac{g(s+c)}{(s+a)(s+b)}$$

It may be said that the modulator noise (inaccuracy of conversion of the input function to a digital signal) reduction achieved by the Delta-Sigma modulator is the result of keeping track of all previous conversion errors and feeding this information (as an error related signal) back to correct the next conversion. In this process, a first order modulator attempts to zero the average error over a period of time, whereas a second order modulator not only keeps this average error at zero but also keeps the first derivative of the error signal at zero.

In a first order system, only a DC input signal will be accurately represented digitally. However, in a second order system, the bandwidth of the signal which can be continuously represented digitally is increased.

According to known filter theory, the integrating filter $H(s)$ can be described for a first order Delta-Sigma modulator as:

$$H(s) = \frac{\alpha + \beta s}{1 + \eta s}$$

and similarly, for a second order filter

$$H(s) = \frac{\alpha + \beta s + \delta s^2}{1 + \eta s + s^2}$$

Capacitor and other component values are chosen to give appropriate values for the coefficients. Delta-Sigma modulation performance in terms of noise and stability is related to these coefficients. The paper cited hereinbefore provides an implementation and the underlying analysis of a "first-order" Delta-Sigma modulator. Figure 1 of that paper shows the "error signal", $S(t) - P(t)$ being applied to an integrator which has a first-order transfer-function and consequently is a "first-order Delta-Sigma modulator".

In Fig. 1 of that paper, the sampling pulse generator and pulse modulator together form an A/D+D/A operation. The pulse modulator outputs a pulse of known shape whose polarity is

determined by the polarity of the analog signal at the input of the pulse modulator at the instant the sampling pulse is asserted.

Higher order Delta-Sigma modulators provide, potentially, better noise behavior but are notorious for being unstable and are consequently not recommended. The second order embodiment herein described is regarded as optimum.

All switched capacitor implementations are generalized in Fig. 2 and can be, mathematically, reduced to the form shown below.

$H(z)$ is a discrete-time transfer function, of the form (for "second-order Delta-Sigma Modulator"):

$$H(z) = z^{-1} \left[\frac{\alpha + \beta z^{-1} + \eta z^{-2}}{1 + \delta z^{-1} + z^{-2}} \right] y$$

where z^{-1} is the unit delay operator, unit delay being the time of one sampling interval. For a sampling rate of 1 MHz, the sampling interval will be seen to be 1 μ s. The coefficients, which determine the noise performance and stability, are functions of capacitor ratios. The absolute value of each capacitor can be chosen by the circuit designer to optimize amplifier performance, to swamp stray capacitance, etc.

The switched capacitor Delta-Sigma modulator according to the invention is best explained in stages. The principle underlying the operation of any Delta-Sigma modulator is to provide an analog-to-digital conversion wherein the digital word size is small but the sampling frequency is much higher than the highest signal (speech) frequency.

First consider the sampling clock which operates the D type (edge-triggered) flip-flop, 20 in Fig. 3. This clock provides the time reference f_s and also two other clock waveforms, at the sampling frequency, but with duty cycle less than 50%. These are designated θ_1 ("charge") and θ_2 ("discharge"). Fig. 4 depicts these waveforms in a typical relationship.

Consider next a section of Fig. 3 consisting of switches 1 and 3, capacitor C_1 , amplifier 4 and capacitor C_3 . Here θ_1 from sampling clock 303 controls the switch 1 and θ_2 controls the switch 3. When θ_1 is low, switch 1 is open (open circuit) and when θ_1 is high, switch 1 is closed (short circuit). Similarly with θ_2 and switch 3. The non-overlapping nature of θ_1 and θ_2 ensures that switches 1 and 3 will not both be closed at any time. Assuming the input signal $u(t)$ remains constant over the interval $[nT, (n+1)T]$, capacitor C_1 will be charged during θ_1 , to a voltage equal to $u(nT)$. Assuming the amplifier, 4, is an ideal op-amp, during θ_2 all the charge on C_1 will be transferred to C_3 , causing a change in the voltage across C_3 of

$$-\frac{C_1 u(nT)}{C_3}$$

Consequently, at $t=(n+1)T$, the op-amp output voltage, x , will be

$$x[(n+1)T] = x(nT) - \left(\frac{C_1}{C_3}\right)u(nT),$$

the negative increment is because the amplifier inverts. Now consider the addition of switches 6, 7 and 9 and capacitor C_2 . If $b(n)$ is +1, i.e. $Q_n = \text{HIGH}$, then during θ_1 , C_2 would charge to $-V$. In short C_2 would charge to $-b(n) \cdot V$. During θ_2 this charge would be transferred to C_3 . The overall operation of switches 1, 3, 6, 7 and 9 and capacitors C_1 , C_2 and C_3 , and amplifier 4 can be described by the equation:

$$x[(n+1)T] = x(nT) - \left(\frac{C_1}{C_3}\right)u(nT) + b(n) \cdot V \cdot \left(\frac{C_1}{C_3}\right)$$

similarly,

$$w[(n+1)T] = w(nT) - \left(\frac{C_4}{C_6}\right)x(nT) - b(n) \cdot V \cdot \left(\frac{C_5}{C_6}\right)$$

The dotted enclosures 301 and 302 may be called reference switching means. The operation of the comparator and D flip-flop is to obtain

$$b(n+1) = \text{sgn}\{w[(n+1)T]\}.$$

The noise performance and stability of the Delta-Sigma modulator is governed by the capacitor ratios

$$\left(\frac{C_1}{C_3}\right), \left(\frac{C_2}{C_3}\right), \left(\frac{C_4}{C_6}\right) \text{ and } \left(\frac{C_5}{C_6}\right).$$

The voltage V is termed the "reference voltage" and normally all voltages are evaluated as fractions thereof. V is sometimes referred to as the "crash point" of the encoder and is the maximum amplitude of the input signal. An input amplitude of greater than V will cause overload.

For a typical Delta-Sigma modulator, the following capacitor ratios were found to be satisfactory.

$$\left(\frac{C_1}{C_3}\right) = \left(\frac{C_2}{C_3}\right) = \frac{1}{2}$$

$$\left(\frac{C_4}{C_6}\right) = \left(\frac{C_5}{C_6}\right) = 1$$

It will be noted that the configuration of Fig. 3 requires two reference voltages, $+V$ and $-V$. If only one reference, for example $+V$ is available, then the configuration consisting of $+V$, $-V$, switches 6, 7 and 9 and capacitor C_2 (similarly with $+V$, $-V$, switches 13, 14, 16 and capacitor C_5)

can be replaced by the circuit 501 shown in Fig. 5 and included in Fig. 6 as dotted block 601.

In that variation, and during each sampling interval, C_8 charges to V during θ_1 and during θ_2 causing a change of

$$-\left(\frac{C_8}{C_3}\right) \cdot V$$

in the output of amplifier 4.

During θ_1 , C_7 charges to V volts with the polarity indicated shown on Figs. 5 and 6. If Q_n were "high", i.e., $b(n) = +1$, switches 23 and 22 would close during θ_2 and, because of the polarity reversal, cause a change of

$$+\left(\frac{C_7}{C_3}\right) \cdot V$$

in the output of amplifier 4. If $b(n) = -1$, then C_7 does not discharge into C_3 . The net effect is then:

if $b(n) = +1$

$$\Delta x = \left(\frac{C_7}{C_3} - \frac{C_8}{C_3}\right) \cdot V - \left(\frac{C_1}{C_3}\right) \cdot u(nT)$$

or if $b(n) = -1$

$$\Delta x = -\left(\frac{C_8}{C_3}\right) \cdot V - \left(\frac{C_1}{C_3}\right) \cdot u(nT).$$

If $C_7 = 2C_8$, then the overall operation of the circuit in Fig. 5 can be described as

$$x[(n+1)T] = x(nT) - \left(\frac{C_1}{C_3}\right) \cdot u(nT) + b(n)V \cdot \left(\frac{C_8}{C_3}\right)$$

similarly

$$w[(n+1)T] = w(nT) - \left(\frac{C_4}{C_6}\right) \cdot x(nT) - b(n)V \cdot \left(\frac{C_{10}}{C_6}\right)$$

Implementing the Delta-Sigma modulator of the invention according to Fig. 6, the following capacitor ratios would be used:

$$\frac{C_8}{C_3} = \frac{C_1}{C_3} = \frac{1}{2}$$

$$\frac{C_4}{C_6} = \frac{C_{10}}{C_6} = 1$$

$$\frac{C_7}{C_8} = \frac{C_9}{C_{10}} = 2.$$

The sampling rate must be much higher than

the highest frequency component of the input signal $u(t)$. The invention is particularly useful for digitally encoding telephone (speech) band signals for transmission through a discrete telephonic channel. Since such signals require only a few kHz of bandwidth, and accordingly the sampling rate of 1MHz typical for the modulator of the invention fulfills the aforementioned requirement. A second order Delta-Sigma modulator can be considered to be constructed of a first order Delta-Sigma modulator embedded in a feedback loop. Conversely, a first order Delta-Sigma modulator can be considered to be a subset of a second order Delta-Sigma modulator obtained by "stripping" the second order Delta-Sigma modulator down. The configuration shown in Figures 3 or 6 can be stripped down to form a first order switched capacitor Delta-Sigma modulator. If amplifier 4, capacitors C_3 , C_1 , C_2 and their associated switches are removed, what remains is a first order Delta-Sigma modulator which converts an analog signal at u into a digital signal $b(n)$.

It is possible to transmit the bit-stream $\{b(n)\}$ as is and at the receiving end have a simple digital-to-analog converter which comprises of a pulse shaper which puts out distinct waveforms in a bit-interval according as $b(n)$ ="HIGH" or $b(n)$ ="LOW" followed by a simple analog lowpass filter to smooth the waveform. This, however, would entail the transmission of $\{b(n)\}$ directly, which is about 1 megabit/s which is quite high. An alternative method, is to employ a sequence of digital lowpass filters which do the "smoothing" while retaining the digital nature of the signal. As a consequence, the number of bits per word increases, that is the granularity of levels, which can be represented, is made fine. In a line circuit such as that of U.S. Patent No. 4,270,027 the lowpass filters permit the re-sampling of the digital signal at 8 Kilowords per sec with a granularity corresponding to 13 bits per word in a uniform code. Each code word can be converted into an 8-bit code, if so desired, corresponding to either the A-law or μ -law format. The 1-bit device, in this sense, does represent a large range of sample values from $u(n)$. The 1 bit/word, 1 Mword/sec stream (i.e. a 1-Megabit/sec stream) is sometimes referred to in the art as "PULSE-DENSITY MODULATED" version of the complex voice channel signal.

Claims

1. A Delta-Sigma modulator for digitally encoding an analog input signal, comprising
 —clock means (303) for generating a timing waveform (f_s) having first and second levels and a frequency substantially higher than the highest frequency component of said analog input signal;
 —integrating means (4, C_3) operative as a low-pass filter,
 —a one-bit analog-to-digital converter (19, 20) clocked by said timing waveform (f_s) and providing an output $b(n)$ as a function of the

instantaneous polarity of the output signal of said integrating means, characterized in

—that said clock means (303) generate, in addition said timing waveform (f_s), first and second switching gates (θ_1 , θ_2) within the duration of but not overlapping said timing waveform first and second levels, and in

—that it further comprises

—a first sampling circuit (1, 3, C_1) including switching capacitance means for storing charge representative of instantaneous amplitude values of said analog input signal ($u(t)$) under control of said first and second switching gates (θ_1 , θ_2) and having an output connected to the input of said integrating means, and

—reference means (301) controlled by said first and second switching gates (θ_1 , θ_2) and applying to the input of said integrating means a charging voltage derived from a fixed reference voltage ($+V$, $-V$) and corresponding in polarity to the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20).

2. A Delta-Sigma modulator as claimed in claim 1, characterized in that it further comprises:

—a second sampling circuit including switching capacitance means (10, 12, C_4) for storing charge representative of instantaneous amplitude values of the output signal ($x(nT)$) of said first integrating means (4, C_3) under control of said first and second switching gates (θ_1 , θ_2);

—second integrating means (17, C_6) operative as a second low-pass filter responsive to the output of said second sampling circuit (10, 12, C_4), said one-bit analog-to-digital converter (19, 20) being responsive to the output signal of said second integrating means (17, C_6), and

—second reference means (302) controlled by said first and second switching gates (θ_1 , θ_2) and applying to said second integrating means (17, C_6) a charging voltage derived from a fixed reference voltage ($+V$, $-V$) and corresponding in polarity to the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20).

3. A Delta-Sigma modulator as claimed in claim 2, characterized in that

—said first and second sampling circuits (1, 3, C_1 , 10, 12, C_4) are each operated to store during said first switching gate (θ_1) charge representative of the instantaneous amplitude value of their respective analog input signal and to output said stored charge during said second switching gate (θ_2), said first and second sampling circuits comprising first and second capacitors (C_1 , C_4) for charge storage and switching means associated therewith

—said first reference means (301) include a third capacitor (C_2) and additional switching means (6, 7, 9) connected to charge said third capacitor (C_2) to $+V$ or $-V$ reference voltage during said first switching gate (θ_1) in polarity corresponding to the logical value 1 or 0, respectively, of the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20), and to apply said

the highest frequency component of the input signal $u(t)$. The invention is particularly useful for digitally encoding telephone (speech) band signals for transmission through a discrete telephonic channel. Since such signals require only a few kHz of bandwidth, and accordingly the sampling rate of 1MHz typical for the modulator of the invention fulfills the aforementioned requirement. A second order Delta-Sigma modulator can be considered to be constructed of a first order Delta-Sigma modulator embedded in a feedback loop. Conversely, a first order Delta-Sigma modulator can be considered to be a subset of a second order Delta-Sigma modulator obtained by "stripping" the second order Delta-Sigma modulator down. The configuration shown in Figures 3 or 6 can be stripped down to form a first order switched capacitor Delta-Sigma modulator. If amplifier 4, capacitors C_3 , C_1 , C_2 and their associated switches are removed, what remains is a first order Delta-Sigma modulator which converts an analog signal at u into a digital signal $b(n)$.

It is possible to transmit the bit-stream $\{b(n)\}$ as is and at the receiving end have a simple digital-to-analog converter which comprises of a pulse shaper which puts out distinct waveforms in a bit-interval according as $b(n) = \text{"HIGH"}$ or $b(n) = \text{"LOW"}$ followed by a simple analog lowpass filter to smooth the waveform. This, however, would entail the transmission of $\{b(n)\}$ directly, which is about 1 megabit/s which is quite high. An alternative method, is to employ a sequence of digital lowpass filters which do the "smoothing" while retaining the digital nature of the signal. As a consequence, the number of bits per word increases, that is the granularity of levels, which can be represented, is made fine. In a line circuit such as that of U.S. Patent No. 4,270,027 the lowpass filters permit the re-sampling of the digital signal at 8 Kilowords per sec with a granularity corresponding to 13 bits per word in a uniform code. Each code word can be converted into an 8-bit code, if so desired, corresponding to either the A-law or μ -law format. The 1-bit device, in this sense, does represent a large range of sample values from $u(nT)$. The 1 bit/word, 1 Mword/sec stream (i.e. a 1-Megabit/sec stream) is sometimes referred to in the art as "PULSE-DENSITY MODULATED" version of the complex voice channel signal.

Claims

1. A Delta-Sigma modulator for digitally encoding an analog input signal, comprising

—clock means (303) for generating a timing waveform (f_s) having first and second levels and a frequency substantially higher than the highest frequency component of said analog input signal;

—integrating means (4, C_3) operative as a low-pass filter,

—a one-bit analog-to-digital converter (19, 20) clocked by said timing waveform (f_s) and providing an output ($b(n)$) as a function of the

instantaneous polarity of the output signal of said integrating means, characterized in

—that said clock means (303) generate, in addition said timing waveform (f_s), first and second switching gates (θ_1 , θ_2) within the duration of but not overlapping said timing waveform first and second levels, and in

—that it further comprises

—a first sampling circuit (1, 3, C_1) including switching capacitance means for storing charge representative of instantaneous amplitude values of said analog input signal ($u(t)$) under control of said first and second switching gates (θ_1 , θ_2) and having an output connected to the input of said integrating means, and

—reference means (301) controlled by said first and second switching gates (θ_1 , θ_2) and applying to the input of said integrating means a charging voltage derived from a fixed reference voltage ($+V$, $-V$) and corresponding in polarity to the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20).

2. A Delta-Sigma modulator as claimed in claim 1, characterized in that it further comprises:

—a second sampling circuit including switching capacitance means (10, 12, C_4) for storing charge representative of instantaneous amplitude values of the output signal ($x(nT)$) of said first integrating means (4, C_3) under control of said first and second switching gates (θ_1 , θ_2);

—second integrating means (17, C_6) operative as a second low-pass filter responsive to the output of said second sampling circuit (10, 12, C_4), said one-bit analog-to-digital converter (19, 20) being responsive to the output signal of said second integrating means (17, C_6), and

—second reference means (302) controlled by said first and second switching gates (θ_1 , θ_2) and applying to said second integrating means (17, C_6) a charging voltage derived from a fixed reference voltage ($+V$, $-V$) and corresponding in polarity to the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20).

3. A Delta-Sigma modulator as claimed in claim 2, characterized in that

—said first and second sampling circuits (1, 3, C_1 , 10, 12, C_4) are each operated to store during said first switching gate (θ_1) charge representative of the instantaneous amplitude value of their respective analog input signal and to output said stored charge during said second switching gate (θ_2), said first and second sampling circuits comprising first and second capacitors (C_1 , C_4) for charge storage and switching means associated therewith

—said first reference means (301) include a third capacitor (C_2) and additional switching means (6, 7, 9) connected to charge said third capacitor (C_2) to $+V$ or $-V$ reference voltage during said first switching gate (θ_1) in polarity corresponding to the logical value 1 or 0, respectively, of the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20), and to apply said



third capacitor voltage to said first integrating means input during said second switching gate (θ_2);

—and said second reference means (302) include a fourth capacitor (C_5) and second additional switching means (13, 14, 16) connected to charge said fourth capacitor (C_5) to +V or -V reference voltage during said first switching gate (θ_1) in polarity corresponding to the logical value 0 or 1, respectively, of the output ($b(n)$) of said one-bit analog-to-digital converter (19, 20), and to apply said fourth capacitor voltage to said second integrating means input during said second switching gate (θ_2).

4. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said first and second integrators comprise corresponding inverting first and second operational amplifiers (4, 17) having fifth and sixth capacitors (C_3 , C_6), connected between input and output of said first and second amplifiers (4, 17), respectively.

5. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said one-bit analog-to-digital converter comprises a comparator (19) responding to the preceding integrator to provide a polarity responsive output having a first or second condition, and a D type flip-flop circuit (20) responsive to said comparator output for providing Q and $\bar{Q}$ outputs, said Q output providing the one-bit code.

6. A Delta-Sigma modulator as claimed in claim 4, characterized in that the ratio of the capacitance of said first capacitor (C_1) to that of said fifth capacitor (C_3) and the capacitance ratio of said third capacitor (C_2) to that of said fifth capacitor (C_3) is approximately 1/2; the ratio of the capacitance of said second capacitor (C_4) to that of said sixth capacitor (C_6) and the capacitance ratio of said fourth capacitor (C_5) to that of said sixth capacitor (C_6) being unity.

7. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said clock means (303) is further defined as generating said switching gates (θ_1 , θ_2) each substantially time-centered with the duration of the corresponding timing gate waveform first and second levels.

8. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said first reference means (601) includes additional switching means (22, 24) associated with said third capacitor (C_7) for switching the terminal of said third capacitor (C_7) which is connected to ground potential to the positive terminal thereof during the time of $\theta_2 nQ$ and to the negative terminal thereof during θ_1 , said third capacitor voltage being outputted to said first integrating means (4, C_3) during $\theta_2 nQ$, and in that said second reference means (602) comprise second additional switching means (30, 33) associated with said fourth capacitor (C_5) for switching the terminal thereof which is connected to ground potential to the positive terminal thereof during the time $\theta_2 nQ$ and to the negative

terminal during θ_1 , said fourth capacitor voltage being outputted to said second integrating means (17, C_6) during $\theta_2 n\bar{Q}$, thereby to provide the function of said reference means using only a positive reference voltage (+V), where θ_1 and θ_2 are said first and second switching gates, and Q and $\bar{Q}$ are the logical value of the output of the one-bit analog-to-digital converter (19, 20) and the complement thereof, respectively.

9. A Delta-Sigma modulator as claimed in any one of the preceding claims, characterized in that said switching means comprise individual signal controlled electronic switches.

Patentansprüche

1. Delta-Sigma-Modulator zum digitalen Codieren eines analogen Eingangssignals, enthaltend

—eine Takteinrichtung (303) zum Erzeugen einer Taktimpulsfolge (f_s) mit einem ersten und einem zweiten Pegel und einer Frequenz, die wesentlich höher ist als die höchste Frequenzkomponenten des analogen Eingangssignals,

—eine Integrierschaltung (4, C_3), die als Tiefpaßfilter arbeitet,

—einen 1-Bit-Analog-Digital-Wandler (19, 20), dessen Takt die Taktimpulsfolge (f_s) ist und der ein Ausgangssignal ($b(n)$) liefert, das eine Funktion der momentanen Polarität des Ausgangssignals der Integrierschaltung ist, dadurch gekennzeichnet,

—daß die Takteinrichtung (303) zusätzlich zu der Taktimpulsfolge (f_s) eine erste und eine zweite Schalt-Taktimpulsfolge (θ_1 , θ_2) erzeugt, deren Impulse innerhalb der Dauer des ersten bzw. zweiten Pegels liegen und diese beiden Pegel nicht überlappen, und

—daß er weiter enthält:

—eine erste Abtastschaltung (1, 3, C_1), die Mittel enthält, um durch Schalten von Kapazitäten unter der Steuerung der ersten und zweiten Schalt-Taktimpulsfolge (θ_1 , θ_2) Ladungen zu speichern, die momentane Amplitudenwerte des analogen Eingangssignals ($u(t)$) repräsentieren, und die einen mit dem Eingang der Integrierschaltung verbundenen Ausgang hat, und

—eine Bezugsschaltung (301), die durch die erste und zweite Schalt-Taktimpulsfolge (θ_1 , θ_2) gesteuert wird und an den Eingang der Integrierschaltung (4, C_3) eine Ladespannung anlegt, die von einer festen Bezugsspannung (+V, -V) abgeleitet ist und in der Polarität dem Ausgangssignal ($b(n)$) des 1-Bit-Analog-Digital-Wandlers (19, 20) entspricht.

2. Delta-Sigma-Modulator nach Anspruch 1, dadurch gekennzeichnet, daß er weiter enthält:

—eine zweite Abtastschaltung (10, 12, C_4), die Mittel enthält, um durch Schalten von Kapazitäten unter der Steuerung der ersten und zweiten Schalt-Taktimpulsfolge (θ_1 , θ_2) Ladungen zu speichern, die momentane Amplitudenwerte des Ausgangssignals ($x(nT)$) der Integrierschaltung (4, C_3) repräsentieren,



—eine zweite Integrierschaltung (17, C_6), die als zweites Tiefpaßfilter arbeitet und deren Eingang mit dem Ausgang der zweiten Abtastschaltung (10, 12, C_4) verbunden ist und deren Ausgang mit dem Eingang der 1-Bit-Analog-Digital-Wandlers (19, 20) verbunden ist, und

—eine zweite Bezugsschaltung (302), die durch die erste und zweite Schalt-Taktimpulsfolge (θ_1 , θ_2) getrennt wird und an den Eingang der zweiten Integrierschaltung (17, C_6) eine Ladespannung anlegt, die von einer festen Bezugsspannung (+V, -V) abgeleitet ist und in der Polarität dem Ausgangssignal ($b(n)$) des 1-Bit-Analog-Digital-Wandlers (19, 20) entspricht.

3. Delta-Sigma-Modulator nach Anspruch 2, dadurch gekennzeichnet,

—daß die erste (1, 3, C_1) und zweite Abtastschaltung (10, 12, C_4) jeweils so betrieben wird, daß sie während eines Impulses der ersten Schalt-Taktimpulsfolge (θ_1) eine den momentanen Wert ihres jeweiligen analogen Eingangssignals repräsentierende Ladung speichert und diese gespeicherte Ladung während eines Impulses der zweiten Schalt-Taktimpulsfolge (θ_2) an ihren Ausgang abgibt, wobei die erste und die zweite Abtastschaltung einen ersten (C_1) bzw zweiten Kondensator (C_4) zum Speichern von Ladungen und dazugehörige Schaltmittel hat,

—daß die erste Bezugsschaltung (301) einen dritten Kondensator (C_2) und weitere Schaltmittel (6, 7, 9) enthält, die so geschaltet sind, daß der dritte Kondensator (C_2) während eines Impulses der ersten Schalt-Taktimpulsfolge (θ_1), auf die Bezugsspannung +V oder -V aufgeladen wird, wobei die Polarität dem logischen Wert 1 oder 0 des Ausgangssignals ($b(n)$) des 1-Bit-Analog-Digital-Wandlers (19, 20) entspricht, und daß die Spannung des dritten Kondensators (C_2) während eines Impulses der zweiten Schalt-Taktimpulsfolge (θ_2) an den Eingang der ersten Integrierschaltung (4, C_3) gelegt wird, und

—daß die zweite Bezugsschaltung (302) einen vierten Kondensator (C_5) und weitere Schaltmittel (13, 14, 16) enthält, die so geschaltet sind, daß der vierte Kondensator (C_5) während eines Impulses der ersten Schalt-Taktimpulsfolge (θ_1) auf die Bezugsspannung +V oder -V aufgeladen wird, wobei die Polarität dem logischen Wert 0 oder 1 des Ausgangssignals ($b(n)$) des 1-Bit-Analog-Digital-Wandlers (19, 20) entspricht, und daß die Spannung des vierten Kondensators (C_5) während eines Impulses der zweiten Schalt-Taktimpulsfolge (θ_2) an den Eingang der zweiten Integrierschaltung (17, C_6) gelegt wird.

4. Delta-Sigma-Modulator nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet, daß die erste und die zweite Integrierschaltung jeweils einen invertierenden Operationsverstärker (4, 17) und einen zwischen dessen Ausgang und Eingang geschalteten fünften (C_3) bzw. sechsten Kondensator (C_6) enthält.

5. Delta-Sigma-Modulator nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet,

daß der 1-Bit-Analog-Digital-Wandler einen Komparator (19) und ein D-Flipflop (20) enthält, wobei der Eingang des Komparators (19) mit dem Ausgang der vorgeschalteten Integrierschaltung (17, C_6) und der Eingang des D-Flipflops (20) mit dem Ausgang des Komparators (19) verbunden ist, der Komparator (19) ein von der Polarität seines Eingangssignals abhängiges Ausgangssignal mit einem ersten oder zweiten Zustand liefert und das D-Flipflop (20) Ausgangssignale Q und $\bar{Q}$ liefert, wobei das Q-Ausgangssignal den 1-Bit-Code bildet.

6. Delta-Sigma-Modulator nach Anspruch 4, dadurch gekennzeichnet, daß das Verhältnis der Kapazitäten des ersten (C_1) und des fünften Kondensators (C_3) sowie das Verhältnis der Kapazitäten des dritten (C_2) und des fünften Kondensators (C_5) ungefähr 1/2 beträgt und daß das Verhältnis der Kapazitäten des zweiten (C_4) und des sechsten Kondensators (C_6) sowie das Verhältnis der Kapazitäten des vierten (C_5) und des sechsten Kondensators (C_6) gleich 1 ist.

7. Delta-Sigma-Modulator nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet, daß die Takteinrichtung (303) die erste (θ_1) und zweite Schalt-Taktimpulsfolge (θ_2) derart erzeugt, daß die Impulse der ersten Schalt-Taktimpulsfolge (θ_1) und die Impulse der zweiten Schalt-Taktimpulsfolge zeitlich etwa in der Mitte der Dauer der ersten bzw. zweiten Pegel der Taktimpulsfolge (f_s) liegen.

8. Delta-Sigma-Modulator nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet,

—daß die erste Bezugsschaltung (601) weitere Schaltmittel (22, 24) enthält, die an den dritten Kondensator (C_2) so angeschaltet sind, daß sie während der Zeit von $\theta_2 n Q$ den positiven Anschluß des dritten Kondensators (C_2) und während θ_1 den negativen Anschluß dieses Kondensators mit Massepotential verbinden, wobei die Spannung des dritten Kondensators (C_2) während $\theta_2 n Q$ an die erste Integrierschaltung (4, C_3) angelegt wird.

—daß die zweite Bezugsschaltung (602) zwei weitere Schaltmittel (22, 24) enthält, die an den vierten Kondensator (C_5) so angeschaltet sind, daß sie während der Zeit von $\theta_2 n \bar{Q}$ den positiven Anschluß des vierten Kondensators (C_5) und während θ_1 den negativen Anschluß dieses Kondensators mit Massepotential verbinden, wobei die Spannung des vierten Kondensators (C_5) während $\theta_2 n \bar{Q}$ an die zweite Integrierschaltung (17, C_6) angelegt wird, wobei die Bezugsschaltungen (601, 602) nur eine positive Bezugsspannung (+V) verwenden und wobei θ_1 und θ_2 die positiven Pegel der ersten bzw. zweiten Schalt-Taktimpulsfolge (θ_1 , θ_2) und Q und $\bar{Q}$ die logischen Werte des Ausgangssignals des 1-Bit-Analog-Digital-Wandlers (19, 20) bzw. dessen Komplement sind.

9. Delta-Sigma-Modulator nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet, daß die Schaltmittel signalgesteuerte elektronische Schalter enthalten.



Revendications

1. Modulateur Sigma-Delta pour l'encodage numérique d'un signal d'entrée analogique, comprenant:

—des moyens d'horloge (303) engendrer un signal de rythme (f_s) ayant des premier et deuxième niveaux et possédant une fréquence sensiblement supérieure à la composante de fréquence la plus élevée dudit signal analogique d'entrée,

—des moyens d'intégration (4, C_3) opérant en filtre passe-bas,

—un convertisseur analogique-numérique à un bit (19, 20) cadencé par ledit signal de rythme f_s et fournissant un signal de sortie ($b(n)$) qui est fonction de la polarité instantanée du signal de sortie desdits moyens d'intégration, caractérisé en ce que:

—lesdits moyens d'horloge (303) engendrent, en plus dudit signal de rythme (f_s), un premier et un deuxième signal de commutation (θ_1 , θ_2) pendant la durée, mais sans recouvrement, desdits premier et deuxième niveaux du signal de rythme et

—le modulateur comprend en outre:

—un premier circuit d'échantillonnage (1, 3, C_1) incluant des moyens capacitif à commutation pour l'enregistrement de charges représentatives de valeurs d'amplitude instantanée dudit signal analogique d'entrée ($u(t)$) sous la commande desdits premier et deuxième signaux de commutation (θ_1 , θ_2) et ayant une sortie connectée à l'entrée desdits moyens d'intégration, et

—des moyens de référence (301) commandés par lesdits premier et deuxième signaux de commutation (θ_1 , θ_2) et appliquant à l'entrée desdits moyens d'intégration une tension de charge dérivée d'une tension de référence fixe (+V, -V) et correspondant à la polarité du signal de sortie ($b(n)$) dudit convertisseur analogique-numérique à un bit (19, 20).

2. Modulateur Sigma-delta conforme à la revendication 1, caractérisé en ce qu'il comprend en outre:

—un deuxième circuit d'échantillonnage comportant un moyen capacitif à commutation (10, 12, C_4) pour l'enregistrement de charges représentatives de valeurs d'amplitude instantanée du signal de sortie ($x(nt)$) desdits premiers moyens d'intégration (4, C_3), sous la commande desdits premier et deuxième signaux de commutation (θ_1 , θ_2),

—des deuxième moyens d'ingrations (17, C_6) opérant comme un filtre passe-bas répondant à la sortie dudit deuxième circuit d'échantillonnage (10, 12, C_4), ledit convertisseur analogique numérique à un bit (19, 20) répondant au signal de sortie desdits deuxième moyens d'intégration (17, C_6), et

—des deuxième moyens de référence (302) commandés par lesdits premier et deuxième signaux de commutation (θ_1 , θ_2) et appliquant auxdits deuxième moyens d'intégration (17, C_6)

une tension de charge dérivée d'une tension de référence fixe (+V, -V) et correspondant à la polarité de la sortie ($b(n)$) dudit convertisseur analogique-numérique à un bit (19, 20).

3. Modulateur Sigma-Delta conforme à la revendication 2, caractérisé en ce que:

—lesdits premier et deuxième circuits d'échantillonnage (1, 3, C_1 ; 10, 12, C_4) sont commandés chacun de manière à enregistrer au cours dudit premier signal de commutation (θ_1) un charge représentative de la valeur d'amplitude instantanée de leur signal d'entrée analogique respectif et pour fournir la charge enregistrée au cours dudit deuxième signal de commutation (θ_2), lesdits premier et deuxième circuits d'échantillonnage comprenant des premier et deuxième condensateurs (C_1 , C_4) pour l'enregistrement de charges ainsi que des moyens de commutation qui leur sont associés,

—lesdits premiers moyens de référence (301) comportent un troisième condensateur (C_2) et des moyens de commutation additionnels (6, 7, 9) connectés de manière à charger ledit troisième condensateur (C_2) à la tension de référence +V ou -V durant ledit premier signal de commutation (θ_1) avec une polarité correspondant respectivement à la valeur logique 1 ou 0 du signal de sortie ($b(n)$) dudit convertisseur analogique-numérique à un bit (19, 20), et à appliquer la tension dudit troisième condensateur auxdits premiers moyens d'intégration au cours dudit deuxième signal de commutation (θ_2),

—et lesdits deuxième moyens de référence (302) comportent un quatrième condensateur (C_5) et des deuxième moyens de commutation additionnels (13, 14, 16) connectés de manière à charger ledit quatrième condensateur (C_5) à la tension de référence +V ou -V au cours dudit premier signal de commutation (θ_1) avec une polarité correspondant respectivement à la valeur logique 0 ou 1 de la sortie ($b(n)$) dudit convertisseur analogique-numérique à un bit (19, 20), et à appliquer la tension dudit quatrième condensateur auxdits deuxième moyens d'intégration durant ledit deuxième signal de commutation (θ_2).

4. Modulateur Sigma-Delta conforme à l'une quelconque des revendications précédentes, caractérisé en ce que lesdits premier et deuxième intégrateurs comprennent des premier et deuxième amplificateurs opérationnels inverseurs correspondants (4, 17) comportant des cinquième et sixième condensateurs (C_3 , C_6), connectés respectivement entre l'entrée et la sortie de ces premier et deuxième amplificateurs (4, 17).

5. Modulateur Sigma-Delta conforme à l'une quelconque des revendications précédentes, caractérisé en ce que ledit convertisseur analogique-numérique à un bit comprend un comparateur (19) répondant à l'intégrateur qui le précède de manière à fournir un signal de sortie qui soit fonction de la polarité et possède un premier et un deuxième état, ainsi qu'une bascule de type D (20) répondant au signal de sortie dudit



comparateur pour fournir des signaux Q et $\bar{Q}$, ledit signal de sortie Q fournissant le code à un bit.

6. Modulateur Sigma-Delta conforme à la revendication 4, caractérisé en ce que le rapport de la capacité dudit premier condensateur (C_1) à celle dudit cinquième condensateur (C_5) et le rapport des capacités dudit troisième condensateur (C_3) et dudit cinquième condensateur (C_5) est approximativement $1/2$; le rapport de la capacité dudit deuxième condensateur (C_2) à celle dudit sixième condensateur (C_6) et le rapport des capacités dudit quatrième condensateur (C_4) et dudit sixième condensateur (C_6) étant égal à l'unité.

7. Modulateur Sigma-Delta conforme à l'une quelconque des revendications qui précèdent, caractérisé en ce que lesdits moyens d'horloge (303) sont en outre tels qu'ils produisent lesdits signaux de commutation (θ_1 , θ_2) de sorte que chacun d'eux soit temporellement centré par rapport aux premier et deuxième niveaux correspondants du signal de rythme.

8. Modulateur Sigma-Delta conforme à l'une quelconque des revendications qui précèdent, caractérisé en ce que lesdits premiers moyens de référence (601) comportent des moyens de commutation additionnels (22, 24) associés audit troisième condensateur (C_3) pour commuter à la

masse, durant le temps $\theta_2 nQ$, la borne positive de ce troisième condensateur (C_3) et, durant le temps θ_1 , sa borne négative, la tension dudit troisième condensateur étant fournie auxdits premiers moyens d'intégration (4, C_3) durant $\theta_2 nQ$, et en ce que lesdits deuxième moyens de référence (602) comprennent des deuxième moyens de commutation additionnels (30, 33) associés audit quatrième condensateur (C_4) pour commuter à la masse, durant le temps $\theta_2 nQ$ la borne positive de ce quatrième condensateur (C_4) et, durant le temps θ_1 , sa borne négative, la tension dudit quatrième condensateur étant fournie auxdits deuxième moyens d'intégration (17, C_4) durant $\theta_2 nQ$, de manière telle que la fonction desdits moyens de référence est remplie en utilisant la tension de référence positive (+V) seulement, θ_1 et θ_2 étant respectivement lesdits premier et deuxième signaux de commutation et Q et $\bar{Q}$ étant respectivement la valeur logique du signal de sortie du convertisseur analogique-numérique à un bit (19, 20) et le complément de celle-ci.

9. Modulateur Sigma-Delta conforme à l'une quelconque des revendications précédentes caractérisé en ce que lesdits moyens de commutation comprennent des commutateurs électroniques commandés par des signaux individuels.



* C L M S *