SEMICONDUCTOR EMBEDDED RESISTOR GENERATION

Abstract of the Disclosure

A method for generating an embedded resistor in a semiconductor device are provided, the method including forming a shallow trench isolation (STI) region in a substrate; forming a pad oxide on the STI region and substrate; depositing a silicon layer on the pad oxide; forming a photo-resist mask on a portion of the silicon layer; etching the silicon layer to yield a poly-conductor (PC); oxidizing the PC; depositing at least one of an oxide material or a metal gate material on the oxidized surface; depositing a silicon layer on the at least one oxide material or metal gate material; patterning a transistor gate structure disposed substantially away from the STI region.

Fig. 15