

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) semiconductor memory device comprising:
 - an electrode structure comprising electrodes vertically stacked on a semiconductor layer;
 - a vertical semiconductor pattern penetrating the electrode structure and connected to the semiconductor layer;
 - a vertical insulating pattern disposed between the electrode structure and the vertical semiconductor pattern; and wherein the vertical insulating pattern comprises:
 - a sidewall portion on a sidewall of the electrode structure; and
 - a protrusion extending from the sidewall portion on a portion of a top surface of the semiconductor layer,
 - wherein the vertical semiconductor pattern comprises:
 - a vertical channel portion having a first thickness and extending along the sidewall portion of the vertical insulating pattern;
 - a contact portion extending from the vertical channel portion and conformally along the protrusion of the vertical insulating pattern and the top surface of the semiconductor layer; and
 - a bottom portion of the contact portion conformally covering a recessed region of the top surface of the semiconductor layer,
 - wherein the contact portion has a second thickness in a first direction parallel to a top surface of the semiconductor layer on the sidewall of the protrusion of the vertical insulating pattern,
 - wherein the bottom portion of the contact portion has a substantially uniform thickness which is the same as the second thickness, and
 - wherein the second thickness is greater than the first thickness.
2. The 3D semiconductor memory device of claim 1, wherein the sidewall portion of the vertical insulating pattern has a third thickness that is greater than the first thickness.
3. The 3D semiconductor memory device of claim 1 or claim 2, wherein the vertical channel portion of the vertical semiconductor pattern is disposed on a top surface of

the protrusion of the vertical insulating pattern, and

wherein the contact portion of the vertical semiconductor pattern is disposed on a sidewall of the protrusion of the vertical insulating pattern.

4. The 3D semiconductor memory device of any one of claims 1 to 3, further comprising:

a filling insulation pattern filling a gap region defined by the vertical channel portion and the contact portion of the vertical semiconductor pattern,

wherein the filling insulation pattern comprises a lower portion adjacent to the contact portion, and an upper portion adjacent to the vertical channel portion, wherein a width of the lower portion is less than a width of the upper portion.

5. The 3D semiconductor memory device of any one of claims 1 to 3, further comprising:

a filling insulation pattern filling a gap region defined by the vertical channel portion and the contact portion of the vertical semiconductor pattern,

wherein a bottom surface of the filling insulation pattern is disposed at a lower level than a bottom surface of the vertical insulating pattern relative to the semiconductor layer.

6. The 3D semiconductor memory device of any one of claims 1 to 5, wherein a bottom surface of the vertical semiconductor pattern is disposed at a lower level than the top surface of the semiconductor layer.

7. The 3D semiconductor memory device of any one of claims 1 to 6, wherein the semiconductor layer comprises a recess region that is disposed under the vertical semiconductor pattern and has a sidewall that is inclined with respect to the top surface of the semiconductor layer, and

wherein the contact portion of the vertical semiconductor pattern is in contact with the sidewall that is inclined.

8. The 3D semiconductor memory device of any one of claims 1 to 6, wherein the semiconductor layer comprises a recess region having a rounded inner surface under the vertical semiconductor pattern, and

wherein the contact portion of the vertical semiconductor pattern is in contact with the rounded inner surface.

9. The 3D semiconductor memory device of any one of claims 1 to 8, further comprising:

a dummy vertical semiconductor pattern that is spaced apart from the vertical semiconductor pattern and penetrates the electrode structure so as to be connected to the semiconductor layer; and

a dummy vertical insulating pattern disposed between the dummy vertical semiconductor pattern and the electrode structure,

wherein a width of the dummy vertical semiconductor pattern is greater than a width of the vertical semiconductor pattern.

10. The 3D semiconductor memory device of claim 9, wherein a bottom surface of the dummy vertical semiconductor pattern is disposed at a lower level than a bottom surface of the vertical semiconductor pattern relative to the semiconductor layer.

11. The 3D semiconductor memory device of claim 9 or claim 10, wherein the dummy vertical semiconductor pattern comprises a first portion on an inner sidewall of the dummy vertical insulating pattern; and a second portion conformally extending along the top surface of the semiconductor layer, wherein the second portion is thicker than the first portion.

12. The 3D semiconductor memory device of any one of claims 1 to 11, wherein the semiconductor layer includes a first region and a second region adjacent to the first region, and

wherein the electrode structure extends from the first region onto the second region and has a stepped structure on the second region.

13. A three-dimensional (3D) semiconductor memory device comprising:
a substrate including a first region and a second region;
an electrode structure comprising electrodes vertically stacked on the substrate;
a first vertical structure penetrating the electrode structure on the first region and

having a first width;

a second vertical structure penetrating the electrode structure on the second region and having a second width greater than the first width; and

a lower semiconductor pattern disposed between the substrate and each of the first and second vertical structures and connected to the substrate, a top surface of the lower semiconductor pattern having a recess region,

wherein each of the first and second vertical structures comprises a vertical semiconductor pattern connected to the lower semiconductor pattern, and a vertical insulating pattern disposed between the electrode structure and the vertical semiconductor pattern on the lower semiconductor pattern,

wherein the vertical insulating pattern comprises a sidewall portion on a sidewall of the electrode structure, and a protrusion extending on a portion of a top surface of the lower semiconductor pattern,

wherein the vertical semiconductor pattern comprises a vertical channel portion having a first thickness on the sidewall portion of the vertical insulating pattern, and a contact portion conformally covering a recessed region of the lower semiconductor pattern and having a second thickness, in a first direction parallel to a top surface of the substrate, on a sidewall of the protrusion of the vertical insulating pattern, and wherein the second thickness is greater than the first thickness,

wherein a bottom portion of the contact portion conformally covers the recessed region of the top surface of the lower semiconductor pattern, and

wherein the bottom portion of the contact portion has a substantially uniform thickness which is the same as the second thickness.

14. The 3D semiconductor memory device of claim 13, wherein a top surface of the lower semiconductor pattern of the first vertical structure is disposed at a higher level than a top surface of the lower semiconductor pattern of the second vertical structure relative to the substrate.

15. The 3D semiconductor memory device of claim 13 or claim 14, wherein the sidewall portion of the vertical insulating pattern has a third thickness that is greater than the first thickness.

16. The 3D semiconductor memory device of any one of claims 13 to 15, wherein each of the first and second vertical structures further comprises: a filling insulation pattern filling a gap region defined by the vertical channel portion and the contact portion of the vertical semiconductor pattern,

wherein a bottom surface of the filling insulation pattern of the second vertical structure is disposed at a lower level than a bottom surface of the filling insulation pattern of the first vertical structure relative to the substrate.

17. The 3D semiconductor memory device of any one of claims 13 to 16, wherein a bottom surface of the vertical semiconductor pattern of the first vertical structure is disposed at a higher level than a top surface of a lowermost electrode of the electrodes relative to the substrate, and

wherein a bottom surface of the vertical semiconductor pattern of the second vertical structure is disposed at a lower level than the top surface of the lowermost electrode relative to the substrate.

18. The 3D semiconductor memory device of any one of claims 13 to 17, wherein, in each of the first and second vertical structures, the contact portion of the vertical semiconductor pattern conformally extends along the top surface of the lower semiconductor pattern and has the second thickness on the top surface of the lower semiconductor pattern.

19. The 3D semiconductor memory device of any one of claims 13 to 18, wherein the electrode structure has a stepped structure on the second region, and

wherein the second vertical structure penetrates the stepped structure of the electrode structure.

20. A three-dimensional semiconductor memory device comprising:
an electrode structure comprising electrodes stacked on a top surface of a substrate having a first region comprising memory cells and a second region comprising interconnection lines; and

first and second vertical structures of different widths extending into the electrode structure on the first and second regions, respectively, each of the first and second vertical structures comprising:

a vertical semiconductor pattern extending into the electrode structure and disposed in a recess region of the top surface of the substrate;

a vertical insulating pattern comprising a sidewall disposed between the electrode structure and the vertical semiconductor pattern, and a protrusion laterally extending on the top surface of the substrate,

wherein the vertical semiconductor pattern conformally covers an inner surface of the vertical insulating pattern and the recessed region of the top surface of the substrate,

wherein a first thickness of the vertical semiconductor pattern on the protrusion of the vertical insulating pattern is greater than a second thickness of the vertical semiconductor pattern on the sidewall of the vertical insulating pattern,

wherein the vertical semiconductor pattern on the recessed region of the top surface of the substrate has a third thickness in a second direction perpendicular to the top surface of the substrate, and

wherein the third thickness is substantially the same as the second thickness.