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(54) AUTOMATIC GAIN CONTROL SYSTEM

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an automatic gain control (AGC) for television receivers and, in particular, to a television AGC circuit having a plurality of operating modes.

In a television receiver, it is desirable that automatic gain control circuits (as well as synchronizing signals separator circuits) be capable of operation with received signals which include substantial spurious noise components. It is also desirable that an AGC circuit be arranged so that, for low level received signals, the receiver radio frequency (RF) amplifier be operated at maximum gain and gain control be applied only to the intermediate frequency (IF) amplifier. For higher level input signals, it is desirable to control the gain of the RF amplifier (i.e., provide an RF AGC delay). Furthermore, in color television receivers provided with internal means for producing a blank raster or a narrow horizontal line on the image display device for testing and alignment procedures, it is advantageous that during such testing procedures, video signals be prevented from reaching the display device.

In accordance with the present invention, there is provided an automatic gain control (AGC) system for use in a television receiver including signal processing means for deriving composite signals including image brightness representative signal components and regularly recurring synchronizing signal components extending in amplitude beyond said image brightness representative signal components, said system comprising automatic gain control means coupled to said processing means for maintaining said synchronizing signal components at a substantially fixed level, noise threshold means coupled to said processing means and responsive to noise components exceeding said fixed level by a predetermined amount, means for supplying from a first voltage source a first fixed reference voltage to said processing means and a second fixed reference voltage to each of said noise threshold and automatic gain control means for establishing said fixed level, a synchronizing signal separator circuit, and means for coupling said noise threshold means to each of said automatic gain control means and said synchronizing signal separator circuit.

Preferably included in an embodiment are output circuit means coupled to gating circuit means and to the source of composite television signals. This output circuit means comprises means for limiting the gain control effect to a first potential level of a first polarity for a first range of input signal levels to the radio frequency amplifier; to a second potential level of opposite polarity for a second range of input signal levels to the radio frequency amplifier; and to provide a gain control voltage which varies between the first and second potential levels for a range of input signal levels between the first and second ranges.

Also preferably included in this embodiment are servicing supply means coupled to the gating circuit means for energizing the gating circuit means so as to reduce the gain of the source of composite signals. Included, too, are switching means for disabling the servicing supply means in a normal operating condition and for energizing the servicing supply means in a service operating condition.

Referring to the accompanying drawing:

An antenna 10 receives transmitted radio frequency (RF) television signals and couples these signals to an RF tuner amplifier 11.

The RF tuner amplifier 11 amplifies and converts the received RF television signals into intermediate frequency (IF) signals. A dual gate field effect transistor (FET) 12 is employed in RF amplifier 11 to amplify the received RF signals. One gate is arranged for response to received RF signals while the

other gate is supplied via lead 16 with a control signal for varying the gain of the RF tuner amplifier 11. The IF signals produced in the RF tuner amplifier 11 are coupled to an IF amplifier 15 where they are amplified to a desired level for transmission to a sound system 18 of the television receiver and to a video or second detector 19. The sound system 18 translates sound signal components of the IF signal into amplified audio signals which are coupled to speaker 9.

In the video detector 19, a diode 20, responsive to the applied IF signals, produces output video signals across a resistor 21. Diode 20 is poled to produce video signals having synchronizing signal voltage components more positive that associated image representative voltage components (i.e., sync positive). Suitable filter networks 22 and 23 are provided to insure recovery of only the desired signal components. A voltage divider comprising resistors 30, 31 and 32 is coupled between a source of potential indicated as $+V_t$ and a source of reference potential (ground). The junction between resistors 31 and 30 is coupled to the junction between resistor 21 and filter 23 so as to maintain the output terminal of the video detector 19 (i.e., the junction between filter 22 and resistor 21) at a predetermined direct potential with reference to ground. The junction of resistors 30 and 31 also is coupled to the anode of diode 20 through a d.c. path supplied by filter 23.

A video amplifier transistor 35, coupled to the output terminal of video detector 19, is arranged in a common collector or emitter follower configuration to present a high input impedance to the video detector 19 and thereby to avoid loading its output while providing isolation. An emitter resistor 36 is coupled between ground and the emitter electrode of transistor 35 and serves as a low impedance output to drive a chrominance channel 37, a low impedance delay line 39 associated with a luminance channel and additional circuits, as will be explained below. Chrominance channel 37 functions to separate color information from the remainder of the detected video signals. Color signal processor 38, coupled to chrominance channel 37, processes applied signals to produce, for example, color difference signals. Color difference signals are coupled to appropriate control electrodes of an image reproducing device such as a three gun shadow-mask kinescope 41.

A luminance or "Y" channel signal representing monochrome image information is produced across resistor 36 and then is delayed a suitable amount by delay line 39. Delayed luminance signals are amplified by means of Y drive amplifier 42, the output of which is coupled to video drive controls 40. Drive controls 40 are arranged for application of luminance signals to appropriate electrodes (e.g. cathodes) of kinescope 41.

Horizontal and vertical deflection circuits 45 are provided for supplying suitable deflection currents to a yoke 43 associated with kinescope 41. The horizontal deflection portion of deflection circuits 45 also is arranged to generate suitable high magnitude operating potentials for appropriate electrodes of the kinescope 41. A synchronizing signal separator 46 is provided to synchronize the deflection circuits 45 with the received signals.

Video signals developed at the emitter electrode of video amplifier transistor 35 are also coupled via resistor 50 to the input of synchonizing signal separator 46. A noise inverting circuit also is coupled to sync separator 46 and comprises a transistor 51 having an emitter electrode coupled to a reference potential such as ground and a collector electrode coupled to the input of sync separator 46. The emitter of video amplifier 35 also is coupled to the anode of threshold diode 54. The cathode of threshold diode 54 is returned through resistor 52 to the junction of resistor 31 and 32 (which form part of the reference voltage divider described in connection with video detector 19). A capacitor 55 is coupled between the cathode of diode 54 and the base (input) of transistor 51. A resistor 56 provides a return path to ground for the base electrode of transistor 51. The collector of transistor 51 is coupled to the base of an AGC gate transistor 60 by means of a resistor 61.

Transistor 60 serves as a noise immune automatic gain control (AGC) gate and is coupled to the previously described voltage divider 30, 31, 32 by returning its emitter to the junction of resistors 31 and 32. A capacitor 65 also is coupled to the junction of resistors 31 and 32 and bypasses that junction to ground for alternating current signals. The base of transistor 60 also is coupled to the cathode of a diode 47, the anode of which is returned to the potential supply $+V_o$ through a resistor 48. The junction of resistor 48 and the anode of diode 47 is returned to a contact of a service switch 49, the function of which will be described subsequently.

AGC gate transistor 60 is keyed or activated at the horizontal deflection rate by a pulse waveshape obtained from the deflection circuits 45 via a capacitor 70. Capacitor 70 is coupled to the collector of transistor 60 via a diode 71. A series RC damping network comprising a resistor 73 and a capacitor 74 is coupled to the junction of capacitor 70 and the anode of diode 71. The junction of capacitor 70 and the anode of diode 71 is coupled through series connected resistors 92 and 93 to a source of positive potential $+V_B$. The junction between resistors 92 and

is coupled to one terminal of a filter capacitor 95, the other terminal of which is returned to ground. The junction of resistors 92 and 93 also is coupled to the anode of a diode 96 which exhibits Zener characteristics and is arranged to limit in each sense (polarity) the range of AGC signals applied via lead 16 to the radio frequency amplifier 11. The cathode of the Zener diode 96 is coupled to a current limiting resistor 97 which is returned to ground and which also forms part of a voltage divider further comprising series resistors 98 and 99 connected to the positive potential supply $+V_o$. The junction of resistors 98 and 99 is coupled to a further Zenor diode 100 which is returned to ground and which provides the reference voltage $+V_t$ supplied to the previously mentioned divider comprising resistors 30, 31 and 32.

The junction of capacitor 70 and diode 71 is coupled via a resistor 76 to the base electrode of a transistor 72, which serves as an amplifier for obtaining a suitable IF automatic gain control range. Operating potential is supplied to transistor 72 via series resistors 80 and 81 connected between the potential supply $+V_o$ and the collector electrode of transistor 72. The collector electrode of transistor 72 is coupled to its base electrode through the parallel combination of a resistor 83 and a capacitor 85. A current bias adjustment for transistor 72 is obtained by means of a resistive divider comprising a resistor 86 and a variable resistor 87 (designated as "Adjust RF AGC Delay") connected between potential supply $+V_o$ and ground. The junction of the resistors 86 and 87 is coupled to the base electrode of transistor 72 via a current limiting resistor 90, all of which serve to control the d.c. biasing of transistor 72.

Circuit operation will be explained utilizing, by way of example, some typical voltage levels which may be found in a typical televsion receiver. Video detector 19 provides at its output a video signal having synchronizing signal components at a more positive voltage level than accompanying image representative signal components. Typically video detector 19 provides such a video signal with a peak to peak amplitude of 3 volts, a level normally maintained by the action of the AGC circuit which will be described in detail subsequently. The 3 volt peak to peak signal at the output of video detector 19 corresponds to 85 per cent modulation of the carrier supplied to the input of detector 19.

This normal video signal level is superimposed on a d.c. voltage level obtained by coupling the junction of resistor 21 and filter 23 to the junction of resistors 30 and 31. The junction between resistors 30 and 31 is maintained at, for example, 2.3 volts by means of Zener diode 100 coupled across the potential supply $+V_o$. For these conditions at the detector 19, the white level of the 3 volt peak to peak, 85 per cent modulated video signal is approximately +2.8 volts. The maximum excursion or the top of the sync tip (the most positive portion of the synchronizing signal) is at approximately +5.8 volts. Transistor 35 when conducting maintains approximately 0.6 volts across its base to emitter junction and therefore a peak voltage of approximately 5.2 volts is produced at the emitter electrode of transistor 35 (and therefore at the anode of diode 54) during the sync interval.

As previously described, the cathode of diode 54 also is referenced to a joint on the voltage divider 30, 31, 32, namely the junction between resistors 31 and 32. The voltage at this point, for example, is maintained at +4.6 volts. It is noted that the emitter electrode of the AGC gate transistor 60 also is returned to this point on the voltage divider and hence also is biased at +4.6 volts. The base electrode of transistor 60, assuming no voltage drop across resistors 50 and 61, is at the same potential as the emitter of transistor 35, which is approximately +5.2 volts during sync interval. In utilizing the above d.c. level referencing, conduction thresholds are established which enable the AGC and sync separator circuits to operate in the presence of noise without the need for independent AGC and noise threshold adjustments.

With the above values, assuming diode 54 is a silicon device, in order for it to conduct, the voltage between its anode and cathode must be approximately 0.6 volts. Substantially the same voltage drop is required across the base to emitter junction of transistor 60 in order for it to conduct. Diode 54, since it is biased in the same manner as the base to emitter junction of transistor 60, just conducts on the tip portion of the synchronizing signals which exceeds 5.2 volts amplitude. Noise pulses above this amplitude and therefore above such "sync tips" are coupled by capacitor 55 to the base electrode of the noise inverter transistor 51. However, transistor 51 also requires a base to emitter voltage of +0.6 volts in order to conduct. Therefore, noise pulses exceeding the sync tips by at least the base to emitter conduction voltage (0.6 volts) of transistor 51 produce inverted noise pulses at the collector of transistor 51 (i.e., at the junction of resistors 50 and 61). Thus, for a video signal having sync tips at 5.8 volts at the output of detector 19, the noise threshold for the inverter transistor 51 is approximately +6.4 volts. Noise pulses above this level cause transistor 51 to conduct and to produce negative pulses at the junction of resistors 50 and 61 which cancel the positive noise pulses coupled from the emitter of

transistor 35. Therefore the AGC transistor 60 and the sync separator 46 are protected against excessive noise interference by means of transistor 51 and its associated components. Under the above signal conditions, AGC transistor 60 will conduct just at the sync tips of 5.2 volts.

The noise threshold for the noise inverter may be reduced further and brought closer to the sync tip level by using a germanium device for diode 54, which has a lower conduction drop from anode to cathode than the silicon device described above.

Since noise pulses are a.c. coupled to transistor 51, cancellation of sync from video under transient AGC conditions is prevented. It is possible under severe noise conditions to alter the noise threshold of transistor 51 by maintaining charge across capacitor 55. This effect can be reduced substantially by adding a series resistance (not shown) in the emitter circuit of transistor 51 or by placing a suitable resistor (not shown) in series with diode 54.

In the above description, it was assumed that the AGC circuit maintains the amplitude of the composite video signals at the output of video detector 19 constant at 3 volts peak to peak for a wide range of amplitudes of received RF signals. The AGC circuit maintains the desired substantially constant amplitude at the output of detector 19 by providing two AGC voltages having different ranges and different simultaneous values, respectively, for the RF tuner amplifier 11 and the IF amplifier 15. For low level signals supplied to RF amplifier 11, it is desirable to operate amplifier 11 at maximum gain while varying the gain of IF amplifier 15. When the RF input signal exceeds a predetermined threshold level (determined by receiver noise performance), the AGC circuit is arranged to vary the gain of RF amplifier 11 with little variation in the gain of IF amplifier 15. Gain control of RF amplifier 11 in this case avoids overdriving the mixer which would cause cross-modulation and, in general, distortion. For particularly high level input signals, RF amplifier 11 is biased to cutoff condition and the AGC circuit again varies only the gain of the IF amplifier 15.

The manner in which the AGC circuit operates will now be described for the condition where the input signal level to the RF amplifier 11 is low (e.g., of the order of 100 microvolts). It will also be assumed that the combined gain of RF amplifier 11 and IF amplifier 15 initially is too low to produce the nominal 3 volt peak to peak video signal at the output of detector 19.

As stated earlier, the emitter electrode of AGC gate transistor 60 is maintained at +4.6 volts. Since the output of detector 19 is less than the nominal 3 volts peak to peak, the base electrode of AGC gate transistor 60 is supplied with a video signal having sync at a lower level than the +5.2 volts required to initiate conduction. Transistor 60 therefore is maintained in cutoff condition even during the sync interval when positive pulses derived from deflection circuit 45 are supplied via capacitor 70.

With respect to the RF amplifier 11, it is desired to maintain maximum gain under these conditions. At this time, diode 96 is forward biased by means of the positive supply $+V_B$ and resistor 93. The RF AGC voltage across capacitor 95 is determined by the substantially fixed reference voltage provided at the junction of resistors 97 and 99. The voltage at this junction is a predetermined fraction of the substantially fixed voltage across Zener diode 100 and is selected, for example, equal to +6.0 volts. Since diode 96 is forward biased (e.g., +0.7 volts anode to cathode) the voltage across capacitor 95 is maintained at +6.7 volts for this condition. Field effect transistor 12 in RF amplifier 11 is arranged to provide maximum gain for this RF AGC output voltage.

Variable gain control is provided under these conditions by means of a varying IF AGC voltage supplied to IF amplifier 15 by means of transistor 72 in the following manner. The positive pulses provided by deflection circuit 45, as noted above, are ineffective to initiate conduction in AGC gate 60 and also have no effect on transistor 72 (i.e., capacitor 85 acts to filter the keying pulses).

The degree of conduction in the output circuit (resistors 80, 81) of transistor 72 is dependent upon the base current supplied to transistor 72. The base current, in turn, is dependent upon the base bias derived from the combination of resistors 86 and 87 coupled to the $+V_c$ potential, resistors 92 and 93 coupled to the $+V_B$ supply and the charge condition of capacitor 70. For the stated condition of low RF signal input level (e.g., 100 microvolts) and insufficient system gain to produce the nominal signal level at the output of detector 19, transistor 72 provides a relatively high output current which, in turn, produces a relatively low IF AGC voltage at the junction of resistors 80 and 81.

If amplifier 15 is arranged so that a relatively low AGC voltage corresponds to relatively high gain of IF amplifier 15 (i.e., transistor in IF amplifier 15 operated in forward AGC mode). The video level at the output of detector 19 therefore is increased until the nominal 3 volt peak-to-peak level is reached.

If the level of the video available at the output of detector 19 is greater than 3 volts peak-to-peak, a video signal will be produced at the base electrode of transistor 60 with sync tips at a higher positive potential than

48

is normal. Therefore, when the positive horizontal gating pulse occurs, transistor 60 is driven into conduction and offers a low impedance charge path for capacitor 70 through diode 71. The capacitor 70 charges so that the terminal coupled to resistor 92 assumes a negative voltage with respect to the terminal coupled to the deflection circuit 45. As a result, base drive current for transistor 72 is reduced, conduction in transistor 72 decreases, the IF AGC output voltage increases and the gain of IF amplifier 15 decreases so as to restore the nominal 3 volt peak-to-peak level at the output of detector 19.

The operating conditions described above apply for all RF input signal levels up to a level determined by the setting of RF AGC delay potentiometer 87. The setting of potentiometer 87 determines the gain characteristics of IF AGC transistor 72 and therefore determines the input signal level at which the RF AGC circuit becomes effective to vary receiver gain. For the maximum resistance setting of potentiometer 87, transistor 72 is biased for maximum conduction (minimum delay) while for minimum resistance setting, transistor 72 is biased for minimum conduction (maximum delay). In practice, potentiometer 87 is adjusted so that for a nominal RF input signal level (e.g., 500 microvolts), the gain of R.F. amplifier 11 is sufficient to provide a noise free image on the kinescope 41. It can be expected, unless the gain of RF amplifier 11 is at its maximum value for the above selected input signal level, that noise free images may also be obtained with lower input signal levels.

When the RF input signal level exceeds the predetermined threshold level established by operation of RF AGC delay potentiometer 87, the RF AGC output voltage is caused to vary in the following manner. For this condition, the voltage produced at the junction of capacitor 70 and resistor 92 is sufficiently low (or actually may be negative) that diode 96 no longer is maintained in its forward conduction condition. The voltage across capacitor 95 therefore no longer is maintained at the reference +6.7 volts described above, rather it decreases (eventually becoming negative) as the RF input signal level increases.

Diode 96 acts as reverse biased diode (i.e., high impedance) under these conditions. Variations in RF input signal level produce momentary variations in the output of detector 19. These variations in detector output cause AGC gate 60 to conduct more or less as its input level increases or decreases, thereby charging capacitor 70 more or less, respectively, during sync time. The charge state of capacitor 70 is reflected in the voltage produced across RF AGC output capacitor 95 under these conditions (i.e. diode 96 reverse biased). The voltage across capacitor 95 varies between a positive voltage limit (e.g., +6.7 volts corresponding to maximum RF gain) and a negative limit (e.g., −4.7 volts corresponding to minimum RF gain) over the range of input signal levels for which the gain of RF amplifier 11 is varied. For most of this range of input signal levels, the gain of IF amplifier 15 is maintained substantially constant or is varied only slightly.

At the point where the RF input signal level is sufficient to produce an RF AGC output voltage of −4.7 volts across capacitor 95, diode 96 is caused to operate in its Zener region and limits the negative voltage supplied to RF tuner 11. As noted earlier, the voltage at the cathode of Zener diode 96 is maintained at a level of +6.0 volts. Therefore, in order to limit the negative excursion across capacitor 95 to −4.7 volts, diode 96 is selected to provide Zener limiting when its anode to cathode voltage is −10.7 volts. FET transistor 12 is protected against reverse voltage breakdown by means of the Zener action of diode 96. Gain control is transferred at this signal level to IF AGC transistor 72 which operates as in the first case.

In the illustrated embodiment, in order to obtain a sharp Zener characteristic or a sharp increase in reverse current at the specified reverse voltage of 10.7 volts, the base to emitter junction of a transistor is utilized for Zener diode 96. It has been found that base to emitter junctions in certain types of transistors exhibit sharper Zener characteristics than do diodes fabricates specifically for Zener operation. The sharpness of the Zener response is related to the sharpness of the RF AGC response and is desirable to improve circuit performance. Furthermore, such a transistor with its collector electrode open-circuited may be more economical than the Zener diode illustrated.

Various control voltage levels are obtainable under different operating conditions within the extreme ranges described above and hence an AGC control with suitable range is available for both the RF and IF stages. For the conditions described above, the values of the circuit components are selected so that the emitter of transistor 60 and the video detector are biased by the voltage divider comprising resistors 30, 31 and 32 to enable the AGC control ranges as described above to maintain the output at the video detector at 3 volts peak to peak with 85 per cent carrier modulation.

A further application of the keyed AGC transistor 60 is available during servicing or testing of a color receiver using this embodiment of the invention. During such modes it is desirable to provide a blank raster on the screen of kinescope 41 so that color temperature may be adjusted. This mode then requires removing video information from

the raster to permit such adjustment. Furthermore, in receivers employing a service switch position wherein vertical deflection is disabled to permit adjustment of the kinescope screen voltages for setting optimum cutoff bias, video information should also be eliminated. Video information may be prevented from reaching the kinescope by reducing the RF and/or IF gain to reduce the video signal to zero at the output of the second detector. The gated AGC transistor 60 is controlled to perform this gain reduction function. A diode 47, having its anode coupled to a source of positive potential $+V_o$ through a resistor 48 and its cathode coupled to the base of AGC transistor 60, is coupled to ground during normal receiver operation by means of a first pair of contacts on a "SERVICE" switch 49. Diode 47 is biased with a reverse voltage at this time allowing transistor 60 to operate normally. When the service switch 49 is placed in a service mode, corresponding to the collapsed raster or blank raster mode, ground is removed from the anode of diode 47 and diode 47 becomes forward biased. Current supplied through resistor 48 and diode 47 causes transistor 60 to conduct beyond saturation level. Therefore, as described above, the gain of both the RF tuner 11 and the IF amplifier 15 are decreased so that no video output is produced from detector 19. The base current provided to transistor 60 is determined by the supply voltage $+V_o$ and the magnitude of resistor 48 and also serves to raise the voltage at the detector 19. This last-mentioned effect occurs as current flows through the base to emitter junction of transistor 60 and to ground through resistors 31 and 30 in the voltage divider. This current then raises the d.c. potential at the video detector from 2.3 volts, described above, to approximately 3.7 volts, which is a level between black and white. In this manner, the brightness of the blank raster on the face of the kinescope 41 is comparable to a brightness obtainable during normal operation. If transistor 60 were merely saturated as in the case of normal operation for low gain control, the voltage at the divider would be substantially unaffected and hence would produce a whiter than white raster in the absence of video signals at the output of the second detector 19.

In a system of practical construction operating in accordance with the principles described, component values were as follows:

Resistor 30	390 ohms
Resistor 31	390 ohms
Resistor 32	1,800 ohms
Resistor 36	1,000 ohms
Resistor 48	3,900 ohms
Resistor 50	470 ohms
Resistor 52	10,000 ohms
Resistor 61	1,000 ohms
Resistor 73	68,000 ohms
Resistor 76	1,000,000 ohms
Resistor 80	3,300 ohms
Resistor 81	1,500 ohms
Resistor 83	150,000 ohms
Resistor 86	270,000 ohms
Resistor 87	20,000 ohms (variable)
Resistor 90	22,000 ohms
Resistor 92	1,000,000 ohms
Resistor 93	3,300,000 ohms
Resistor 97	2,200 ohms
Resistor 98	220 ohms
Resistor 99	3,300 ohms
Capacitor 55	.01 microfarads
Capacitor 65	20 microfarads
Capacitor 70	820 picofarads
Capacitor 74	.027 microfarads
Capacitor 85	.068 microfarads
Capacitor 95	.18 microfarads
Transistor 35	SE1002
Transistor 51	2N3646
Transistor 60	2N3440
Transistor 72	2N3565
Diode 54	Silicon FD 100
Diode 71	FD 222
Diode 96	Base to emitter junction of SE4002 or 10.8 v. Zener
Diode 100	15 volt Zener
$+V_o$	+30 volts
$+V_t$	+15 volts
$+V_b$	+155 volts

WHAT WE CLAIM IS:—

1. An automatic gain control (AGC) system for use in a television receiver including signal processing means for deriving composite signals including image brightness representative signal components and regularly recurring synchronizing signal components extending in amplitude beyond said image brightness representative signal components, said system comprising automatic gain control means coupled to said processing means for maintaining said synchronizing signal components at a substantially fixed level, noise threshold means coupled to said processing means and responsive to noise components exceeding said fixed level by a predetermined amount, means for supplying from a first voltage source a first fixed reference voltage to said processing means and a second fixed reference voltage to each of said noise threshold and automatic gain control means for establishing said fixed level, a synchronizing signal separator circuit, and means for coupling said noise threshold means to each of said automatic gain control means and said synchronizing signal separator circuit.

2. An automatic gain control system according to claim 1 wherein said first reference voltage is supplied to detecting means included in said processing means for detect-

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the raster to permit such adjustment. Furthermore, in receivers employing a service switch position wherein vertical deflection is disabled to permit adjustment of the kinescope screen voltages for setting optimum cutoff bias, video information should also be eliminated. Video information may be prevented from reaching the kinescope by reducing the RF and/or IF gain to reduce the video signal to zero at the output of the second detector. The gated AGC transistor 60 is controlled to perform this gain reduction function. A diode 47, having its anode coupled to a source of positive potential $+V_c$ through a resistor 48 and its cathode coupled to the base of AGC transistor 60, is coupled to ground during normal receiver operation by means of a first pair of contacts on a "SERVICE" switch 49. Diode 47 is biased with a reverse voltage at this time allowing transistor 60 to operate normally. When the service switch 49 is placed in a service mode, corresponding to the collapsed raster or blank raster mode, ground is removed from the anode of diode 47 and diode 47 becomes forward biased. Current supplied through resistor 48 and diode 47 causes transistor 60 to conduct beyond saturation level. Therefore, as described above, the gain of both the RF tuner 11 and the IF amplifier 15 are decreased so that no video output is produced from detector 19. The base current provided to transistor 60 is determined by the supply voltage $+V_c$ and the magnitude of resistor 48 and also serves to raise the voltage at the detector 19. This last-mentioned effect occurs as current flows through the base to emitter junction of transistor 60 and to ground through resistors 31 and 30 in the voltage divider. This current then raises the d.c. potential at the video detector from 2.3 volts, described above, to approximately 3.7 volts, which is a level between black and white. In this manner, the brightness of the blank raster on the face of the kinescope 41 is comparable to a brightness obtainable during normal operation. If transistor 60 were merely saturated as in the case of normal operation for low gain control, the voltage at the divider would be substantially unaffected and hence would produce a whiter than white raster in the absence of video signals at the output of the second detector 19.

In a system of practical construction operating in accordance with the principles described, component values were as follows:

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Resistor 36	1,000 ohms
Resistor 48	3,900 ohms
Resistor 50	470 ohms
Resistor 52	10,000 ohms
Resistor 61	1,000 ohms
Resistor 73	68,000 ohms
Resistor 76	1,000,000 ohms
Resistor 80	3,300 ohms
Resistor 81	1,500 ohms
Resistor 83	150,000 ohms
Resistor 86	270,000 ohms
Resistor 87	20,000 ohms (variable)
Resistor 90	22,000 ohms
Resistor 92	1,000,000 ohms
Resistor 93	3,300,000 ohms
Resistor 97	2,200 ohms
Resistor 98	220 ohms
Resistor 99	3,300 ohms
Capacitor 55	.01 microfarads
Capacitor 65	20 microfarads
Capacitor 70	820 picofarads
Capacitor 74	.027 microfarads
Capacitor 85	.068 microfarads
Capacitor 95	.18 microfarads
Transistor 35	SE1002
Transistor 51	2N3646
Transistor 60	2N3440
Transistor 72	2N3565
Diode 54	Silicon FD 100
Diode 71	FD 222
Diode 96	Base to emitter junction of SE4002 or 10.8 v. Zener
Diode 100	15 volt Zener
$+V_c$	+30 volts
$+V_t$	+15 volts
$+V_b$	+155 volts

WHAT WE CLAIM IS:—

1. An automatic gain control (AGC) system for use in a television receiver including signal processing means for deriving composite signals including image brightness representative signal components and regularly recurring synchronizing signal components extending in amplitude beyond said image brightness representative signal components, said system comprising automatic gain control means coupled to said processing means for maintaining said synchronizing signal components at a substantially fixed level, noise threshold means coupled to said processing means and responsive to noise components exceeding said fixed level by a predetermined amount, means for supplying from a first voltage source a first fixed reference voltage to said processing means and a second fixed reference voltage to each of said noise threshold and automatic gain control means for establishing said fixed level, a synchronizing signal separator circuit, and means for coupling said noise threshold means to each of said automatic gain control means and said synchronizing signal separator circuit.

2. An automatic gain control system according to claim 1 wherein said first reference voltage is supplied to detecting means included in said processing means for detect-

g said brightness representative and synchronizing signal components.

3. An automatic gain control system according to claim 2 wherein said detecting means comprises a diode poled for conduction upon application of positive polarity signals.

4. An automatic gain control system according to claim 3 having means for supplying said reference voltages from a substantially constant voltage of positive polarity.

5. An automatic gain control system according to any preceding claim including for deriving said reference voltages from a voltage source, a voltage divider having first and second junctions for supplying said first and second reference voltages with the first reference voltage less than the second.

6. An automatic gain control system according to any preceding claim wherein said noise threshold means is alternating current coupled to noise inverting means, having an output direct current coupled to each of said automatic gain control and synchronizing signal separator circuits.

7. An automatic gain control system according to any one of the preceding claims, wherein said automatic gain control means is coupled to a radio frequency amplifier of the receiver and has output circuit means coupled to gating circuit means and to said signal processing means, said output circuit means comprising means for limiting the gain control effect on said radio frequency amplifier to a first potential level of a first polarity for a first range of input signals to said signal processing means, and to a second potential level of opposite polarity for a second range of input signal levels, and for providing a gain control voltage which varies between said first and second potential levels for a range of input signal levels between said first and second ranges.

8. An automatic gain control system according to claim 7 wherein said output circuit means further comprises means for supplying varying gain control voltage to an intermediate frequency amplifier of said signal processing means such as to produce a varying gain therein for said first and second ranges and a substantially invariant gain for said range between said first and second ranges.

9. An automatic gain control system according to claim 7 or claim 8 including servicing supply means for energizing said gating circuit means so as to reduce the gain of said signal processing means, together with switching means for disabling said servicing supply means in a normal operating condition and for activating said servicing supply means in a service operating condition.

10. An automatic gain control system according to claim 9 wherein said servicing supply means includes a voltage divider coupled to said gating circuit means and to said signal processing means responsive to energization of said servicing supply means for producing a reference signal level for the output of said signal processing means.

11. An automatic gain control system according to any of claims 7 to 10 wherein said output circuit means comprises a diode, a first potential means coupled to said diode and to said gating means, and a second potential means coupled to said diode, said first and second potential means maintaining said diode in forward conduction and Zener conduction conditions, respectively, for said first and second ranges of input signal levels.

12. An automatic gain control system according to any of claims 7 to 11 including capacitive means for coupling said gating circuit means to a source of pulses and for coupling to said output circuit means, in response to said pulses, a voltage of opposite polarity with respect to said first potential means.

13. An automatic gain control system according to claims 11 and 12 wherein said first potential means comprises voltage divider means for coupling across a source of voltage and having at least first and second junctions coupled, respectively, to said diode and to said capacitive means.

14. An automatic gain control system according to any of claims 11 to 13 wherein said diode comprises anode and cathode electrodes, said first potential means being coupled to said anode, and said second potential means being coupled to said cathode and arranged to supply a voltage less than that of said first source.

15. An automatic gain control system according to any of claims 7 to 14 including means for adjustably selecting said first range of signal levels.

16. A television receiver automatic gain control system substantially as hereinbefore described with reference to the accompanying drawing.

17. A television receiver having an AGC system according to any preceding claim.

T. I. M. SMITH,
Chartered Patent Agent,
50, Curzon Street,
London, W.1.
Agent for the Applicant.

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