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DRIVE CIRCUIT FOR MULTIPLE SCAN RATE LINE DEFLECTION CIRCUIT

This invention relates to horizontal (line) deflection
circuits and in particular to horizontal deflection
5 circuits having multiple scan rates.

In recent years, the quality of the picture
displayed by commercial television receivers has been
greatly improved. Computer monitors or word processing
display terminals, however, may require even greater resolu-
10 tion and sharpness than is currently possible with ordinary
television receivers. Further improvements in picture quality
may be obtained through improvements in color picture tubes
and signal processing, and through modification of
current signal processing standards. Modification of
15 signal processing standards should, however, be
compatible with the circuitry in receivers already in
use and should not make them obsolete.

One technique which improves the observed picture
quality provides a change in the horizontal scanning system
20 from the current line interlaced to a non-interlaced, or
progressive scan system. In an NTSC system, this would involve
an increase in the horizontal scanning rate from 15.75 KHz
to 31.5 KHz, or 63 KHz, but would not require any change
in the transmitted signal. Therefore, there would be no
25 effect on reproduction of pictures by receivers already
in use. Benefits of the non-interlaced scanning system
for monitors and video display terminals would be the
almost complete elimination of such picture artifacts
as large area flicker, inter-line flicker, line breakup
30 and line crawl.

At high scanning or deflection rates, such as
31.5 KHz and 63 KHz, power dissipation in the horizontal
output transistor is considerably higher than at a normal
receiver scanning rate of 15.75 KHz. Proper adjustment
35 of the horizontal drive waveform is necessary in order
to minimize this power dissipation. The negative portion
of the drive waveform is extremely critical, as that
represents the interval when stored charge in the output

transistor is removed as the transistor is being turned off. In a conventional television receiver, the negative drive that sweeps out the stored charge is provided by a secondary winding of a horizontal driver transformer. Leakage
5 inductance of the transformer and external components are used to shape the drive waveform as desired.

At high scanning rates, the leakage inductance of the driver transformer may not be low enough to provide the required amount of negative drive to the horizontal output
10 transistor in order to remove the stored charge. Also, at high scanning rates, it is desirable to remove the stored charge at a faster rate in order to maintain a desirable ratio of trace interval to retrace interval. It is also
15 desirable to provide a means for switching between scanning rates to provide additional versatility in the use of video display equipment.

In accordance with one aspect of the present invention, there is provided a line deflection circuit operable at first and second selectable line scan rates
20 comprising:

means providing a drive signal having a first signal amplitude in response to the selection of said first selectable line scan rate and having a second signal
25 amplitude in response to the selection of said second selectable line scan rate; and

output means incorporating a deflection winding and a switching transistor having a base terminal coupled to said drive signal providing means, said switching transistor being responsive to said drive signal for causing switching
30 of said switching transistor between saturated and nonconductive states in order to provide line deflection current in said deflection winding defining trace and retrace intervals, said first and second signal amplitudes determining the length of the transition interval when said
35 switch transistor switches between said saturated and said nonconductive states.

In accordance with another aspect of the present

invention, there is provided a line deflection circuit operable at multiple line scan rates comprising:

means for providing line rate signals at a plurality of selectable frequencies;

5 a drive circuit having a first terminal coupled to said means for providing line rate signals, a second terminal providing line rate drive signals, and a third terminal;

a line output circuit incorporating a deflection winding and a switching transistor having a base terminal coupled to said drive circuit second terminal, said switching transistor being responsive to said drive signals for causing switching of said switching transistor between saturated and nonconductive states in order to provide line trace and retrace current in said deflection winding, said transition interval between said saturated and nonconductive states of said switching transistor being determined by the amplitude of said drive signals; and

means coupled to said third terminal of said drive circuit for providing to said drive circuit a voltage having a level dependent upon the frequency of said line rate signals, the magnitude of said voltage level determining the amplitude of said drive signals.

In the accompanying drawing:

25 FIGURE 1 is a schematic and block diagram of a horizontal deflection circuit incorporating a drive circuit in accordance with an aspect of the present invention;

FIGURE 2 illustrates waveforms associated with the drive circuit shown in FIGURE 1; and

30 FIGURE 3 is a schematic and block diagram of a portion of the circuit shown in FIGURE 1, illustrating additional features.

Referring to Figure 1, there is shown a horizontal drive circuit 10 and a horizontal output circuit 11.

35 Horizontal oscillator 43 generates a horizontal rate signal (44) whose frequency is determined by frequency selector 45, which is controlled by a signal at terminal 25.

1 The horizontal rate signal 44 is applied to drive circuit 10.
The signal from the horizontal oscillator is applied through
a coupling capacitor 12 to the bases of transistors 13 and 14,
connected in a push-pull arrangement. The emitters of
5 transistors 13 and 14 are connected together and provide
a drive signal to the base of horizontal output transistor
15 of horizontal output circuit 11 without the need for
a driver transformer. Horizontal output circuit 11 also
includes a damper diode 16, retrace capacitor 17, horizontal
10 deflection coils 20 and S-shaping capacitor 21. Power
is provided to output circuit 11 from a source of voltage B+
via a winding 22 of a high voltage transformer (not shown).
The drive signals from drive circuit 10 switch transistor 15
between conductive and nonconductive states at the desired
15 horizontal scan or deflection frequency. Retrace pulses,
appearing across retrace capacitor 17 and winding 22 when
transistor 15 is switched off, are used via the high
voltage transformer to generate the high voltage that is
applied to the anode of a picture tube (not shown).

20 As previously described, it is important to
remove as rapidly as possible the charge stored in the base
region of transistor 15 when transistor 15 is switched off
from its saturated conduction state, in order to as much as
possible reduce the power dissipation of transistor 15.

25 In accordance with an aspect of the present invention,
drive circuit 10 incorporates multiple level voltage
sources 23 and 24 which are coupled to the collectors of
transistors 13 and 14, respectively. Multiple level voltage
source 23 provides a positive voltage which determines the
30 forward drive level for transistor 15. The magnitude or
level of the voltage provided by voltage source 23 is
dependent on the horizontal scanning or deflection rate
that is selected. For example, to maintain a constant ratio
of trace-to-retrace interval, the inductance of the horizontal
35 deflection coils 20 is decreased as the horizontal scanning
frequency increases, by means of switch bank 46. This
causes the forward drive current requirement of transistor
15 to increase in order to maintain the transistor in
saturation during the increased deflection current, which in
turn requires a higher voltage _____

1 requirement from voltage source 23. This is illustratively
shown in FIGURES 2A, 2B and 2C, which shows the base or drive
current waveforms of horizontal output transistor 15 at
horizontal scanning rates of 15.75 KHz, 31.5 KHz and
5 63 KHz, respectively. The level of voltage source 23,
as shown in FIGURE 1, is also controlled by a signal at
terminal 25. This signal is representative of the
scanning rate selected.

Multiple level voltage source 24 provides a
10 negative voltage level to the collector of transistor 14,
which determines the negative drive level for transistor 15.
As the horizontal scanning frequency is increased, the
negative drive current requirement, and hence the magnitude
of the voltage level of the voltage source 24 is increased,
15 as shown illustratively by the base current waveforms of
FIGURES 2A, 2B and 2C. The voltage level provided by
voltage source 24 is also controlled by a signal
at terminal 25.

20 It is possible to maintain a constant retrace
interval by maintaining a constant impedance of the deflection
coils. Although the horizontal output circuit voltage supply
requirements may change with different scanning frequencies,
the forward drive level for the horizontal output
25 transistor would remain constant. A multiple level
supply, such as voltage source 23, would not be necessary
in this case. However, the negative drive requirement
would change as the scanning frequency changed.
Therefore, a multiple level supply, such as voltage
30 source 24, would be needed.

The operation of a multiple scan rate deflection
circuit is described in detail in U.S. Patent Application
Serial No. 497,950, filed May 25, 1983, in the names of
W.F. Wedam, et al., entitled "POWER SUPPLY AND DEFLECTION
35 CIRCUIT PROVIDING MULTIPLE SCAN RATES". This application
corresponds to British Application 8412557 (2140640A) and
describes an illustrative arrangement for producing a
signal representative of the horizontal scanning rate

1 selected, which could be applied, for example, to
terminals 25 of FIGURE 1. This application
also describes arrangements for changing
the S-shaping capacitance and the horizontal output circuit
5 supply voltage when the horizontal scanning frequency is
changed. Multiple level voltage sources 23 and 24 could
include, for example, some form of switching circuitry
which would control the magnitude of the voltage levels
produced by voltage sources 23 and 24.

10 FIGURE 3 shows a drive circuit similar to that
shown in FIGURE 1 which includes components that further
aid in shaping the drive waveform for the horizontal
output transistor.

Inductor 27 provides shaping of the collector
15 current for transistor 13. Diode 30 returns some power
to the voltage source during the negative drive interval.
Shaping of the base current waveform for the horizontal
output transistor is also provided by inductors 31 and 32.

The source of voltage for transistor 13, which
20 provides the forward drive to horizontal output transistor
15, is shown as separate voltage sources 33, 34 and 35,
which illustratively provide voltage levels for operation
at horizontal scanning rates of 15.75 KHz, 31.5KHz and
63 KHz, respectively. Additional voltage sources for
25 additional scanning frequencies are of course possible.
A switching circuit 36, schematically shown, selects the
appropriate voltage source based on the selected scanning
rate representative signal at terminal 25.

The source of voltage for transistor 14, which
30 provides negative or reverse drive for transistor 15, is
shown as individual voltage sources 37, 40 and 41 which
provide voltage levels for operation at horizontal
scanning rates of 15.75 KHz, 31.5KHz and 63 KHz,
respectively. A switching circuit 42, similar to switching
35 circuit 36, selects the proper voltage sources in response
to the signal at terminal 25.

**CLAIMS:**

1. A line deflection circuit operable at first and second selectable line scan rates comprising:

means providing a drive signal having a first
5 signal amplitude in response to the selection of said first selectable line scan rate and having a second signal amplitude in response to the selection of said second selectable line scan rate; and

output means incorporating a deflection winding
10 and a switching transistor having a base terminal coupled to said drive signal providing means, said switching transistor being responsive to said drive signal for causing switching of said switching transistor between saturated and nonconductive states in order to provide line deflection
15 current in said deflection winding defining trace and retrace intervals, said first and second signal amplitudes determining the length of the transition interval when said switch transistor switches between said saturated and said nonconductive states.

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2. A line deflection circuit operable at multiple line scan rates comprising:

means for providing line rate signals at a plurality of selectable frequencies;

25 a drive circuit having a first terminal coupled to said means for providing line rate signals, a second terminal providing line rate drive signals

and a third terminal;

30 a line output circuit incorporating a deflection winding and a switching transistor having a base terminal coupled to said drive circuit second terminal, said switching transistor being responsive to said drive signals for causing switching of said
35 switching transistor between saturated and nonconductive states in order to provide line



trace and retrace current in said deflection winding,
said transition interval between said saturated and
nonconductive states of said switching transistor being
determined by the amplitude of said drive signals; and

5 means coupled to said third terminal of said drive
circuit for providing to said drive circuit a voltage having
a level dependent upon the frequency of said line rate
signals, the magnitude of said voltage level determining the
amplitude of said drive signals.

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3. A circuit according to claim 2, wherein
said voltage level magnitude determines the reverse
base current amplitude of said switching transistor.

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4. A circuit according to claim 2 or claim
3, wherein said means for providing a voltage comprises
a DC voltage supply for generating a DC voltage having
different voltage levels in response to different
selected scan frequencies in order to provide different
20 peak reverse base current amplitudes for said switching
transistor.

5. A line deflection circuit substantially
as hereinbefore described with reference to Figure 1
25 optionally as modified by Figure 3.
