CLAIMS:

1. A multilayer structure comprising:

a single crystal semiconductor handle substrate comprising two major, generally parallel surfaces, one of which is a front surface of the single crystal semiconductor handle substrate and the other of which is a back surface of the single crystal semiconductor handle substrate, an imaginary central plane between the front surface and the back surface, a circumferential edge joining the front and back surfaces of the single crystal semiconductor handle substrate, and a bulk region between the front and back surfaces of the single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate has a minimum bulk region resistivity of at least about 500 ohm-cm;

a charge trapping layer comprising a polycrystalline silicon layer, the charge trapping layer being in interfacial contact with the front surface of the single crystal semiconductor handle substrate, wherein the charge trapping layer has a minimum resistivity of at least about 1000 ohm-cm;

an insulating layer comprising silicon nitride or silicon oxynitride in interfacial contact with the charge trapping layer comprising polycrystalline silicon layer;

a dielectric layer in interfacial contact with the insulating layer, the dielectric layer comprising silicon dioxide; and

a single crystal silicon device layer, wherein the single crystal silicon device layer is in interfacial contact with the dielectric layer.

2. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises single crystal silicon.

3. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises a single crystal silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method or the float zone method.

4. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 500 Ohm-cm and about 100,000 Ohm-cm.

5. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 1000 Ohm-cm and about 100,000 Ohm-cm.

6. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 1000 Ohm-cm and about 6,000 Ohm-cm.

7. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 3000 Ohm-cm and about 5,000 Ohm-cm.

8. The multilayer structure of claim 1 wherein the charge trapping layer has a minimum resistivity of at least about 3000 ohm-cm.

9. The multilayer structure of claim 1 wherein the charge trapping layer has a minimum resistivity of at least about 7000 ohm-cm.

10. The multilayer structure of claim 1 wherein the insulating layer comprises silicon nitride.

11. The multilayer structure of claim 1 wherein the insulating layer comprises silicon oxynitride layer.

12. The multilayer structure of claim 1 wherein the insulating layer has a thickness between about 2000 angstroms and about 10,000 angstroms.

13. The multilayer structure of claim 1 wherein the dielectric layer further comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, hafnium oxide, titanium oxide, zirconium oxide, lanthanum oxide, barium oxide, and a combination thereof.

14. The multilayer structure of claim 1 wherein the dielectric layer further comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, and a combination thereof.

15. The multilayer structure of claim 1 wherein the dielectric layer comprises an insulating layer having a thickness of at least about 10 nanometer thick, such as between about 10 nanometers and about 10,000 nanometers, between about 10 nanometers and about 5,000 nanometers, between 50 nanometers and about 400 nanometers, or between about 100 nanometers and about 400 nanometers, such as about 50 nanometers, 100 nanometers, or 200 nanometers.

16. A multilayer structure comprising:

a single crystal semiconductor handle substrate comprising two major, generally parallel surfaces, one of which is a front surface of the single crystal semiconductor handle substrate and the other of which is a back surface of the single crystal semiconductor handle substrate, an imaginary central plane between the front surface and the back surface, a circumferential edge joining the front and back surfaces of the single crystal semiconductor handle substrate, and a bulk region between the front and back surfaces of the single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate has a minimum bulk region resistivity of at least about 500 ohm-cm;

a semiconductor oxide in interfacial contact with the front surface of the single crystal semiconductor handle substrate;

a charge trapping layer comprising a polycrystalline silicon layer, the charge trapping layer being in interfacial contact with the semiconductor oxide, wherein the charge trapping layer has a minimum resistivity of at least about 1000 ohm-cm;

an insulating layer comprising silicon nitride or silicon oxynitride in interfacial contact with the charge trapping layer comprising the polycrystalline silicon layer;

a dielectric layer in interfacial contact with the insulating layer, the dielectric layer comprising two or more layers, wherein each of the two or more layers comprises a material selected from the group consisting of silicon dioxide, silicon oxynitride, and silicon nitride, and further wherein at least one layer comprises silicon dioxide; and

a single crystal silicon device layer, wherein the single crystal silicon device layer is in interfacial contact with the dielectric layer.