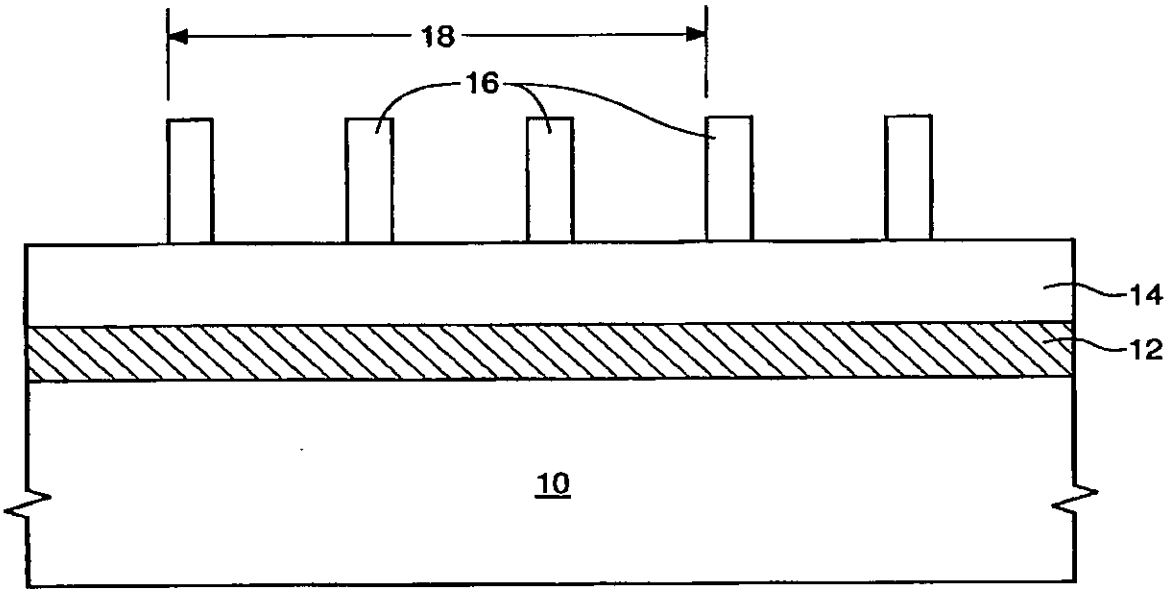


FIG. 1
(RELATED ART)

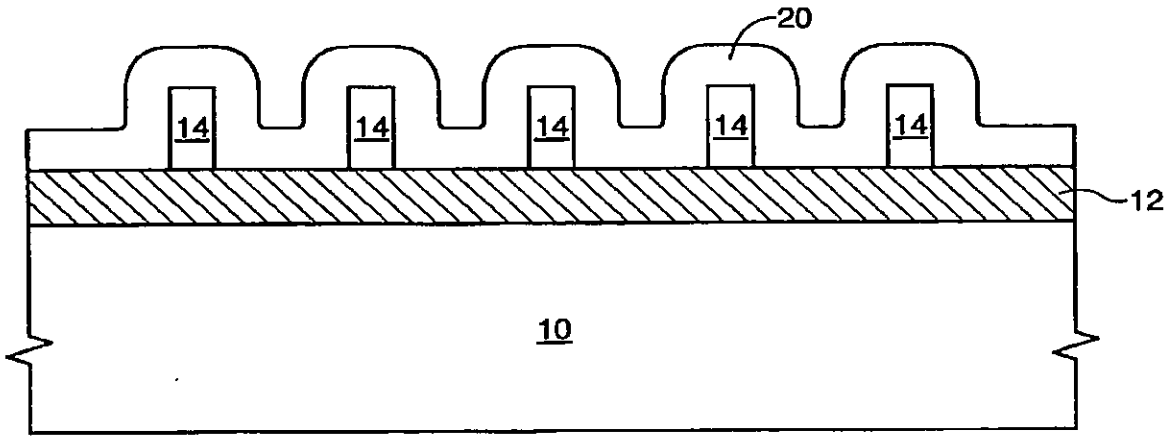


FIG. 2
(RELATED ART)

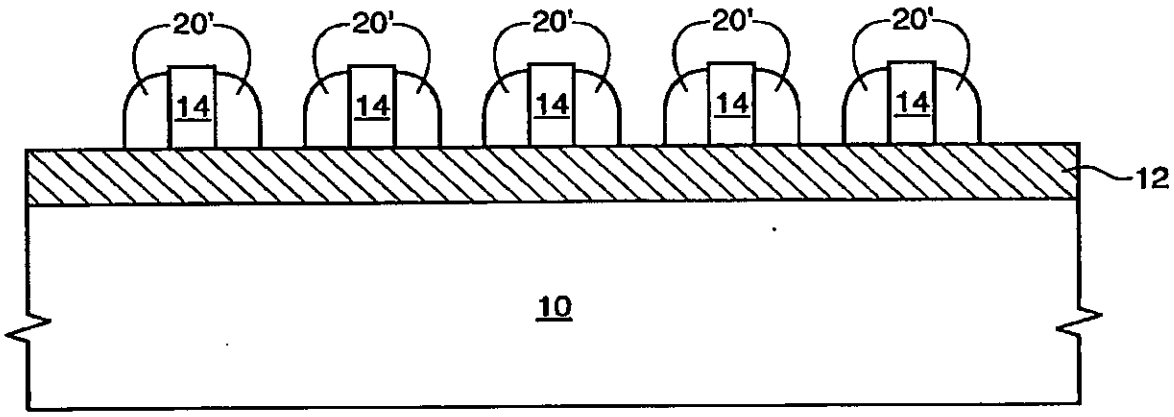


FIG. 3
(RELATED ART)

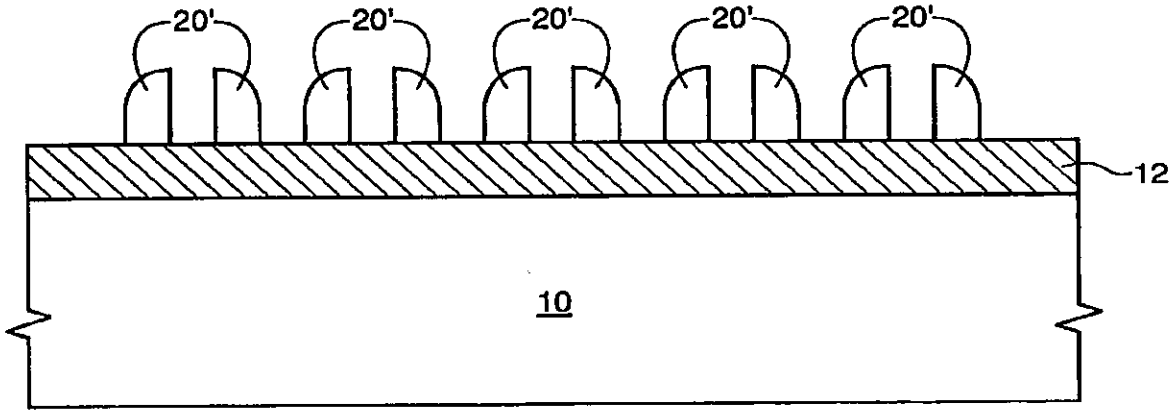


FIG. 4
(RELATED ART)

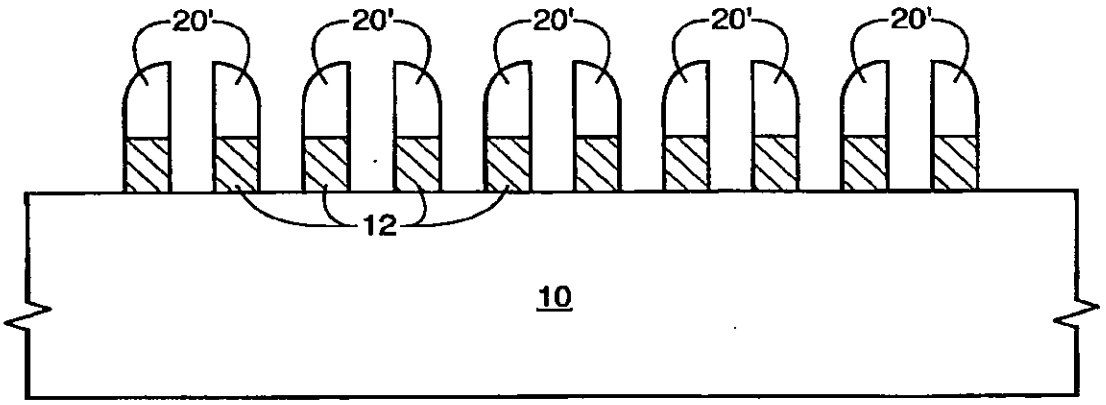


FIG. 5
(RELATED ART)

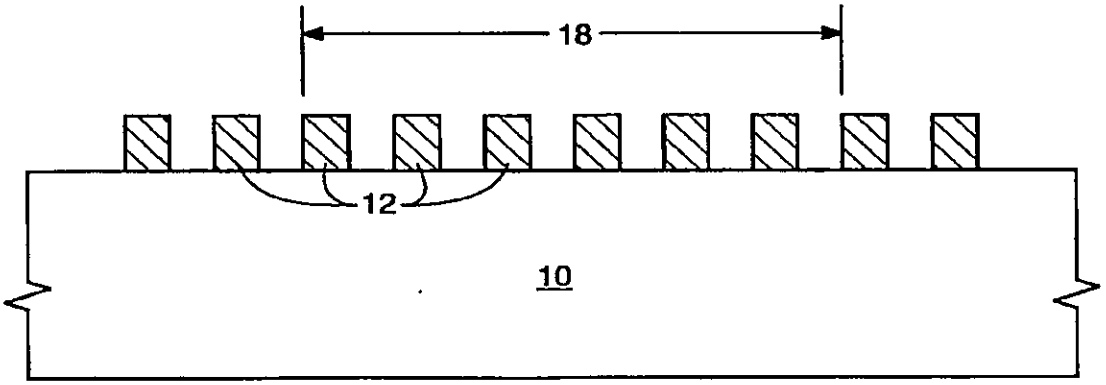


FIG. 6
(RELATED ART)

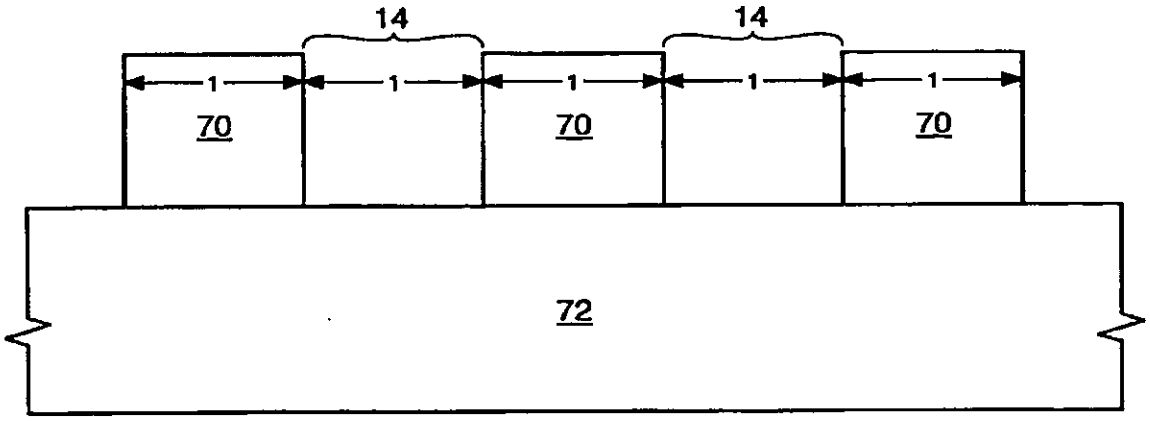


FIG. 7

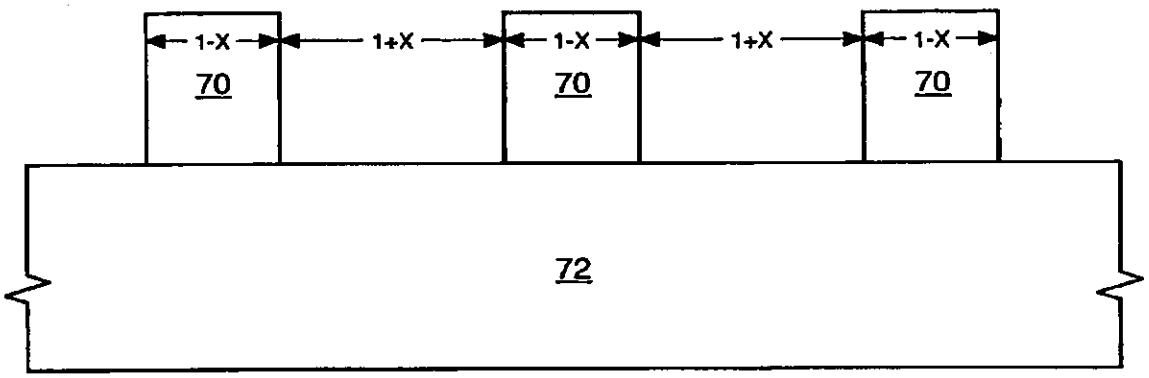


FIG. 8

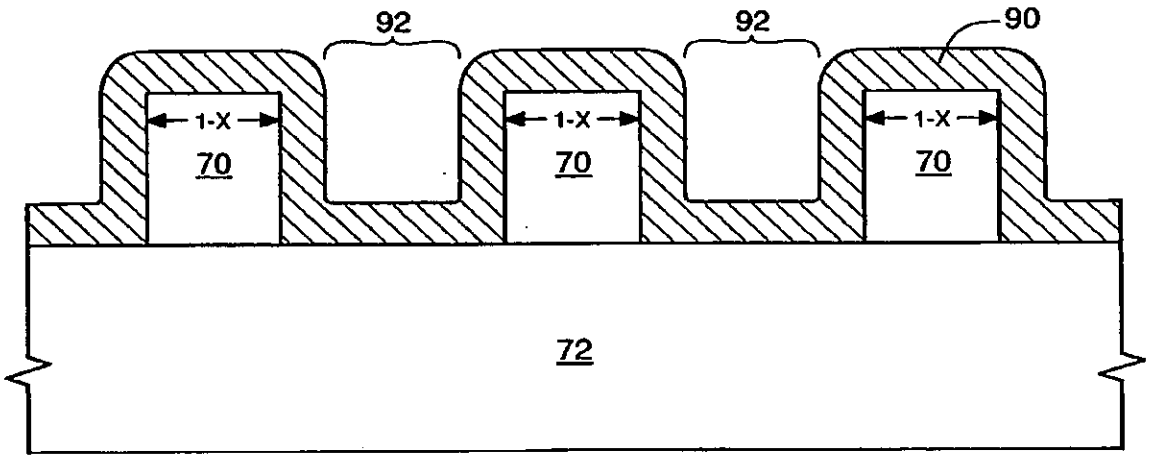


FIG. 9

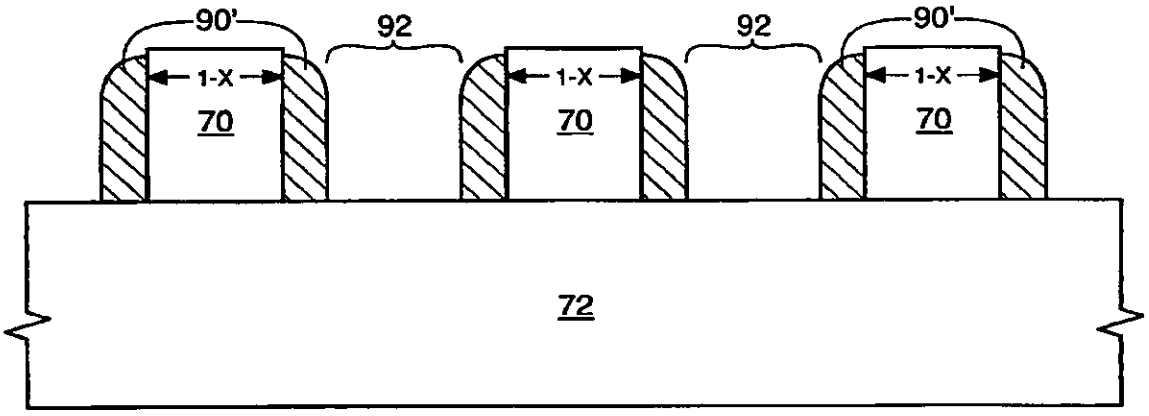


FIG. 10

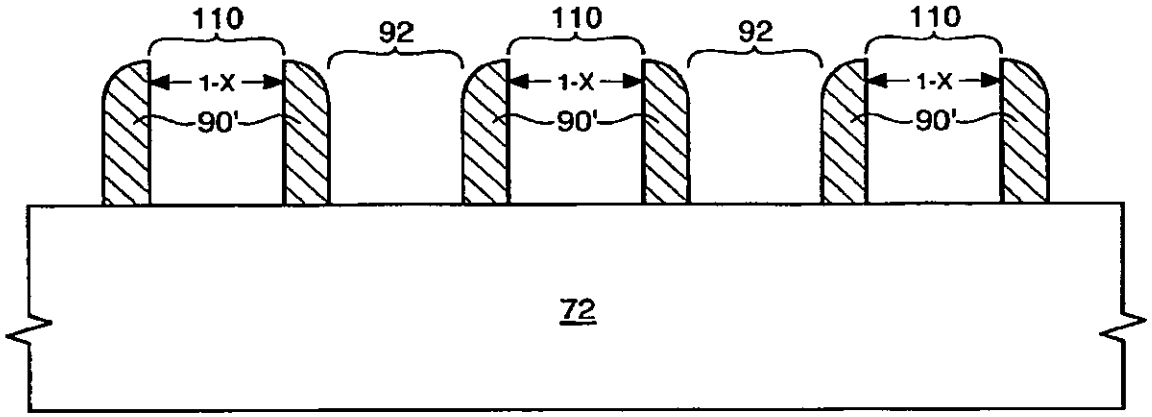


FIG. 11

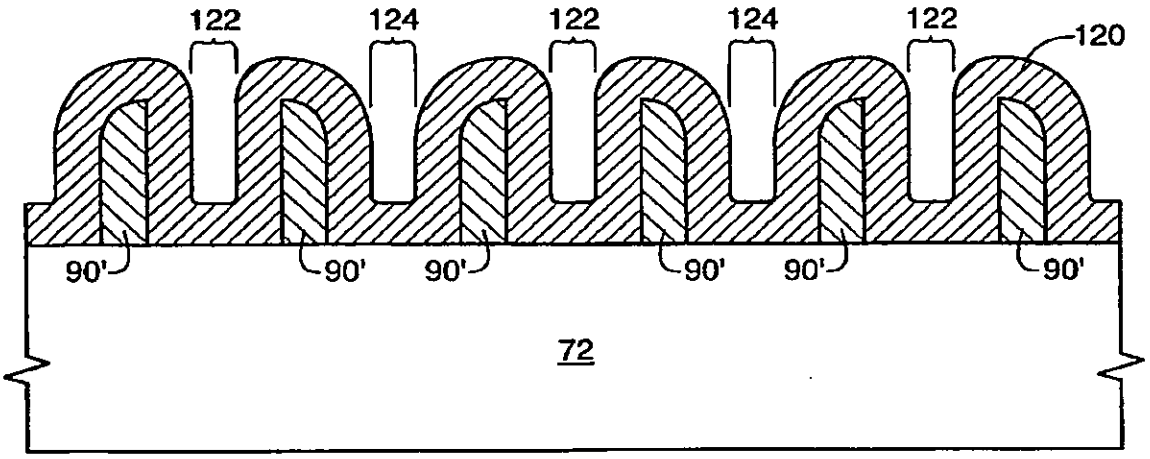


FIG. 12

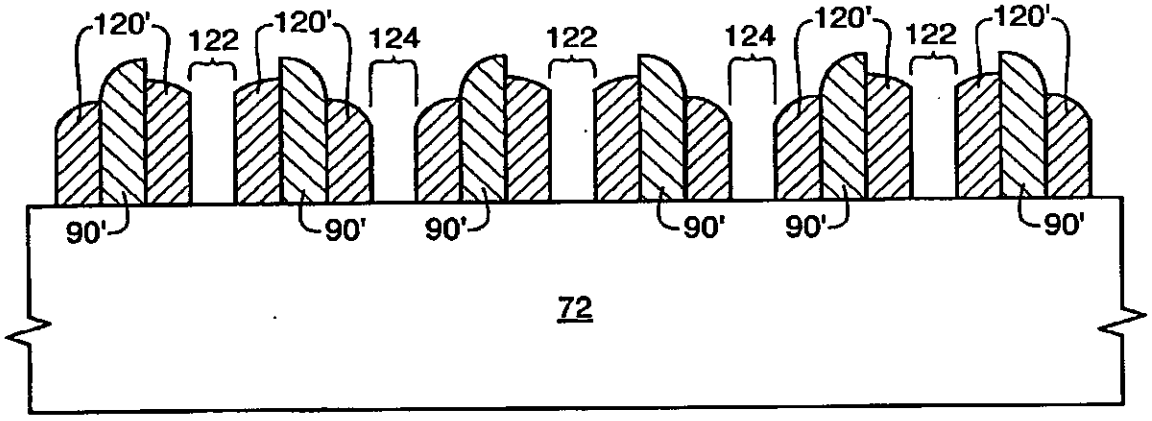


FIG. 13

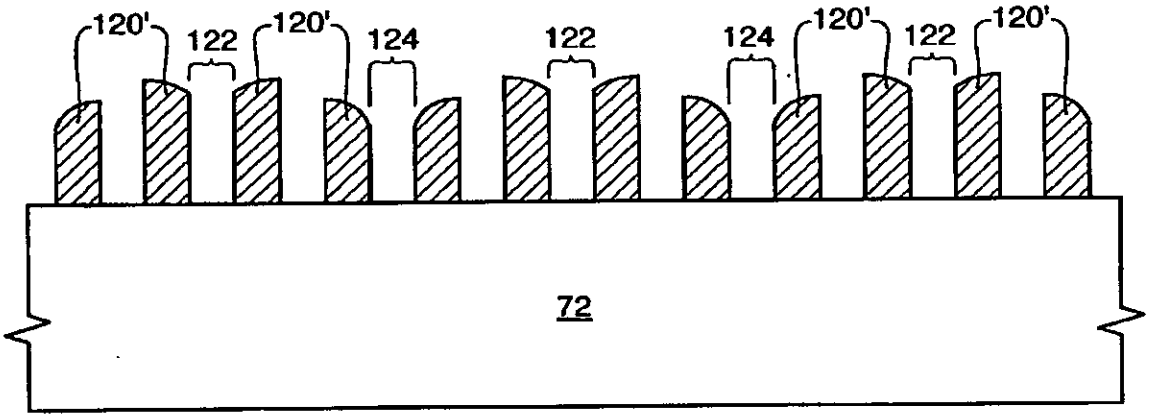


FIG. 14

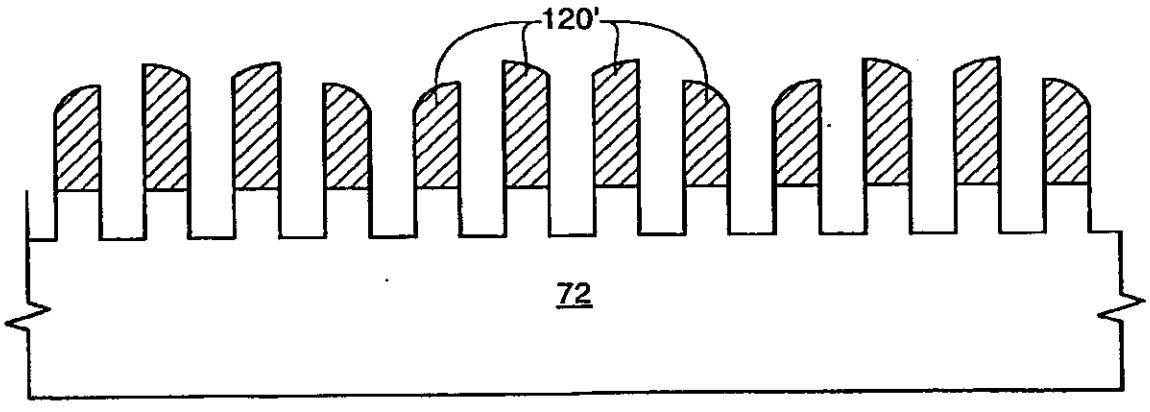


FIG. 15

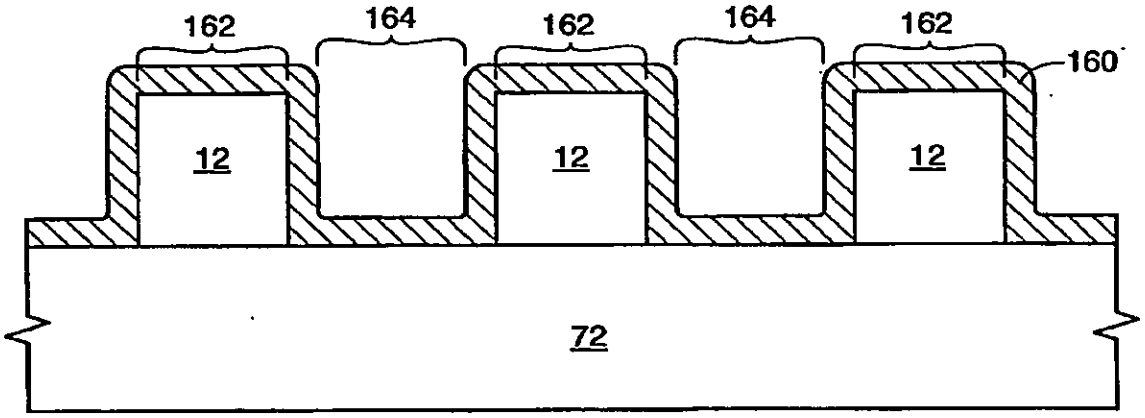


FIG. 16

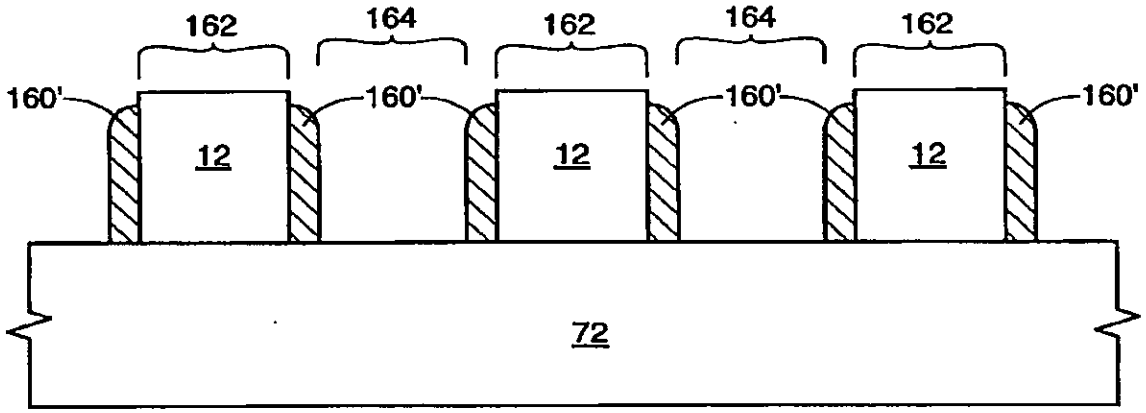


FIG. 17

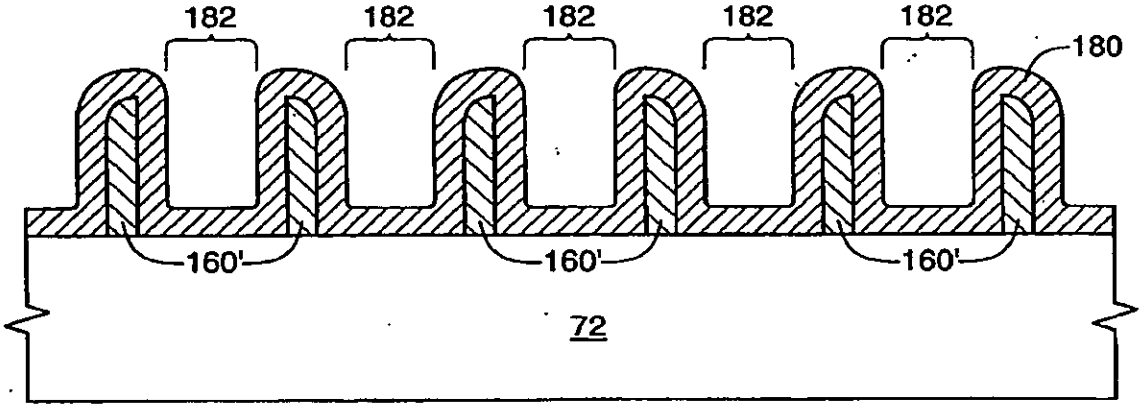


FIG. 18

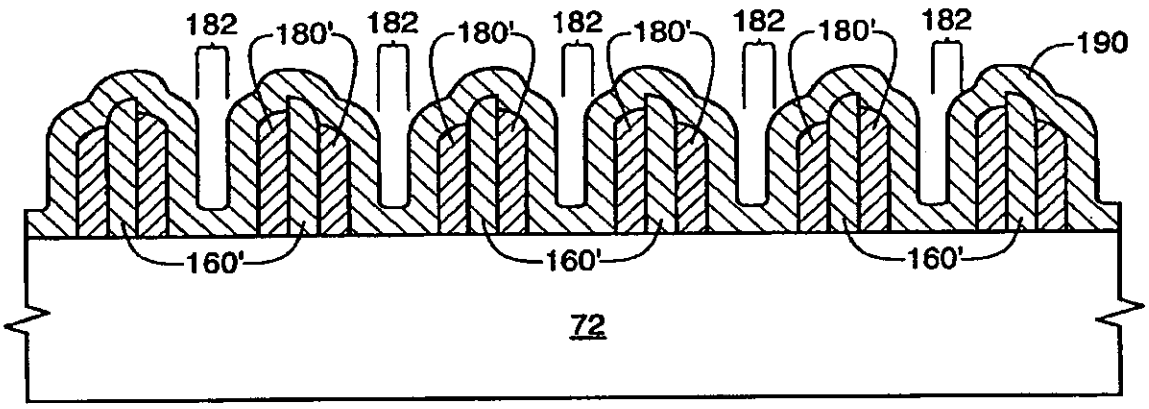


FIG. 19

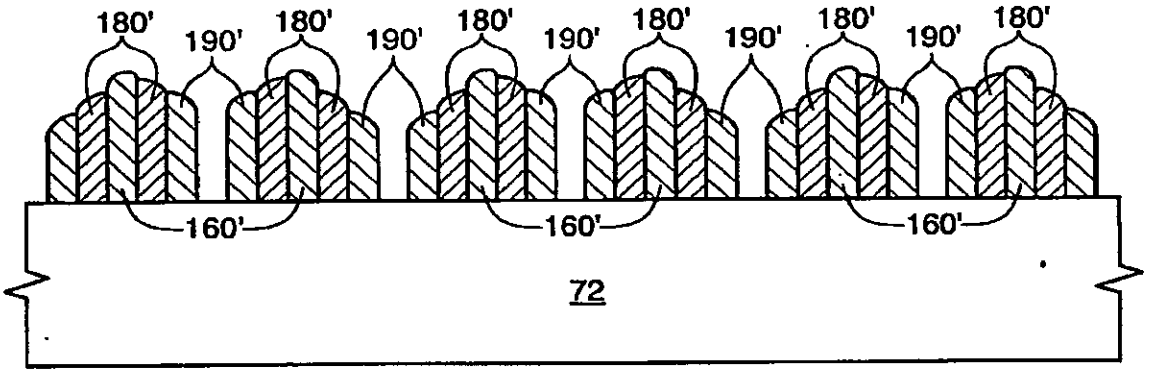


FIG. 20

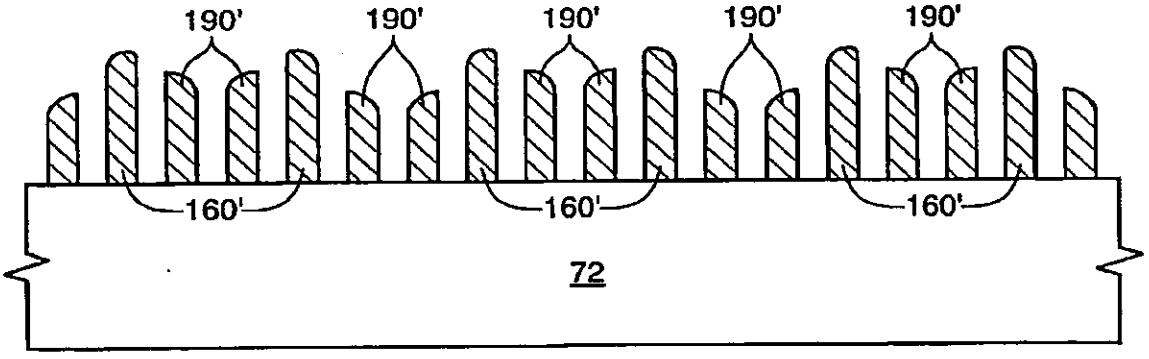


FIG. 21

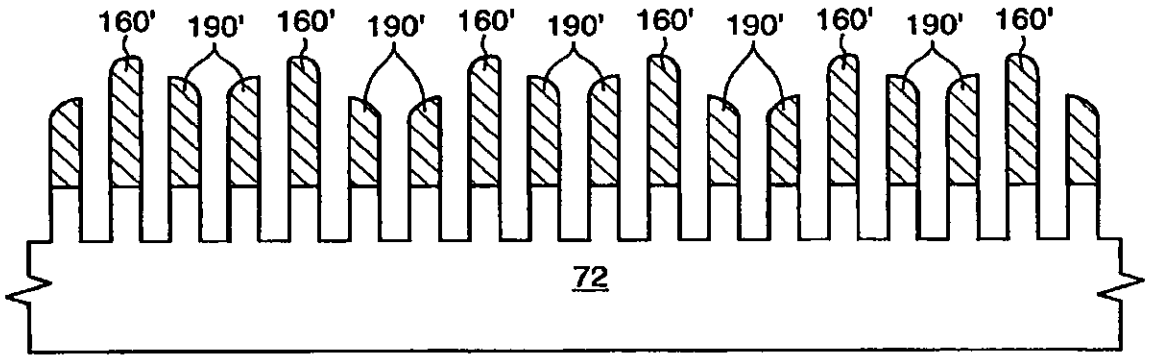


FIG. 22

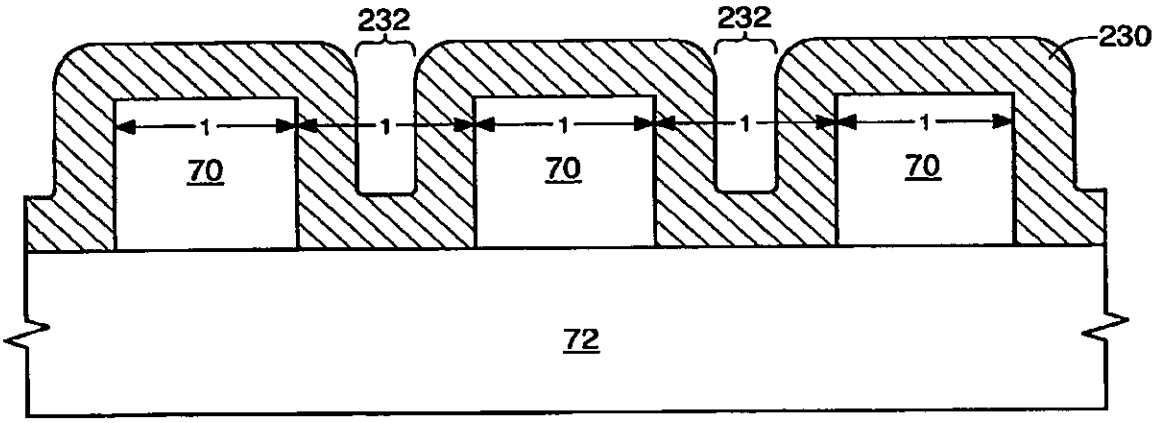


FIG. 23

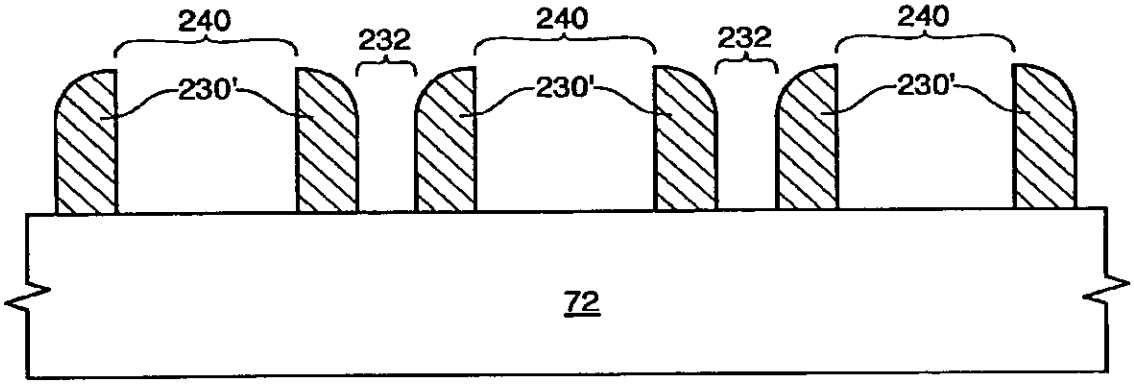


FIG. 24

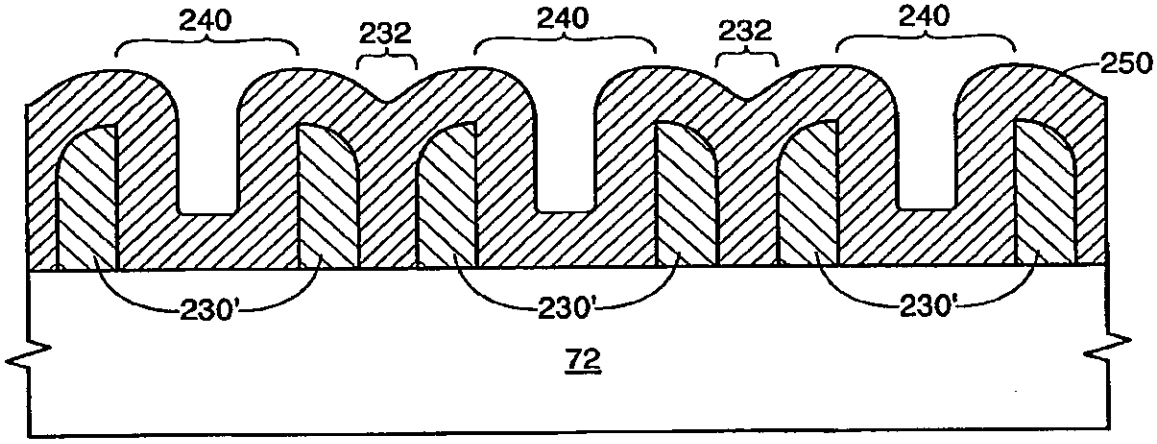


FIG. 25

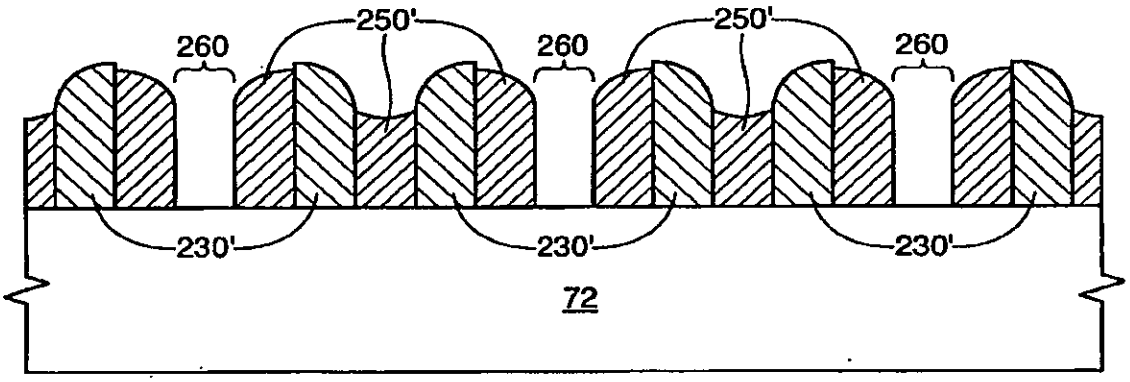


FIG. 26

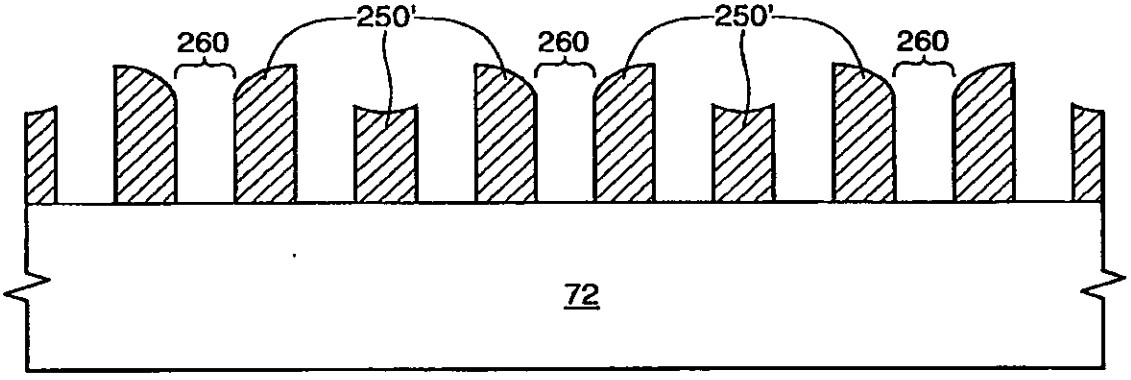


FIG. 27

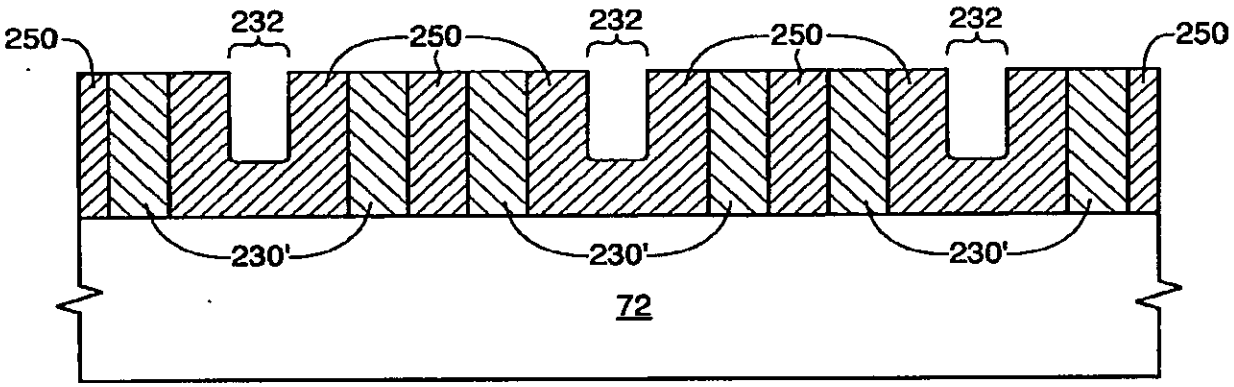

250
232
250
232
250
232
250
230'
230'
230'
72

FIG. 28

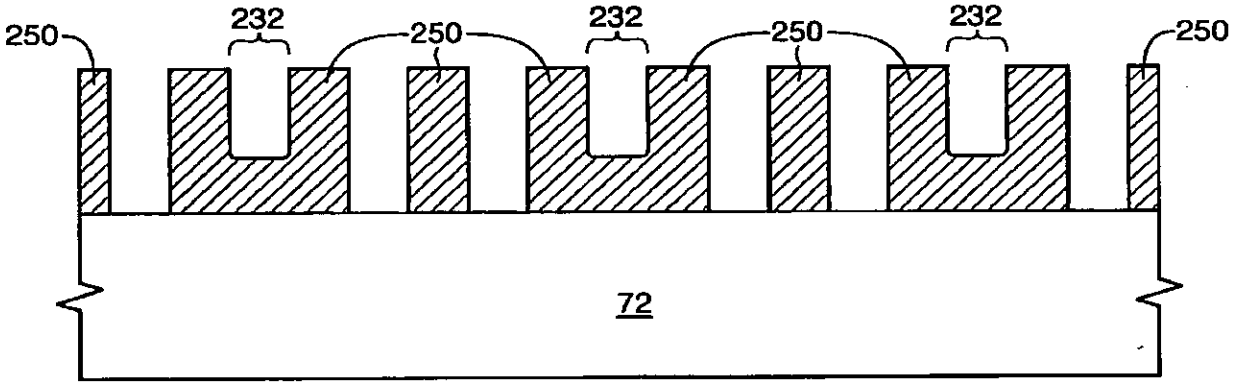

250
232
250
232
250
232
250
72

FIG. 29

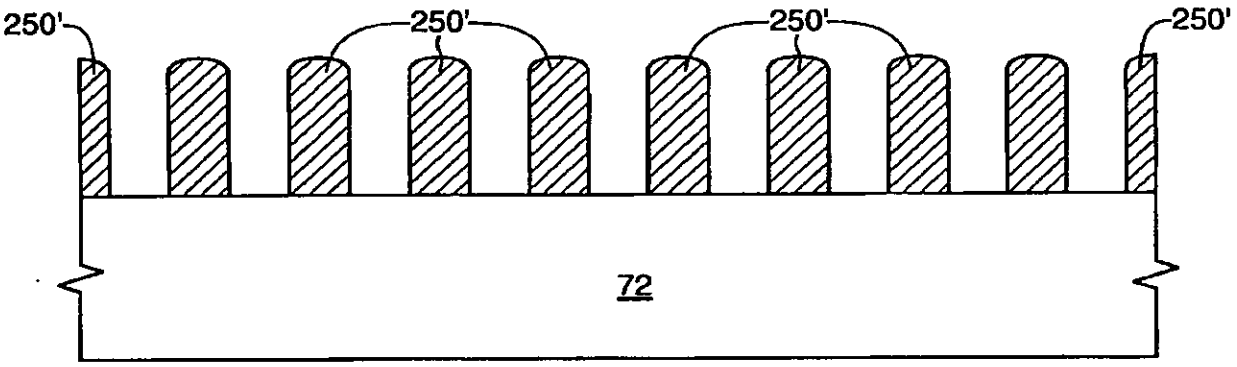


FIG. 30

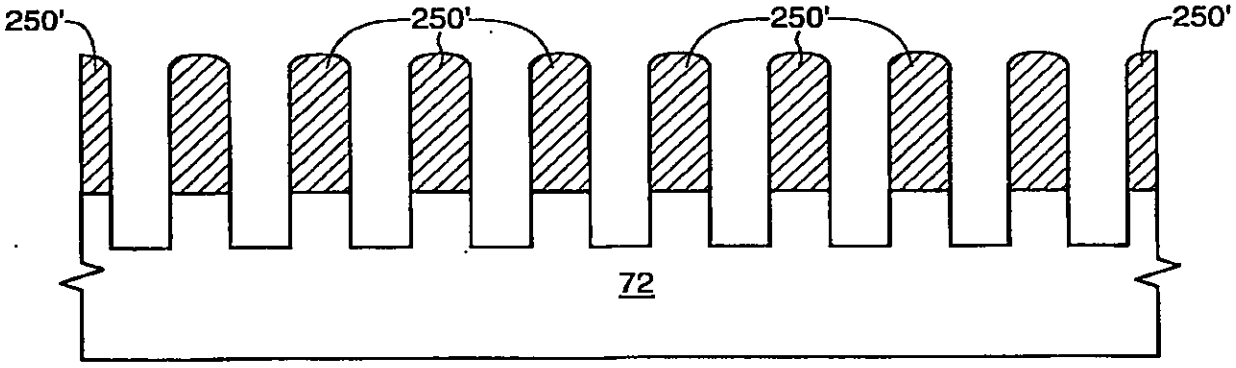


FIG. 31

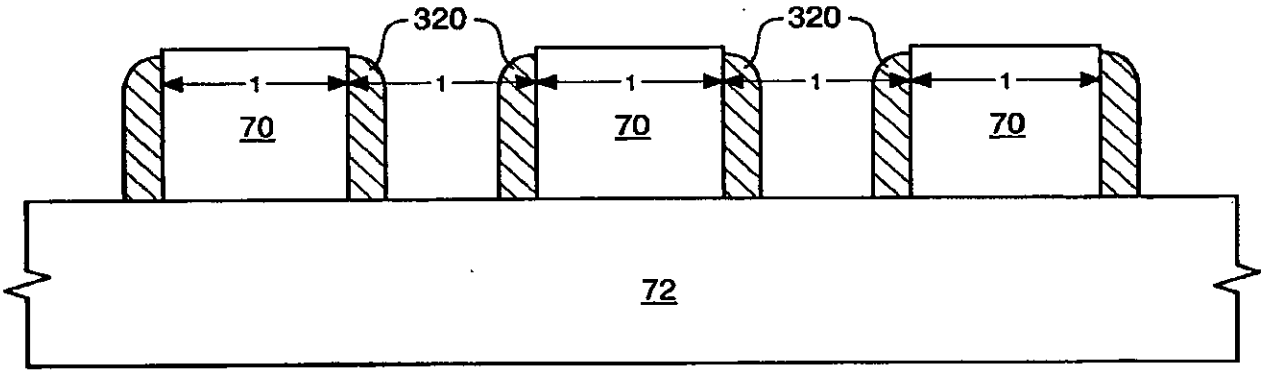


FIG. 32

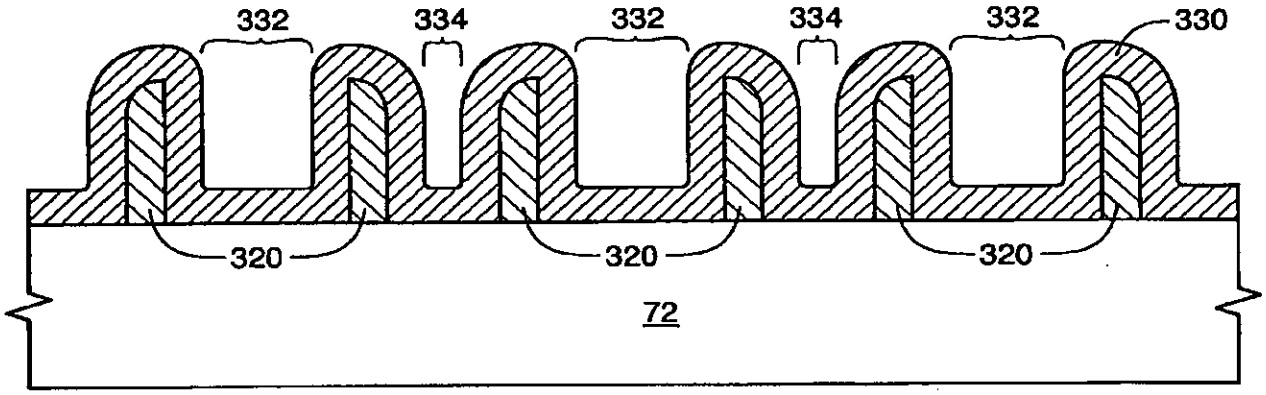


FIG. 33

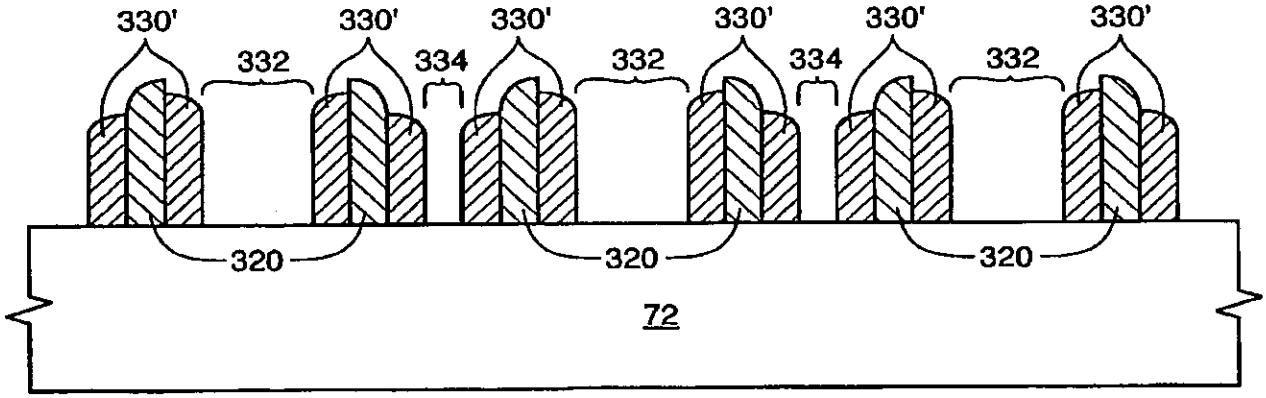


FIG. 34

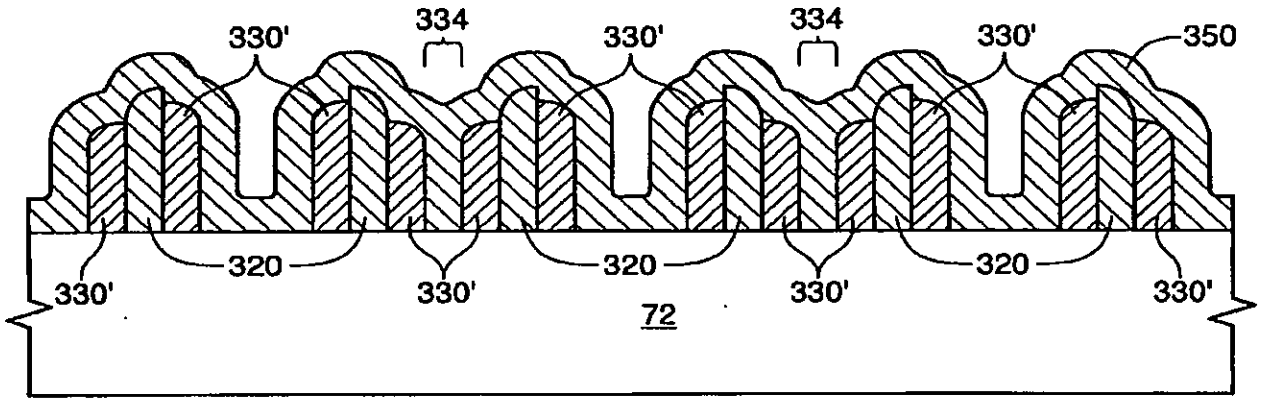

330'
334
330'
334
330'
350
320
320
320
330'
330'
330'
330'
72

FIG. 35

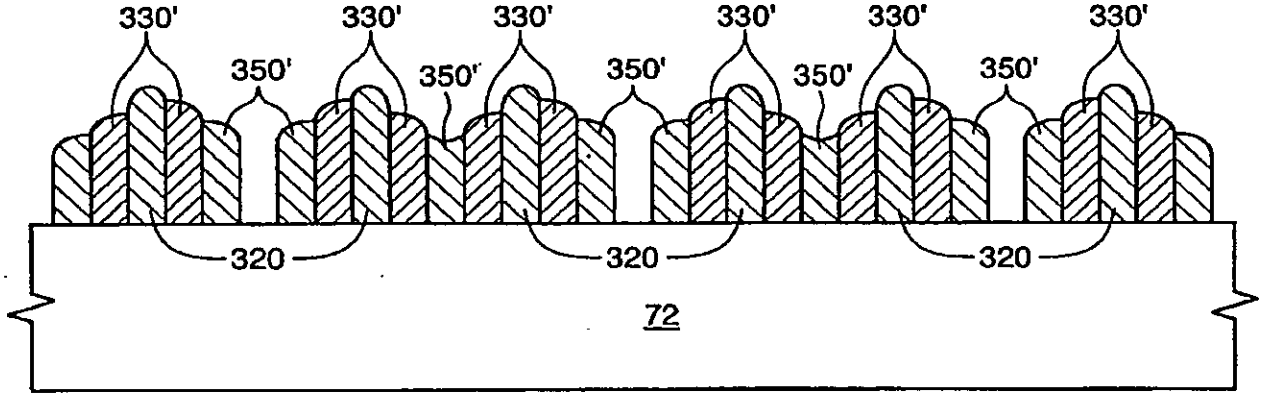

330'
330'
330'
330'
330'
330'
350'
350'
350'
350'
350'
320
320
320
72

FIG. 36

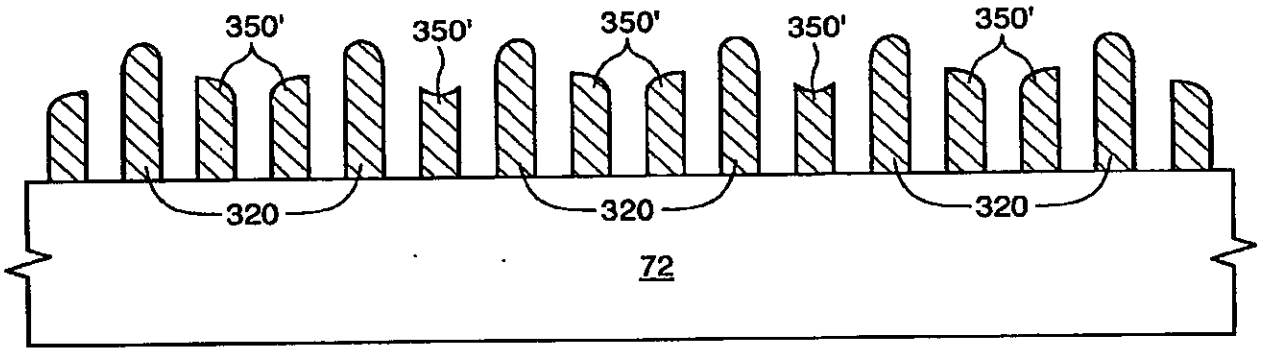

350'
350'
350'
350'
350'
320
320
320
72

FIG. 37

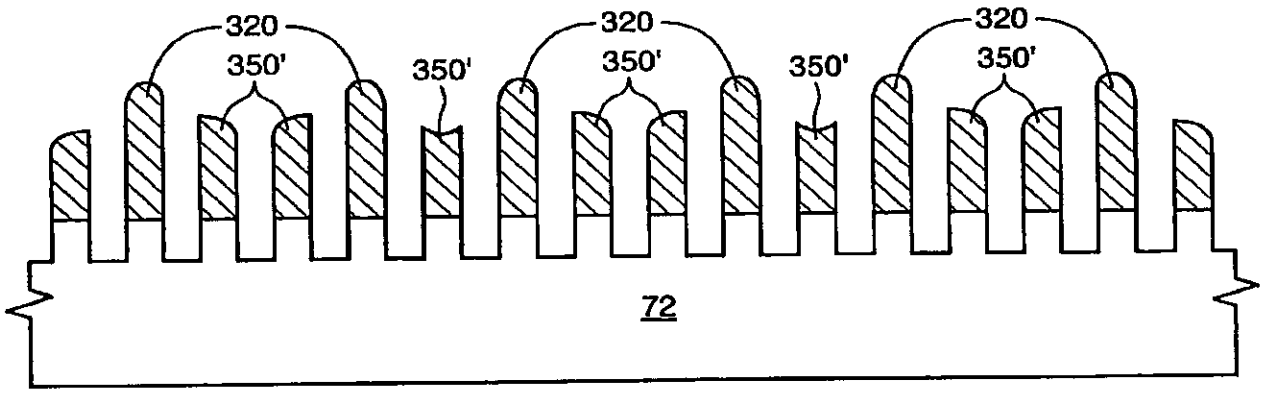

320
320
320
350'
350'
350'
350'
350'
72

FIG. 38

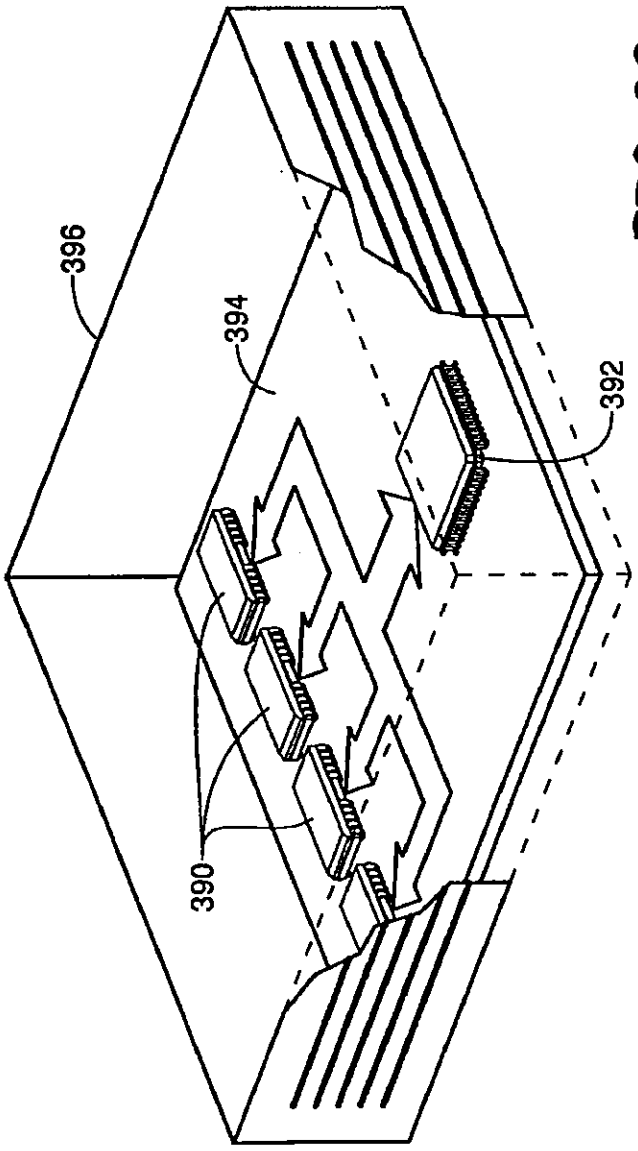


FIG. 39

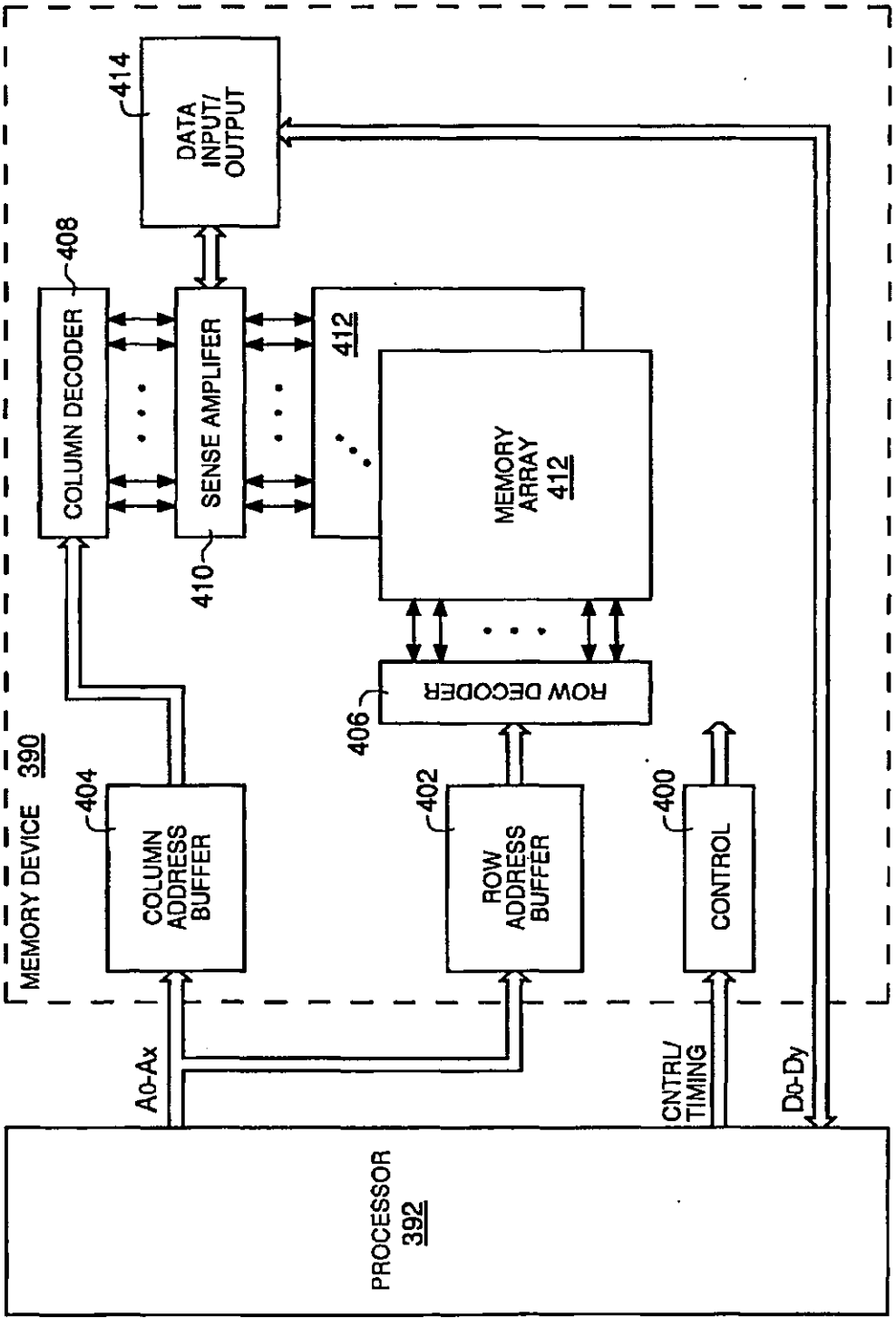

MEMORY DEVICE 390
DATA INPUT/ OUTPUT
414
COLUMN DECODER
408
SENSE AMPLIFER
410
412
MEMORY ARRAY 412
ROW DECODER
406
COLUMN ADDRESS BUFFER
404
ROW ADDRESS BUFFER
402
CONTROL
400
A0-Ax
CNTRL/ TIMING
D0-Dy
PROCESSOR 392

FIG. 40