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(57) Abstract

In a scalable data processing apparatus, particularly a data storage apparatus, one or more thin–film devices which form a substantially planar layer comprise a plurality of sublayers of thin film. Two or more thin–film devices are provided as an integrated stack of the substantially planar layers which form the thin–film devices, such that the apparatus thereby forms a stacked configuration. Each thin–film device comprises one or more memory areas which form matrix addressable memories and additionally circuit areas which form electronic thin–film circuitry for controlling, driving and addressing memory cells in one or more memories. Each memory device has an interface to every other thin–film device in the apparatus, said interfaces being realized with communication and signal lines as well as supporting circuitry for processing extending vertically through dedicated interface areas in the thin–film device.

