ABSTRACT OF THE DISCLOSURE

MULTI-CHIP CHIP-SCALE INTEGRATED CIRCUIT PACKAGE

A multi-chip chip-scale integrated circuit (IC) package is provided to pack two chips in the same IC package. The overall size of the resulting IC package is only slightly larger than the size of the chips enclosed therein. The two chips are mounted in a face-to-face manner on a film carrier by using the flip-chip or controlled collapse chip connection technique in which conductive bumps are used to bond and electrically connect the two chips to the corresponding conductive wires on the insulating film. Furthermore, an insulating compound is formed from an insulating material filled between the two chips in such a manner as to cover the component surfaces of the two while uncovering the backs of the same. The multi-chip chip-scale IC package allows a higher heat-dissipating efficiency by exposing the backs of the chips in the IC package and being arranged in such a manner that the back of one chip is coupled to a printed circuit line on the circuit board, while the back of the chip is coupled to a heat-dissipating device. Moreover, it allows the signal transmission path between the chips and the external circuitry to be shorter than in the prior art, thus increasing the performance of the chips.

Figure 3