CLAIMS

1. A method comprising:

patterning mandrels on a liner, wherein the liner is located on a semiconductor substrate;

forming spacers on sidewalls of the mandrels;

forming dielectric material lines on exposed surfaces of the liner and within a plurality of gaps between the spacers;

removing the mandrels;

removing at least one of the dielectric material lines within at least one of the plurality of gaps between the spacers;

forming conductive metal within each gap;

patterning the conductive metal to form metal interconnect lines and vias; and

removing the plurality of spacers and the remaining dielectric material lines.

2. The method of claim 1, wherein forming the dielectric material layer on the exposed portions of the liner comprises:

depositing dielectric material to a height above the mandrels, via a process selected form the group consisting of: spin-on-glass and flowable chemical vapor deposition; and

reducing the height of the dielectric material to form the dielectric material layer and expose a top surface of the mandrels utilizing a planarization process.

3. The method of claim 1, wherein the spacers are composed of titanium nitride (TiN).

4. The method of claim 1, wherein the conductive metal is selected from the group consisting of: ruthenium (Ru), molybdenum (Mo), cobalt (Co), aluminum (Al), tungsten (W), and rhodium (Rh).

5. The method of claim 1, further comprising:

subsequent to removing the plurality of spacers and the remaining dielectric material lines, removing exposed portions of the liner.

6. The method of claim 1, wherein the at least one of the dielectric material lines comprises a plurality of the dielectric material lines.

7. The method of claim 1, wherein patterning the conductive metal to form the metal interconnect lines and the vias utilizes a subtractive patterning process.

~~8. A semiconductor structure comprising:~~

~~a semiconductor substrate;~~

~~a liner on a portion of a surface of the semiconductor substrate; and~~

~~conductive metal patterned to form interconnect lines and vias on a surface of the liner.~~

~~9. The semiconductor structure of claim 8, wherein no portion of the liner is externally exposed.~~

~~10. The semiconductor structure of claim 8, wherein the conductive metal is selected from the group consisting of: ruthenium (Ru), molybdenum (Mo), cobalt (Co), aluminum (Al), tungsten (W), and rhodium (Rh).~~

~~11. The semiconductor structure of claim 8, wherein the liner is composed of a selection from the group consisting of: titanium nitride (TiN), tantalum nitride (TaN), titanium (Ti), and tantalum (Ta).~~

8. A method comprising:

providing a dielectric layer located on a liner, wherein the liner is located on a surface of a semiconductor substrate;

forming a plurality of trenches of a depth that exposes a surface of the liner and creates dielectric material lines from the remaining dielectric layer;

forming spacers on sidewalls of the dielectric material lines, wherein a first gap is present between two of the spacers;

removing at least one of the dielectric material lines that is between two of the spacers, creating at least a second gap;

forming conductive metal within each gap, including at least the first gap and the second gap, present between the spacers;

patterning the conductive metal to form metal interconnect lines and vias; and

removing the spacers and the remaining dielectric material lines.

9. The method of claim 8, wherein a width of the trench is equal to a sum of a desired metal interconnect line width and expected spacer thickness.

10. The method of claim 8, wherein a width of the trench is three times greater than a desired metal interconnect line width.

11. The method of claim 8, wherein the spacers are composed of titanium nitride (TiN).

12. The method of claim 8, wherein the conductive metal is selected from the group consisting of: ruthenium (Ru), molybdenum (Mo), cobalt (Co), aluminum (Al), tungsten (W), and rhodium (Rh).

13. The method of claim 8, further comprising:

subsequent to removing the spacers and the remaining dielectric material lines, removing exposed portions of the liner.

14. The method of claim 8, wherein patterning the conductive metal to form the metal interconnect lines and the vias utilizes a subtractive patterning process.