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WIRING BOARD FOR BUMP BONDING, SEMICONDUCTOR DEVICE ASSEMBLED FROM THE WIRING BOARD AND MANUFACTURING METHOD OF WIRING BOARD FOR BUMP BONDING

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a wiring board for bump bonding used for a semiconductor package which is employed in various electric equipment, a semiconductor device assembled from the wiring board and a manufacturing method of the wiring board for bump bonding.

Description of the Related Art:

In order to meet recent demands for miniaturization and weight saving in electronic equipment, the configuration of semiconductor packages is shifting from wire bonding types which employ gold wires for electric connection between a semiconductor package and a wiring board, toward bump bonding types that are more advantageous for miniaturization. In a semiconductor package of this bump bonding type, electric connections between a semiconductor chip and a wiring material to which the chip is mounted are obtained through electrode pads of the semiconductor chip and bumps formed on the wiring material to which the chip is mounted.

Conventionally, for a wiring material having such bumps, a photo resist is applied on a surface of a conductive layer

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of a material consisting of a polyimide film having a conductive layer such as copper foil for example, provided on one surface, and it is masked with a mask of a desired pattern, exposed and developed to obtain an etching pattern, and the conductive layer is then etched to obtain a desired wiring pattern. Next, a laser of excimer, carbonic acid gas or the like is irradiated from the side of the polyimide film to form via holes with a desired diameter.

Thereafter, on the side of the wiring pattern, an insulating resin film is formed, masking the wiring pattern, and copper plating is then grown from the surface of the conductive layer exposed at the bottom sections of the via holes to form bumps. Next, a laser is irradiated to the insulating resin film to form via holes for external terminals. At last, in order to facilitate the bonding with electrode pads of a semiconductor chip, the exposed copper surface at the bottom sections of the via holes for external terminals and the surfaces of the bumps are gold plated.

In order to bond the wiring material obtained through the above processes to the semiconductor chip, a thermo-compression method or a thermo-compression method combined with ultrasonic is employed, and in addition, in the via holes for forming the external terminals, solder bumps are formed for mounting on a printed wiring board.

However, according to the above described conventional

manufacturing method, since discontinuous sections of grain boundaries occur at an interface between the copper foil which is a raw material of the copper wiring and a bump formed by the plating, there has been a problem that a broken connection is likely to occur as the bump and the wiring come apart at the interface due to a stress generated at the time of bonding to the semiconductor chip.

In addition, since the bumps are formed by growing the metal plating from the bottom sections of the via holes, the plating must be at least in a thickness equal to or greater than that of the polyimide film which is the insulating resin layer, thus a long time has been required for the metal plating process, and this causes inability to improve productivity.

Furthermore, since the bumps are grown by metal plating, it has been unable to reduce the deviations in the heights of the bumps.

SUMMARY OF THE INVENTION

The present invention was made in consideration of the above conditions, and its object is to provide a wiring board for bump bonding which allows to prevent broken connections between the bumps and wiring, and have small deviation of bump heights and superior productivity, and a semiconductor device assembled from the wiring board and a manufacturing method of the wiring board for bump bonding.

In order to solve the above problems, a wiring board for bump bonding associated with the first mode of the present invention comprises an insulating layer, a wiring layer provided on one surface of the insulating layer, having integral bumps in desired positions, and a protective resist layer provided on the one surface of the insulating layer, with the surfaces of the bumps being exposed, and wherein via holes are provided on the other surface of the insulating layer.

Moreover, a semiconductor device associated with the second mode of the present invention is characterized in that it is assembled by using the wiring board for bump bonding having the above described configuration.

Furthermore, a manufacturing method of a wiring board for bump bonding associated with the third mode of the present invention comprises;

(a) a process providing a first resist layer on a surface of a conductive layer provided on one surface of an insulating layer;

(b) a process performing exposure and development and removing the first resist layer in areas other than bump formation regions;

(c) a process performing half etching on the conductive layer exposed to form bumps;

(d) a process providing a second resist layer on the conductive layer;

(e) a process performing exposure, development and etching on the conductive layer exposed to form a wiring pattern;

(f) a process providing a protective resist layer on an entire surface on the side of the wiring pattern;

(g) a process performing exposure and development to have surfaces of the bumps exposed, and curing the protective resist layer;

(h) a process providing a third resist layer on an other surface of the insulating layer;

(i) a process performing exposure and development on the third resist layer to form an etching pattern; and

(j) a process forming via holes by etching the insulating layer which has been exposed; and wherein;
after the exposed insulating layer is etched to form via holes, metal plating is further applied to the surface of the conductive layer at the exposed bottom surfaces of the via holes and the surfaces of the bumps, the conductive layer being copper, and the insulating layer being a polyimide film.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a cross sectional view of one embodiment of a wiring board for bump bonding according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Hereafter, the present invention is explained in conjunction with the attached figure.

Fig. 1 is a schematic showing a wiring board for bump bonding of the first embodiment according to the present invention, and it is configured by providing a wiring layer 3 made of copper etc. having bumps 2 in desired positions as its integral parts, on one surface of an insulating layer 1 such as a polyimide film, and on the side of the wiring layer 3 provided on the one surface of the insulating layer 1, providing a protective resist layer 4 so as to have the surfaces of the bumps 2 exposed, and by providing via holes 5 on the other surface of the insulating layer 1 on the side of the insulating layer 1, and preferably it is so configured that the surfaces of the bumps 2 and the bottom surfaces of the via holes 5 are metal plated with gold or silver plating 2-1, 5-1.

Also, the use of the wiring board for bump bonding according to the present invention allows to assemble a semiconductor device extremely easily by bonding a semiconductor chip and bumps in the same manner as the conventional method, and by filling the via holes with solder balls and, through this, by bonding to a printed wiring board.

Next, to explain a manufacturing processes of the wiring board for bump bonding according to the present invention, it is as follows.

First, using a copper-polyimide substrate in which an insulating layer such as a polyimide film having a conductive layer made of, preferably a copper foil laminated on its one surface, a dry film resist layer is provided by lamination on a surface of the substrate on the side of the copper foil.

Next, the dry film resist layer is masked, exposed by irradiating a UV beam, and developed, then the dry film resist layer is eliminated in the area other than the sections on which bumps are to be formed.

The conductive layer of the copper foil etc. which has been exposed in this way is half etched to form bumps.

Thereafter, a resist film similar to the above is provided on the side of the conductive layer by lamination, but as necessary, it is desirable to eliminate the dry film resist layer on the bumps beforehand.

The laminated resist layer is masked with a mask having a desired wiring pattern, and exposed by irradiating a UV beam, then the conductive layer which has been exposed after developing is etched to form the wiring pattern.

Moreover, a dry film resist is laminated to the entire surface of the wiring pattern side through vacuum lamination for example, to form a protective resist layer, but it is desirable to eliminate the prior resist layer on the wiring pattern beforehand as necessary.

Following the above, the protective resist layer is

exposed and developed to eliminate the dry film resist on the bumps, and thereafter, the protective resist layer is cured.

For the resist layer used as the protective resist layer, a method to apply a liquid type or a method to laminate a dry film formed beforehand as a resin film by lamination etc. may be employed, however, in terms of ease in forming a film with an even thickness, the dry film resist is preferred.

Thereafter, a dry film resist layer is provided by lamination on the surface of the polyimide which is the insulating layer of the copper-polyimide substrate.

At this point, it is preferable to provide a similar dry film resist layer also on the entire surface of the wiring pattern side to protect the bumps from a subsequent etching process.

Next, the above dry film resist layer is masked, exposed and developed to form an etching pattern on the insulating layer.

The exposed polyimide which is the insulating layer is etched to form via holes.

According to the present invention, by going through these processes, a wiring board for bump bonding can be manufactured.

Moreover, in the present invention, it is desirable to apply metal plating on the surface of the conductive layer at the bottom surfaces of the via holes formed as the above and

the surfaces of the bumps, and at this point, a plating such as silver plating or gold plating etc. can be selected as desired.

As the above, according to the present invention, since the bumps and the wiring are integrally configured by the same conductive layer, discontinuous sections of grain boundaries would not occur between the bumps and the wiring, and moreover, since the formation of the bumps are performed by the half etching, the time-taking metal plating process required in the conventional method would not be necessary, thus it would yield extremely superior productivity.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following, an embodiment of the present invention is explained along with a comparative example.

Example:

First of all, a resist layer is formed by laminating a negative dry film resist of an alkali development type in a thickness of 15μm on a copper foil side of a copper-polyimide substrate which consists of a polyimide film with a thickness of 50μm, width of 35mm, and length of 20cm, having the copper foil in a thickness of 25μm provided on its one surface, and the resist layer is masked, exposed by irradiating a UV beam at a strength of 200mJ, and developed, so that patterns are formed at an interval of 19mm in the length direction, each

for formation of 200 bumps at an interval of 120μm in the width direction of the copper foil of the copper polyimide substrate.

Next, by having the exposed area of the copper foil come into contact with an etching solution consisting of commercial cupric chloride at a temperature of 40°C, the area of the copper foil is half etched to form bumps, and thereafter, the etching resist layer on the bumps is delaminated by a sodium hydroxide solution and eliminated.

Furthermore, a dry film resist layer of the same type as the above is laminated on the copper foil side, and it is masked with a mask having a desired wiring pattern, similarly exposed and developed so that the wiring pattern is formed.

Next, in the same manner as the above, the copper foil is etched to form the wiring pattern, and the etching resist layer is then delaminated and eliminated.

Thereafter, an alkali development type dry film resist in a thickness of 35μm is laminated on the entire surface on the side of the wiring pattern by a vacuum lamination method. The laminated dry film resist layer is then exposed and developed, and the dry film resist layer on the surfaces of the bumps is eliminated, then a curing treatment on the remaining dry film resist layer is performed by heating the substrate to 170°C.

Thereafter, on both the wiring pattern side and the polyimide film side, dry film resist layers in a thickness of

25μm, that are tolerant to alkaline are laminated, and the surface of the resist layer on the polyimide side of the substrate is masked by a given mask, exposed and developed to form openings with a diameter of 220μm, and by etching the exposed sections of the polyimide film to form via holes. Thereafter, the remaining resist layers on the both sides are eliminated.

At last, the bottom surfaces of the via holes and the surfaces of the bumps are plated by electro-plating of gold in a thickness of approximately 2μm using a commercial cyanogen type gold plating solution.

When the bumps of the wiring board for bump bonding obtained through the above processes were observed by an optical microscope with magnification of 400, it was found that bumps obtained had a cross sectional shape of a trapezoid. Moreover, when this wiring board for bump bonding is studied for broken connections between the bumps and the wiring by a destructive inspection after performing thermo-compression bonding to a printed wiring board with a load of 100gf/bump, temperature at 300°C and duration of 30 seconds, no broken connections were observed.

Comparative Example:

A resist layer is formed by laminating a negative dry film resist of an alkali development type on a copper foil side of a copper-polyimide substrate which consists of a polyimide

film with a thickness of 30μm, width of 35mm, and length of 20cm, having the copper foil in a thickness of 18μm provided on its one surface, and the resist layer is masked, exposed by irradiating a UV beam at a strength of 200mJ, and developed, so that a wiring pattern is formed.

Following the above, the exposed area of the copper foil is etched by an etching solution consisting of cupric chloride at a temperature of 45°C to form the wiring pattern, and thereafter, the etching resist layer is delaminated and eliminated.

Next, an argon laser is irradiated from the polyimide side of the copper-polyimide substrate so as to form via holes with a diameter of 50μm by which the copper foil is exposed at the bottom sections of the via holes.

After applying an acrylate resin on the wiring pattern side as a protective film for metal plating and drying it, cleaning is performed on the surface of the copper foil at the bottom sections of the via holes using a sulfuric acid type etching solution, and following that, bumps are formed by performing electro-plating for 0.5 hour using copper sulfate plating solution. Thereafter, using a keton type solvent, the acrylate resin protective film is dissolved and eliminated.

Moreover, a solder resist of an alkali development type is printed on the entire surface of the wiring pattern side, and it is masked by a specified mask, exposed and developed

to provide opening sections of 200μm, the substrate is then heated to 170°C to perform curing of the solder resist layer. And at last, the opening sections of the resist layer on the wiring pattern side and the surfaces of the bumps are plated by electro-plating of gold in a thickness of 2μm using a commercial cyanogen type gold plating solution.

When the wiring board for bump bonding obtained in this manner was studied for broken connections between the bumps and the wiring by a destructive inspection after performing thermo-compression bonding to a printed wiring board with a load of 100gf/bump, temperature at 300°C and duration of 30 hours, 9 bumps out of 832 bumps were found to be failed.

Effect of the Invention:

As explained heretofore, according to the present invention, since the formation of the wiring is performed by etching after forming the bumps of the wiring board for bump bonding by half etching of the copper foil, the formation of the bumps can be performed effectively, and there would be no occurrence of discontinuous sections of grain boundaries between the bumps and the wiring, and also, since the bumps are formed by performing the half etching on the copper foil which has an even thickness, it is possible to obtain a wiring board having small deviations in the heights of the bumps.

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WHAT IS CLAIMED IS:

1. A wiring board for bump bonding comprising an insulating layer, a wiring layer provided on one surface of said insulating layer, having integral bumps in desired sections, and a protective resist layer provided on said one surface of the insulating layer in such a way so as to have surfaces of said bumps exposed, wherein via holes are provided on an other surface of said insulating layer.

2. The wiring board for bump bonding of claim 1 wherein the surfaces of said bumps and bottom surfaces of said via holes are metal-plated.

3. A semiconductor device assembled from the wiring board for bump bonding as described in claim 1 or 2.

4. A manufacturing method of a wiring board for bump bonding comprising;

(a) a process providing a first resist layer on a surface of a conductive layer provided on one surface of an insulating layer;

(b) a process performing exposure and development, and eliminating said first resist layer in an area other than bump formation regions;

(c) a process performing half etching on the conductive layer exposed to form bumps;

(d) a process providing a second resist layer on said conductive layer;

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(e) a process performing exposure and development, and forming a wiring pattern by etching said conductive layer exposed;

(f) a process providing a protective resist layer on an entire surface on the side of said wiring pattern;

(g) a process performing exposure and development to have surfaces of said bumps exposed, and curing the protective resist layer;

(h) a process providing a third resist layer on an other surface of said insulating layer;

(i) a process performing exposure and development on said third resist layer to form an etching pattern; and

(j) a process forming via holes by etching the insulating layer exposed.

5. The manufacturing method of a wiring board for bump bonding as described in claim 4 wherein, after the formation of the via holes by etching said exposed insulating layer, exposed surface of the conductive layer at bottom surfaces of the via holes and the surfaces of the bumps are metal-plated.

6. The manufacturing method of wiring board for bump bonding as described in claim 4 or 5 wherein said conductive layer is copper, and the insulating layer is a polyimide film.