WHAT IS CLAIMED IS:

1. A nonvolatile memory device comprising:

a substrate;

a first mold structure on the substrate and including a plurality of first gate electrodes;

a second mold structure on the first mold structure and including a plurality of second gate electrodes; and

a plurality of channel structures intersecting the plurality of first gate electrodes and the plurality of second gate electrodes by penetrating the first and second mold structures,

wherein

the first mold structure includes first and second stacks, which are spaced apart from each other by a first block trench, and

the second mold structure includes a third stack, stacked on the first stack, a fourth stack, stacked on the second stack, and first connecting parts, which connect the third and fourth stacks, wherein the third and fourth stack are partially spaced apart from each other by a second block trench, and

wherein the second block trench is connected to the first block trench.

2. The nonvolatile memory device of claim 1, wherein

the first mold structure includes the first block trench, which separates the first and second stacks, and

the first connecting parts do not overlap with the first block trench in a plane that is perpendicular to a top surface of the substrate.

3. The nonvolatile memory device of claim 1, wherein bottom surfaces of the first connecting parts are spaced apart from a top surface of the substrate.

4. The nonvolatile memory device of any one of claims 1 to 3, further comprising:

a third mold structure on the second mold structure and including a plurality of third gate electrodes,

wherein the channel structures intersect the third gate electrodes by penetrating the third mold structure.

5. The nonvolatile memory device of claim 4, wherein the third mold structure includes a fifth stack, stacked on the third stack, a sixth stack, stacked on the fourth stack, and second connecting parts, which connect the fifth and sixth stacks.

6. The nonvolatile memory device of claim 4, wherein

the third mold structure includes a fifth stack, stacked on the third stack, and a sixth stack, stacked on the fourth stack, and

the fifth and sixth stacks are spaced apart from each other.

7. The nonvolatile memory device of any one of claims 1 to 3, further comprising:

a third mold structure between the first and second mold structures and including a plurality of third gate electrodes,

wherein the channel structures intersect the third gate electrodes by penetrating the third mold structure.

8. The nonvolatile memory device of claim 7, wherein the third mold structure includes a fifth stack, stacked between the first and third stacks, a sixth stack, stacked between the second and fourth stacks, and second connecting parts, which connect the fifth and sixth stacks.

9. The nonvolatile memory device of claim 7, wherein

the third mold structure includes a fifth stack, stacked between the first and third stacks, and a sixth stack, stacked between the second and fourth stacks, and

the fifth and sixth stacks are spaced apart from each other.

10. The nonvolatile memory device of any one of claims 1 to 9, wherein

the second mold structure includes a cutting line, in the first connecting parts, and

the cutting line cuts an uppermost second gate electrode among the second gate electrodes.

11. A nonvolatile memory device comprising:

a substrate;

a first mold structure on the substrate and including a plurality of first gate electrodes;

a second mold structure on the first mold structure and including a plurality of second gate electrodes;

a plurality of channel structures intersecting the first gate electrodes and the second gate electrodes by penetrating the first and second mold structures; and

bit lines extending in a first direction, the bit lines being connected to the channel structures, wherein the first mold structure includes a first block trench, which extends in a second direction that intersects the first direction, to completely cut the first mold structure,

the second mold structure includes a plurality of second block trenches, which expose part of the first block trench, and

the second block trenches are spaced apart from one another and are arranged in the second direction,

wherein a second block trench among the plurality of second block trenches is connected to the first block trench.

12. The nonvolatile memory device of claim 11, wherein

the first mold structure further includes a third block trench, which is spaced apart in the first direction from the first block trench and extends in the second direction to completely cut the first mold structure,

the second mold structure includes a plurality of fourth block trenches, which expose part of the third block trench, and

the fourth block trenches are spaced apart from one another and are arranged in the second direction.

13. The nonvolatile memory device of claim 11 or claim 12, further comprising:

a peripheral circuit structure below the substrate.

14. The nonvolatile memory device of any one of claims 11 to 13, wherein the channel structures include semiconductor patterns, which penetrate the first and second mold structures, and information storage films, which are between the semiconductor patterns and each of the plurality of first and second gate electrodes.

15. The nonvolatile memory device of claim 14, further comprising:

a source structure between the substrate and the first mold structure,

wherein the channel structures are connected to the substrate through the source structure, and

the source structure is connected to the semiconductor patterns through the information storage films.

16. A nonvolatile memory device comprising:

a substrate;

a first mold structure on the substrate and including a plurality of first gate electrodes;

a second mold structure on the first mold structure and including a plurality of second gate electrodes;

a plurality of channel structures intersecting the first gate electrodes and the second gate electrodes by penetrating the first and second mold structures;

bit lines extending in a first direction, the bit lines being connected to the channel structures;

a first word line trench extending in a second direction that intersects the first direction, the first word line trench cutting the first gate electrodes and the second gate electrodes;

a second word line trench extending in the second direction, the second word line trench cutting the first gate electrodes and the second gate electrodes; and

a first block trench extending, between the first and second word line trenches, in the second direction, the first block trench cutting the first gate electrodes,

wherein

the first mold structure includes first and second stacks, which are separated by the first block trench, and

the second mold structure includes a third stack, stacked on the first stack, a fourth stack, stacked on the second stack, and a plurality of first connecting parts, which connect the third and fourth stacks, wherein the third and fourth stack are partially spaced apart from each other by a second block trench, and

wherein the second block trench is connected to the first block trench.

17. The nonvolatile memory device of claim 16, wherein

the second mold structure includes a plurality of cutting lines, which extend in the second direction in the first connecting parts, and

the plurality of cutting lines cut an uppermost second gate electrode among the second gate electrodes.

18. The nonvolatile memory device of claim 16, wherein the second mold structure includes a fifth stack, spaced apart from the third stack by the first word line trench, and a plurality of second connecting parts, which connect the third and fifth stacks.

19. The nonvolatile memory device of claim 18, wherein the second gate electrodes are in part in the second connecting parts.

20. The nonvolatile memory device of claim 18 or claim 19, wherein the second mold structure further includes a cutting line, in the second connecting parts and cuts the second gate electrodes.