A BUS CONTROLLING METHOD AND EQUIPMENT USING THE METHOD

ABSTRACT OF THE DISCLOSURE

With respect to design regarding a bus cycle, it has been necessary to consider a data conflict, if an output disable time of a device is long. A bus controlling unit is installed in a processor. In the bus controlling unit, parameters regarding output disable times of external devices such as a first device are utilised. When a device with a long output disable time is read in a bus cycle, an idle state is forcibly inserted before a following bus cycle activation to avoid a data conflict.

FIGURE 1