

Abstract

5 A detector (10) for vertical synchronizing pulses comprises a nonwrapping up/down counter (14) and a comparator (18). The counter (14) samples the level of a composite synchronizing signal at a sampling rate. The counter (14) has a numerical output which increases responsive to detection of said level during a sample interval and decreases responsive to nondetection of said level during a sample interval. The comparator (18) generates a vertical sync detection pulse when the numerical output of the counter (14) is greater than a reference value. In order to provide hysteresis, the numerical value is alternately one of first and second numerical reference counts, the first reference count being greater than the second reference count. The comparator (18) initiates the vertical sync detection pulse when the numerical output of the counter (14) rises above the first reference count and terminates the vertical sync detection pulse when the numerical output of the counter (14) falls below the second reference count. The numerical reference supplied to the comparator (18) is changed at times corresponding to initiation and termination of each vertical sync detection pulse. A pulse shaping circuit may comprise a latch (22) for sampling the output of the comparator (18) and generating a vertical synchronizing signal.

Reference Indicia Are From Fig. 1

This Sheet Has Been Replaced

