

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN FRAME ALIGNERS FOR T.D.M. COMMUNICATION SYSTEMS

(71) We THE PLESSEY COMPANY LIMITED, a British Company of Vicarage Lane, Ilford, Essex IG1 4AQ do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The present invention relates to improvements in frame aligners for use in time division multiplex (t.d.m.) communication systems.

In telephone switching networks it is well known to use time division multiplex transmission systems each employing say thirty pulse code modulation (p.c.m.) channels for the passage of speech signals and the like. High quality connections for music channels and television information or the like are handled in a p.c.m. transmission system by using a number of channels spaced apart throughout the 30 information channel frame of the multiplex.

Co-pending application No. 9041/75 (Serial No. 1,498,498) discloses a frame aligner for use in a time division multiplexed communication system which includes means for maintaining a displacement of at least N bit-periods between the t.d.m. frame of a data bit-stream on a data highway incoming to a communication exchange and the t.d.m. frame of that exchange (where N is the maximum number of bits drift experienced between the data bit-stream clock and the exchange clock). The actual displacement used in application No. 9041/75 (Serial No. 1,498,498) is 2N and the aligner includes logic gating arrangements to indicate when the clocks in question become dangerously close so that the read and write counters of the aligner can be displaced by the required number of bit-periods.

The operation of displacing the read and write counters however, causes data corruption since part of a frame is either read twice

or not read at all. This arrangement has the disadvantage that channel order integrity may be lost during the overlap adjustment operation which creates severe distortion as far as the high quality connections are concerned. It is an aim of the present invention therefore to provide a frame aligner which does not suffer from this disadvantage.

According to the invention there is provided a frame aligner for use in a time division multiplex communication system in which a digital data bit-stream is transmitted over a data highway interconnecting a first communication exchange and a second communication exchange, each exchange incorporating its own clock arrangement for defining a time division multiplex frame and bit periods within a frame, wherein the data bit-stream is applied to the frame aligner in the second exchange and the frame aligner includes (i) information storage means for temporarily storing two successive frames of the incoming data stream, the storage means being operated (a) in write mode by a write counter driven from a derived clock pulse source extracted from the incoming data stream and (b) in read mode by a read counter driven from the clock arrangement of the second exchange, and (ii) an overlap detector arranged to detect when the write counter and the read counter approach a clash condition and to advance the read counter by one frame.

The invention will be more readily understood from the following description of one embodiment thereof. The description should be read in conjunction with the drawing accompanying the provisional specification which shows at Figure 1 a schematic diagram of the operation of the clash detection arrangements of the aligner which is shown in block diagram form in Figure 2.

The aligner (Figure 2) comprises a temporary information store RAM fed from a

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“serial-to-parallel” converter circuit SIPO to which the incoming data bit-stream (transmitted by a data highway DH) is connected. The serial-to-parallel converter SIPO applies a 2-bit word to the store RAM and the area of store selected to temporarily hold that word is defined by the write counter WC acting through the address selector AS. The write counter is driven by clock pulses extracted from the data highway by the clock extraction logic CEL and is driven at half the clock rate as a two bit SIPO has been used on the store input path.

The store RAM is operated in read mode under the control of the read counter RC acting through the address selector AS. The read counter is driven by the local clock LCL at half the clock rate and the output of the store RAM is re-converted to serial form by parallel-to-serial converter PISO. Each 2-bit word has a parity bit stored in the store RAM generated by PARGEN which is checked by PARCH as each word is read out.

Accordingly the store RAM provides temporary storage acting as a buffer between the data highway DH and the exchange highway EH framing arrangements producing a locally aligned data bit-stream on highway EH. The store RAM provides storage for two frames worth of information (i.e. 2 times 256 bits for a 32 channel p.c.m. system) and may be implemented as two 256×1 stores in series or preferably using a single chip random access 256×4 store.

The outputs of the read counter RC and the write counter WC are applied to a clash detection logic CDL which is arranged to advance the read counter RC by 256 steps (i.e. 1 frame) when the read count and the write count approach a clash condition within the forbidden band of Figure 1.

Such an arrangement ensures that data loss occurs in an integral frame block to ensure that all the channels of a particular frame are lost or read twice and hence the channel order of multi-slot connections is not affected by aligner operation. Also there is no longer any requirement for inserting delay elements between the aligner store output and the exchange highway as is the case in the prior art aligner referred to above.

The above description has been of one embodiment only. Alternative arrangements can readily be seen by those skilled in the art. For example the incoming data stream is applied to a two-bit serial-to-parallel converter however the data stream could have been fed a bit at a time directly into the store RAM. The use of the converters of the input and output of the store allows a slower random access store to be used as the addressing rate has to be twice the input data rate. Obviously for a slower

access store the number of bits converted could be increased.

WHAT WE CLAIM IS:-

1. A frame aligner for use in a time division multiplex communication system in which a digital data bit-stream is transmitted over a data highway interconnecting a first communication exchange and a second communication exchange, each exchange incorporating its own clock arrangement for defining a time division multiplex frame and bit periods within a frame wherein the data bit-stream is applied to the frame aligner in the second exchange and the frame aligner includes (i) information storage means for temporarily storing two successive frames of the incoming data stream, the storage means being operated (a) in write mode by a write counter driven from a derived clock pulse source extracted from the incoming data stream and (b) in read mode by a read counter driven from the clock arrangement of the second exchange to produce an aligned data bit-stream and (ii) an overlap detector arranged to detect when the write counter and the read counter approach a clash condition and to advance the read counter by one frame.

2. A frame aligner according to claim 1 in which the incoming data stream is fed to a two bit serial-to-parallel converter and succeeding pairs of bits of the data stream are stored at successive addresses in the information storage means under the control of a write counter driven at half the clock rate of the incoming data bit stream.

3. A frame aligner according to claim 2 in which the information store when operated in read mode produces a stream of pairs of bits which are applied to a two bit parallel-to-serial converter to produce the aligned data bit-stream.

4. A frame aligner according to claim 2 or 3 in which a parity bit is generated for each pair and stored in the information store with each pair.

5. A frame aligner substantially as described with reference to the drawings accompanying the provisional specification.

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