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"A two-signal amplifying system".

The present invention relates to a two-signal amplifying system constructed of a BTL (Balanced Transformer-Less) amplifier including a B-class push-pull output circuit, and more particularly to a two-signal amplifying system such as a stereophonic amplifying system constructed of a one-chip or two-chip type monolithic IC (semiconductor integrated circuit).

An ASO (area of safe operation) limiter is well known in the art as the protecting circuit for the output transistor in the amplifying system including the B-class push-pull output circuit.

We have found that the protecting circuit detects the operating state of the output transistors in order to render the limiter transistor conductive, the limiter transistor being connected between the input and output of the output transistors, so that the operation of the output transistors may be limited.

These output transistors have a drawback that they oscillate because they constitute an undesired high-frequency positive feedback loop between their inputs and outputs.

We have further found that in a stereophonic amplifying system including a BTL amplifier a problem arises in that the construction of the protecting circuit becomes complex if the above referred to ASO limiter is arranged for all eight of the output transistors constituting the BTL amplifier in order to prevent the output transistors from being broken down in the event that a short-circuit occurs between the two output terminals due to incorrect wiring or inadequate insulation of the leads to the speakers because the output circuit has an OCL (Output Condenser Less) construction.

On the other hand, by arranging the ASO limiter for those output transistors, which are connected between a power source V_{CC} and an output OUT, at the power source side, which constitute the single power source type B-class push-pull output circuit, those output transistors are rendered non-conductive for a short-circuit or earthed connection so that the output transistors on the earth side are supplied with no

voltage and current and can be indirectly protected. However, we have found that the output voltage and current of one channel are fed, when this channel becomes accidentally short-circuited, through the output terminals to the other channel so that there is a risk that the output transistors of the other channel will be damaged.

It is therefore an object of the present invention to provide a two-signal amplifying system such as a stereophonic amplifier for ensuring adequate protection with the use of a simple circuit.

According to the present invention there is provided a two-signal amplifying system having:

(a) a first BTL amplifier for amplifying a first input signal and a second BTL amplifier for amplifying a second input signal; said first BTL amplifier including a first push-pull output circuit for delivering a non-inverting output signal of the first input signal, and a second push-pull output circuit for delivering an inverting output signal of the first input signal; said second BTL amplifier including a first push-pull output circuit for delivering a non-inverting output signal of the second input signal, and a second push-pull output circuit for delivering an inverting output signal of the second input signal;

(b) a first speaker load connected between an output terminal of the first push-pull output circuit and an output terminal of the second push-pull output circuit of the first BTL amplifier;

(c) a second speaker load connected between an output terminal of the first push-pull output circuit and an output terminal of the second push-pull output circuit of the second BTL amplifier;

(d) the first push-pull output circuit of each of the first and second BTL amplifiers including a first output transistor connected between a power source and the output terminal thereof;

(e) the second push-pull output circuit of each of the first and second BTL amplifiers including a second output transistor connected between the power source and the output terminal thereof;

(f) first and second detectors respectively associated with the first and second output transistors, the first and second detectors detecting the respective operating states of said transistors; and

(g) a control circuit having its input connected to receive the outputs of the first and second detectors of each of the first and second BTL amplifiers, the output of the control circuit rendering non-conductive both of the first and second output transistors of both the first and second BTL amplifiers in the case where at least one of the first or second output transistors of the first or second BTL amplifier deviates from a predetermined operating range.

The present invention will now be described in greater detail by way of examples with reference to the

accompanying drawings, wherein:-

Figure 1 is a block diagram showing a first preferred form of a two-signal amplifying system;

Figure 2 is a circuit diagram showing a BTL amplifier which constitutes the two-signal amplifying system shown in Figure 1 for amplifying one channel; and

Figure 3 is a block diagram showing a second preferred form of a two-signal amplifying system.

Referring first to Figure 1, first and second input signals IN_L and IN_R, i.e. stereophonic left and right signals are fed to the input terminal P_1 of a first BTL amplifier AMP_L and the input terminal P_1 of a second BTL amplifier AMP_R, respectively.

The circuit construction of the first BTL amplifier AMP_L is identical to that of the second BTL amplifier AMP_R. The first BTL amplifier AMP_L includes a phase splitter 3 responding to the first input signal IN_L for separating the non-inverting and inverting output signals (+) and (-) which are in phase with and in phase opposition to the first input signal, respectively. The non-inverting output signal (+) is amplified by a first push-pull output circuit 1 of the first BTL amplifier AMP_L and is fed to a first output terminal P_7, whereas the inverting output signal (-) is amplified by

a second push-pull output circuit 1' of the first BTL amplifier AMP_L and is fed to a second output terminal P_7'. On the other hand, the second BTL amplifier AMP_R also includes a phase splitter 3 responding to the second input signal IN_R for separating the non-inverting and inverting output signals (+) and (-) which are in phase with and in phase opposition to the second input signal, respectively. The non-inverting output signal (+) is amplified by a first push-pull output circuit 1 of the second BTL amplifier AMP_R and is fed to a first output terminal P_7, whereas the inverting output signal (-) is amplified by a second push-pull output circuit 1' of the second BTL amplifier AMP_R and is fed to a second output terminal P_7'.

The first push-pull output circuit 1 of each of the first and second BTL amplifiers AMP_L and AMP_R is equipped, as shown in Figure 2, with a first output transistor Q_{10}, which is connected between a power source V_{CC} and the first output terminal P_7, and a second output transistor Q_{12} which is connected between the first output terminal P_7 and an earth point GND. The second push-pull output circuit 1' of each of the first and second BTL amplifiers AMP_L and AMP_R is likewise equipped, as shown in Figure 2, with a first output

transistor Q_{10}', which is connected between the power source V_{CC} and the second output terminal P_7', and a second output transistor Q_{12}' which is connected between the second output terminal P_7' and the earth point GND.

A first detector 7 is associated with each of the output transistors Q_{10} of the first push-pull circuits 1 of the first and second BTL amplifiers AMP_L and AMP_R. The first detector 7 is provided for detecting the operating states of those transistors. A second detector 7' is associated with each of the output transistors Q_{10} of the second push-pull output circuits 2 of the first and second BTL amplifiers AMP_L and AMP_R. The second detector 7' is likewise provided for detecting the operating states of those transistors.

In both the first BTL amplifier AMP_L and the second BTL amplifier AMP_R, the output of the first detector 7 and the output of the second detector 7' are connected to the input of a switch circuit 8. The output of the switch circuit 8 of the first BTL amplifier AMP_L is fed to an external terminal P_5 of a first semiconductor integrated circuit IC_L whereas the output of the switch circuit 8 of the second BTL amplifier AMP_R is fed to an external terminal P_5 of a second semiconductor integrated circuit IC_R. The external

terminal P_5 of the first semiconductor integrated circuit IC_L and the external terminal P_5 of the second semiconductor integrated circuit IC_R are electrically connected outside the two integrated circuits.

In the first BTL amplifier AMP_L and the second BTL amplifier AMP_R, the output of the switch circuit 8 is connected to the input of a control circuit 9. Since this control circuit 9 is made to respond to the output signals of the first and second detectors 7 and 7' of each of the first and second BTL amplifiers AMP_L and AMP_R, all of the output transistors Q_{10} and Q_{10}' of the first and second push-pull output circuits 1 and 1' of the first and second BTL amplifiers AMP_L and AMP_R are controlled into their non-conductive states in the case where at least one of the output transistors Q_{10} or Q_{10}' of the first or second push-pull output circuit 1 or 1' of the first or second BTL amplifier AMP_L or AMP_R deviates from a predetermined operating region.

The deviations of the output transistors Q_{10} and Q_{10}' from the predetermined operating region result not only from a short-circuit occurring between both the terminals of loud-speakers SP_L or SP_R constituting loads and connected between the output terminals P_7 and P_7' of the first and second push-pull output circuits 1 and 1' in the

first or second BTL amplifier AMP_L or AMP_R, but also from a short-circuit to earth of either the first or second output terminal P_7 or P_7' or a short-circuit between channels.

The control circuit 9 controls the output transistors into their non-conductive states in the above manner in the case where at least one of the output transistors Q_{10} or Q_{10}' of the first or second push-pull output circuit 1 or 1' of the first or second BTL amplifier AMP_L or AMP_R deviates from a predetermined operating range due to an abnormal condition in the state of the load of at least one of the first or second output terminal P_7 or P_7' of the first or second BTL amplifier AMP_L or AMP_R.

The switch circuit 8 is of an automatic return type so that it controls the input to the control circuit 9 in a manner to interrupt the non-conduction of the output transistors of the control circuit 9 when an abnormal condition of the state of the load is eliminated.

Figure 2 is a detailed circuit diagram showing the circuit construction of either the first or second BTL amplifier AMP_L or AMP_R. The circuit defined by broken lines IC_L (or IC_R) is manufactured as a semiconductor integrated circuit.

The phase splitter 3 is constructed in the form of

a differential amplifier for generating the non-inverting and inverting output signals (+) and (-) in opposite phase in response to the input signal IN_L (or IN_R) fed from the external terminal P_1 of the IC so that it may be amplified.

The non-inverting output signal (+) of the phase splitter 3 is applied to a pre-amplifier 4, the output of which is applied to a class A voltage amplifier constructed of transistors Q_6 and Q_7 connected in Darlington configuration and a constant current load transistor Q_4 connected to the commoned collector electrodes of the transistors Q_6 and Q_7.

The output signal from the collector electrode of the transistor Q_7 is applied to the base electrode of a PNP transistor Q_{11}, which operates to drive the output transistor Q_{12} for generating a negative half-wave output of a class B push-pull output circuit, through a resistor R_5 for preventing oscillations. The half-wave output can be generated by driving the output transistor with the collector output signal of that drive transistor Q_{11}.

The emitter electrode of the drive transistor Q_{11} is supplied with the voltage at the output treminal P_7 through the emitter-base path of a transistor Q_{13} and a

a constant voltage circuit consisting of a transistor Q_{14}, a resistor R_9 connected between the base and emitter of the transistor Q_{14}, and diodes Q_{16} and Q_{30} connected in base and collector circuits of the transistor Q_{14}.

The collector output signal of the amplifying transistor Q_7 is also applied through a biasing diode Q_{15} and a transistor Q_8 to the base electrode of a PNP transistor Q_9 which operates to drive the output transistor Q_{10} for generating the positive half-wave output of the class B push-pull output circuit. The collector output signal of the transistor Q_7 is inverted once by the transistor Q_8 and then again by the drive transistor Q_9 so that the above referred positive half-wave output can be generated by the output transistor Q_{10}.

The reason why a PNP transistor is used as the drive transistor Q_9 for driving the output transistor Q_{10} for generating the positive half-wave output is to effect symmetry with respect to the negative side of the circuit and to reduce the remaining positive side voltage to a level $(V_{BEQ_{10}} + V_{CEsatQ_9})$.

Resistors R_6 and R_7 are connected in the respective emitter and collector circuits of the phase inverting transistor Q_8 which is located in front of the drive

transistor Q_9, and a level shifting diode Q_{29} is connected between the emitter electrode of the transistor Q_8 and the base electrode of the output transistor Q_{10}.

The above referred to constant voltage circuit and the transistor Q_{13} are supplied with a bias current from a constant current transistor Q_5.

Consequently, for the input signal IN_L (or IN_R), an output signal OUT in phase therewith is generated from the first output terminal P_7.

The inverting output (-) of the phase splitter 3 generates an output signal OUT' in opposite phase from the output terminal P_7' in response to the input signal with the aid of a pre-amplifier 4' of identical construction to the pre-amplifier 4, a class A voltage amplifier and a class B push-pull output circuit 1', thus constituting the BTL amplifier, in which the speaker load SP_L (SP_R) is connected between the first and second output terminals P_7 and P_7'.

External terminals P_2 and P_2', which are connected to the inverting input (-) of the pre-amplifiers 4 and 4', are used to provide a negative feedback circuit (although not shown) for setting an AC gain between the first and second output terminals P_7 and P_7'.

The BTL amplifier AMP_L or AMP_R also includes a

stabilizing power source circuit which constitutes a constant voltage source circuit having a high power source ripple eliminating coefficient with the use of a constant voltage element such as a zener diode thereby to feed the phase splitter 3 and the pre-amplifiers 4 and 4' with a stabilized voltage. This stabilized voltage is also fed to the constant voltage generating circuit which consists of a resistor R_1 and a diode-connected transistor Q_1.

The constant voltage, which is generated at the base electrode of the transistor Q_1, is applied to the base electrodes of the transistors Q_2 and Q_2' in order to generate a constant current which is predetermined by the ratio between resistors R_2, R_3 and R_3' connected in the emitter circuits of the respective transistors Q_1, Q_2 and Q_2'. The constant current thus generated flows through transistors Q_3 and Q_3' which constitute a current mirror circuit together with the constant current transistors Q_4 and Q_5.

In the embodiment being described, the following circuit is used as the ASO type protecting circuit for the BTL amplifier having the construction so far described.

The detector 7 for detecting the operating state of the transistor Q_{10} is connected to the collector electrode

of the transistor Q_{10} for generating the positive half-wave output. The detector 7 is provided with a resistor R_{11} for detecting the collector current, and with voltage dividing resistors R_{12} and R_{13} connected between the collector and emitter electrodes of the transistor Q_{10} for detecting the collector-emitter voltage. The resistors R_{11}, R_{12} and R_{13} detect the current and voltage of the output transistor Q_{10} so that the detected output is applied to the emitter electrode of a PNP transistor Q_{19}. The collector electrode of the transistor Q_{19} is connected to the earth terminal Pa through a resistor R_{14} and a constant current circuit I_0 and is also connected to the base electrode of a transistor Q_{20}. The power source voltage V_{CC} is applied to the emitter electrode of the transistor Q_{20}, from the collector electrode of which the ASO detected output is generated.

In the ASO type detector 7 thus constructed, if the values of the resistors R_{11} and R_{13} are preset to have a relationship of $R_{11} \ll R_{13}$, the voltage $V_{BEQ_{20}}$ to be applied between the base and emitter electrodes of the transistor Q_{20} can be calculated by the following equation (1):

$$V_{BEQ_{20}} = R_{11}I_{CQ_{10}} + \frac{R_{12}}{R_{13}} V_{CEQ_{10}} + I_0(R_{12} - R_{14}) + V_{BEQ_{19}} \quad \text{----- (1)}$$

In the circuit of the detector 7, the effect of a pair of diodes Q_{17} and Q_{18} connected in series with the resistor R_{13} have been neglected because they are provided for temperature compensation.

In the detector 7, by taking the transistors Q_{19} and Q_{20} into a pair, it is when $V_{BEQ_{20}} - V_{BEQ_{19}} > 0$ that the transistor Q_{21} of the detector 7 becomes conductive. Therefore, the ASO detection level can be deduced from the following inequality (2):

$$R_{11}I_{CQ_{10}} + \frac{R_{12}}{R_{13}} V_{CEQ_{10}} + I_0(R_{12} - R_{14}) > 0 \quad \text{- - - -(2)}$$

The inequality (2) can be transformed into the following inequality (3):

$$I_{CQ_{10}} > \frac{R_{14} - R_{12}}{R_{11}} I_0 - \frac{R_{12}}{R_{11}R_{13}} V_{CEQ_{10}} \quad \text{- - - - - -(3)}$$

On the other hand, if the relationships of $I_0 = \frac{V_{CC}}{R_{13}}$ and $R_{14} = 2R_{12}$ are set, the inequality (3) can be simplified into the following inequality (4):

$$I_{CQ_{10}} > \frac{R_{12}}{R_{11}R_{13}}(V_{CC} - V_{CEQ_{10}}) \quad \text{- - - - - - - - - -(4)}$$

As has been mentioned above, the ASO type detector 7 can effect a highly accurate ASO detection because the ASO detection level can be preset only by the resistance ratio 8 between the resistors R_{11}, R_{12} and R_{13} independently of the base-emitter voltage V_{BE} of the detecting transistors Q_{19} and Q_{20}. Moreover, since a highly accurate resistance ratio can be attained in the monolithic IC, the embodiment is suitable for monolithic circuit integration.

As will be apparent from the inequality (4), the ASO detection output, at which the transistor Q_{21} is turned on, is generated when the relationship between the collector current $I_{CQ_{10}}$ of the output transistor Q_{10} and the collector-emitter voltage $V_{CE_{10}}$ exceeds the straight line joining the point (0(V), $\frac{R_{12}}{R_{11}R_{13}} V_{CC}$(A)) and the point (V_{CC}(V), 0(A)).

As to the operating locus of the output transistor Q_{10} in its steady operation, even if the linearity of the current amplification factor is infinite and if the saturation current is zero, the collector current and the collector-emitter voltage for a load resistance R_L in the case of the BTL amplifier of the OCL type never exceed theoretically the straight line joining the point (0(V), V_{CC}/R_L(A)) and the point (V_{CC}(V), 0(A)).

Therefore, if the minimum of the load resistance R_L is denoted at R_{Lmin}, the erroneous operation that the ASO detection output is generated in the steady operation ($R_L > R_{Lmin}$) is not caused if the design is made to satisfy the relationship of $\frac{R_{12}}{R_{11}R_{13}} > \frac{1}{R_{Lmin}}$.

The ASO detector 7' is identically constructed as the detector 7 is located in the class B push-pull output circuit 1' which operates to generate the outer output OUT_2.

The collector detection output of the transistor Q_{20} is applied to the transistors Q_{21} and Q_{21}' having their respective collector and emitter electrode commonly connected so that the discharge of a capacitor C, which is connected through an external terminal P_4, is controlled by a transistor Q_{22} of the retention circuit 8, which is connected in Darlington configuration with the transistors Q_{21} and Q_{21}'.

The switch circuit 8 is constructed by connecting resistors R_{15} and R_{15}' having a high value of resistance between the first and second output terminals P_7 and P_7' and the power source voltage V_{CC}, by connecting the first and second output terminals P_7 and P_7' across resistors R_{16} and R_{16}' having a high value of resistance

and by feeding a charging current to the capacitor C through a resistor R_{18} having a high value of resistance.

The charging voltage of the capacitor C of the switch circuit 8 is applied to a first transistor Q_{23} forming a differential pair of transistors Q_{23} and Q_{24} which have their commonly connected emitter electrodes connected to a resistor R_{21}. To the collector electrode of the first transistor Q_{23}, there is connected firstly the base electrode of the second transistor Q_{24} and a load resistor R_{22}. To the collector electrode of the second transistor Q_{24}, there is connected an output transistor Q_{25}, which together with the differential pair constitutes a Schmidt trigger circuit.

The output of the Schmidt trigger circuit is divided by resistors R_{23} and R_{24} so that the divided voltage is applied to the transistor Q_{27} of the control circuit 9, which operates to render the transistors Q_1 and Q_2 (or Q_2') non-conductive for generating the above referred to constant current.

The output of the Schmidt trigger circuit is also applied to the external terminal P_5 on the outside of the monolithic IC.

In the control circuit 9, a transistor Q_{28} is connected in series with the transistor Q_{27}. A zener

diode Z_1 and a resistor R_{25} are connected in series between the base electrode of the transistor Q_{28} and the power source voltage V_{CC}. The transistor Q_{28} and the zener diode Z_1 are used to prohibit the operation of the control circuit 9 because the protecting operation of the output transistor is not required in the case where the power source voltage V_{CC} is preset at a lower level than the base-emitter voltage V_{BE} of the transistor Q_{28} and the zener voltage V_z. On the other hand, the zener voltage is used to feed a stabilizing voltage to the Schmidt trigger circuit through a transistor Q_{26}.

In each of the BTL amplifiers in the case where a current or voltage exceeding the ASO operation level is applied to the output transistor Q_{10} or Q_{10}' for generating the positive half-wave output of the output OUT or OUT' (i.e., in the case where the output transistor Q_{10} or Q_{10}' deviates from its predetermined operating range), the transistor Q_{22} is rendered conductive through the transistor Q_{21} or Q_{21}' so that the capacitor C is discharged to invert the Schmidt trigger circuit. The output of the Schmidt trigger renders the transistor Q_{27} conductive which in turn renders the transistors Q_2 and Q_2' non-conductive. As a result, the constant current transistors Q_4 and Q_5 are rendered non-conductive.

As a result, since no base current is fed to the transistors Q_8, Q_9 and Q_{10} of the class B push-pull output circuit 1 by the non-conduction of the transistor Q_4, these transistors can be rendered non-conductive. Moreover, since no base current is supplied to the transistors Q_{11} and Q_{12} of the class B push-pull output circuit 1 by the non-conduction of the transistor Q_5, these transistors can also be rendered non-conductive. At the same time, the transistors Q_8, Q_9, Q_{10}, Q_{11} and Q_{12} of the class B push-pull output circuits 1 and 1' of the second BTL amplifier AMP_R are likewise rendered non-conductive.

Since no charging current flows to charge the capacitor C whilst a short-circuit to earth continues in the case when the requirement for effecting the aforementioned ASO protecting operation is caused by a short-circuit to earth at the output terminals P_7 and P_7', the Schmidt trigger circuit is left inverted so that the bias current of the output circuit 1 is still interrupted by the conduction of the transistor Q_{27} to thereby continue the protecting operation.

When the short-circuit to earth is removed, the capacitor C is charged through the resistors R_{15}, R_{15}', R_{16} and R_{16}'. If the voltage for returning the Schmidt trigger circuit is reached, the transistor Q_{27} is rendered non-conductive to again feed the bias current of the output circuit 1 so that the amplification is automatically started.

In the case of a short-circuit occurring between the output terminals of the other channel, the output terminals P_5 of the switch circuits 8 of the respective BTL amplifiers IC_L and IC_R of the stereophonic amplifying system consisting of similar BTL amplifiers IC_L and IC_R, are connected, as shown in Figure 1. As a result, in the case where a short-circuit occurs between the output terminals of the other channel, this short-circuit is detected by either one of the ASO detectors 7 and 7' to thereby invert the switch circuits 8, the outputs of which operate the transistors for blocking the biasing current of the other BTL amplifier, thus rendering all of the output transistors non-conductive. Thus, the protecting operation can be performed even for the short-circuits occurring between the two channels.

In the case of a short-circuit occurring between the outputs of the two channels, the output terminals P_7 and P_7' of the BTL amplifiers IC_L and IC_R are not earthed. As a result, the capacitor C is charged through the resistors R_{16}, R_{16}' and R_{18} so that the Schmidt trigger circuit automatically restores its operation. If, at this time, the short-circuit between the two channels continues the operation of discharging the capacitor C, inverting the Schmidt trigger circuit and blocking the biasing current are repeated at the time when the ASO detection level is exceeded. As a result, in the case where short-circuit conditions

between channels arise, the intermittent amplifying operations are repeated in accordance with the hysteresis voltage of the Schmidt trigger circuit and with a time constant determined by the value of capacitance and resistance of the capacitor C, and the resistor R_{18} respectively.

The intermittent operations of the stereophonic amplifying system and the interruptions of the outputs of the two channels can be used as an indication of the abnormal condition of the stereophonic amplifying system in order to warn the user of the need to check the wiring between the respective output terminals P_7 and P_7' of the two BTL amplifiers IC_L and IC_R to the respective loudspeakers SP_L and SP_R.

Since the ASO detectors are associated with only the output transistors for generating the positive half-wave outputs, the protecting circuits for controlling the biasing currents can be made common in order to simplify the construction of the circuit and to effect the protecting operations through the interruption of the biasing currents. As a result, no oscillation takes place.

Moreover, the ASO detectors may also be connected with the output transistors for generating the negative half-wave outputs.

Furthermore, in the case where the stereophonic amplifying system is constructed of an IC having two chips, it is sufficient to merely add one external terminal for supplying the ASO direction output. As a

result, it becomes possible to minimize the number of the external terminals to be added and to ensure the protecting operations for all the possible short-circuit conditions of the output terminals.

The above described protection system can be so modified that it is constructed of two BTL amplifiers having one chip IC, as shown in Figure 3. In this modification, the switch circuit 8 which includes the Schmidt trigger circuit, is shared between the two BTL amplifiers thereby reducing the number of external terminals thus simplifying the circuit construction.

In an alternative, a latch circuit may be operated by the ASO detection output thereby controlling the biasing current.

In this modification, although the capacitor C and the resistor R_{18} can be omitted, it is necessary to interrupt the power source in order to release the protecting operation so that the circuit can be returned to normal.

CLAIMS.

1. A two-signal amplifying system having:

(a) a first BTL amplifier for amplifying a first input signal and a second BTL amplifier for amplifying a second input signal; said first BTL amplifier including a first push-pull output circuit for delivering a non-inverting output signal of the first input signal, and a second push-pull output circuit for delivering an inverting output signal of the first input signal; said second BTL amplifier including a first push-pull output circuit for delivering a non-inverting output signal of the second input signal, and a second push-pull output circuit for delivering an inverting output signal of the second input signal;

(b) a first speaker load connected between an output terminal of the first push-pull output circuit and an output terminal of the second push-pull output circuit of the first BTL amplifier;

(c) a second speaker load connected between an output terminal of the first push-pull output circuit and an output terminal of the second push-pull output circuit of the second BTL amplifier;

(d) the first push-pull output circuit of each of the first and second BTL amplifiers including a first output transistor connected between a power source and the output terminal thereof;

(e) the second push-pull output circuit of each of the first and second BTL amplifiers including a second output transistor connected between the power source

and the output terminal thereof;

(f) first and second detectors respectively associated with the first and second output transistors, the first and second detectors detecting the respective operating states of said transistors; and

(g) a control circuit having its input connected to receive the outputs of the first and second detectors of each of the first and second BTL amplifiers, the output of the control circuit rendering non-conductive both of the first and second output transistors of both the first and second BTL amplifiers in the case where at least one of the first or second output transistors of the first or second BTL amplifier deviates from a predetermined operating range.

2. A two-signal amplifying system according to Claim 1, wherein the first and second input signals are stereophonic left and right signals.

3. A two-signal amplifying system according to Claim 2, wherein the outputs of the first and second detectors are fed through a switch circuit to the input of said control circuit.

4. A two-signal amplifying system according to Claim 3, wherein the first and second BTL amplifiers are manufactured on first and second semiconductor integrated circuits respectively.

5. A two-signal amplifying system according to Claim 4, wherein both the outputs of the two switch circuits, which are arranged in the first and second BTL amplifiers are connected to external terminals on respective semiconductor integrated circuits, both of said two external terminals being electrically connected in order to electrically connect together both the inputs of the respective control circuits which are arranged in the first and second BTL amplifiers.

6. A two-signal amplifying system according to any of the preceding claims, wherein the first and second detectors detect the collector current and the collector-emitter voltage of the first and second output transistors respectively.

7. A two-signal amplifying system according to any one of the preceding claims 1 to 4, wherein the first push-pull output circuit of each of the first and second BTL amplifiers includes a third output transistor connected between the first output terminal thereof and earth, and wherein the second push-pull output circuit of each of the first and second BTL amplifiers includes a fourth output transistor connected between the second output terminal thereof and earth, the output of said control circuit likewise rendering the third and fourth transistors non-conductive in the case where at least one of the first or second output transistors of the first or second BTL amplifier deviates from a predetermined operating range.

8. An amplifying system according to any one of the preceding claims, wherein said two signals are stereophonic left and right channel signals, said first and second BTL amplifiers are left and right channel amplifiers respectively, and said first and second speaker loads are left and right channel loud-speakers respectively.

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9. A stereophonic amplifying system constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 1 and 2 or Figure 3 of the accompanying drawings.

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