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A method for testing an integrated circuitry and an integrated circuit having a plurality of functional components and having junction/switch test components in interconnecting channels between functional components.

FIELD OF THE INVENTION

The invention relates to a method for testing electronic circuitry with a plurality of functional components interconnected by handshake channels. Testability of integrated circuits has been approached in various ways, inter alia as dependent on circuit technology, fault model, and test provisions that may be present or absent, physically as well as notionally. Earlier provisions include scan test or LSSD, boundary scan test, both of these approaching the circuit as a single black box. US Patent 4,656,592 to the same assignee teaches the breaking up of complicated circuits into partial circuits that maintain mutual synchronization through a handshaking procedure. This would allow for blockwise testing in such quite specific environment wherein the partial circuits operate synchronously and only the interaction between the various circuits is executed via handshakes. During development of the present invention it has occurred that widespread use of handshaking functional components is a preferred method to keep development of asynchronous circuitry manageable. Given such asynchronous realization, test generation remains a problem that more or less explodes exponentially with the size of the circuit, causing rather simple circuits to need an astronomical number of test patterns and/or test time. The present invention presents a solution in that it envisages breaking-into and breaking-out from the channels. In particular, a channel is herein understood to be a point-to-point connection that has an active port on its first end, and a passive port on its second end. The active/passive notion relates to activities on the communication protocol level, and not on the data transfer direction. This means that data may go from the passive port side to the active port side. By itself, no data transfer need even occur, if the only object of the communication is, e.g. synchronization.

SUMMARY TO THE INVENTION

Amongst other things, it is an object of the present invention to provide

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an infrastructure for structural testing of handshake circuits at a low level of organizational complexity. According to the present environment a handshake circuit is a network of asynchronous circuit blocks that exhibit mutual synchronization and may exchange information.

According to one of its aspects, the invention provides a solution as a method for testing electronic circuitry having a plurality of functional components interconnected by handshake communication channels channels each channel terminating at respective functional components by an active port from which a communication is initiated and a passive port where such communication is awaited, respectively, said method comprising providing one of said channels with an inbreaking junction thereby forming a first test component that at other times than testing just forms part of the in-channel handshaking, said method comprising breaking in via a passive port of said junction with a first test signalization as an alternative to any in-channel signalization towards the in-channel passive port of said junction, said first test signalization representing the test signalization for said channel in a test on any component with a passive port on said channel and inclusive of any channel part between said any component and said test component. The design-for-testability may be embedded in a silicon compilation organization as per US Patent 5,005,136, issued April 2, 1991 to the same assignee that is referred to in particular for corresponding terminology. It has been found that inbreaking via a junction would even in the absence of any data transfer, by means of a synchronization signal returned, allow for executing a test. If the synchronization is not returned, this could signal a failed test. It should be noted that the present invention would not necessarily comprise the sequence: provide test pattern, execute test, extract result pattern. Presentation of a test pattern may or may not result in a returned synchronization signal. A result pattern may emanate from executing a test by means of a test pattern that had been stored earlier. The test may be a self-test, wherein control is temporarily effected locally without external intervention.

More comprehensively, the invention provides a method for testing electronic circuitry having a plurality of functional components interconnected by handshake communication channels each terminating at respective functional components by an active port from which a communication is initiated and a passive port where such communication is awaited, respectively, said method comprising

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providing one or more of said channels with an inbreaking junction and/or one or more of said channels with an outbreaking switch thereby forming a set of test components that at other times than testing just form part of the in-channel handshaking, said method comprising breaking in via a passive port of a first channel's junction with a first test signalization as an alternative to any in-channel signalization towards the in-channel passive port of said junction, under control of an external control signal to a control port of a switch on a second channel breaking out therefrom a second test signalization via an active extra-channel port thereof as an alternative to any further in-channel signalization via any active further port of said second channel's switch, said first c.q. second test signalization being the test signalization for said first c.q. second channel in a test on any component with a passive port on said first channel c.q. with with an active port on said second channel, and inclusive of any channel part between said components and said test components. Generally, a complicated circuit will need a plurality of junctions and a plurality of switches. In certain circumstances, one category of the two could be absent; like the junction, a switch could work in isolation: in case of a test, internal control could produce or not produce the result data at the switch's output.

The present invention allows to make the problem simpler by allowing it to be broken down into parts: insertion of such inbreaking and outbreaking facilities leads to a smaller depth of the state diagrams with respect to testing. It should be noted that both said first and said second test signalizations may comprise respective composite signals and/or multibit patterns, and moreover, neither of them need to contain data inasmuch as either one may comprise only communication primitive signals. It should be noted that US Patent 4,656,592 does not teach any specifics as to how the test would effectively be executed on the level of the synchronization primitives.

Advantageously, the method comprises providing at least one channel with a switch that in its test signalization is controlled both in test mode for breaking out of in-channel signalizations within said at least one channel as well as in non-test mode for continuing in-channel signalizations. This under non-test situations would allow for standard functionality. Advantageously, the method comprises providing at least one channel with both a junction and a switch as a test component pair thereby

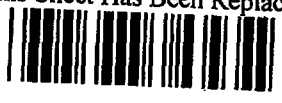
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allowing both inbreaking and outbreaking test facilities for said said at least one channel. Contiguous junction and switch now constitute a concrete or physical test component pair. By having the span of such concrete test component pairs overlapping each other, any part of the channel now covered by such overlapping is rendered testable. In particular, apart from wires, the channel may comprise such elements as buffers or invertors, that are now also rendered testable. The methodology deployed can be applied on various levels, such as on the board level, within a single chip, as well as on-chip between blocks of various levels of complexity. Moreover, it can be used as a partial approach, such as for specifically testing those parts of the circuits that are difficult to control or to observe otherwise.

Advantageously, the invention provides a method for executing a plurality of tests on respective functional components by presenting to said circuitry an aggregate test signal including aggregate control signals, extracting therefrom first test signalization for inbreaking onto various junctions and also respective external control signals for presentation to various switches and also respective second test signalizations for breaking out from various switches. This allows for an external access either at a narrower path width or at a lower amount of data transfer. The organization for a proper ordering, extraction, aggregation of the various test and control signals may be obtained from the organizational structures that are available for handshake circuits, such as for (de)multiplexing, parallel composition, and sequential composition structures as disclosed in US patent 5,005,136. Additionally, translating tables, hashing technology and signature generation could be used in various instances. The provision of various junctions and switches in the circuitry's communication channels is a direct hardware mirroring of the design for testability and the test method itself. Moreover, the provision of respective test components can be used in a self-test organization. Self-test is herein defined in that an aggregate test signal provided from outside is used in conjunction with various in-circuitry prepresented or prestored test signalizations, whether explicit or implicit, to execute a plurality of elementary test operations, after which a plurality of elementary test results are joined, signatured, or otherwise evaluated to signal an overall test evaluation outside the circuitry tested. By itself, such self-test principle with respect to a static RAM memory has been described in US Serial 752,166 , EP published specification 350,538, to the assignee of the present application,

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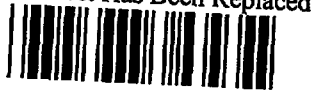


herein incorporated by reference.

It is particularly advantageous of the invention, for testing said electronic circuitry having a plurality of integrated circuits, by assigning to any channel crossing any border between separate integrated circuits a dummy functional component at said border for so at either side of said border creating a separate channel as a respective one of said handshake channels. If the circuitry consists of more than one separate integrated circuit, it is not known in advance what the "neighbour" circuit would be. It could have the test provisions according to the invention, or not. And even in the positive case the two channels could have somewhat different protocols on a level that would interfere with the testing, although this would not be the case for standard handshaking. In particular, the latter provision would allow to execute a boundary or interconnection test, as an alternative approach to the boundary scan test standard according to JTAG, now IEEE 1149.1. On another level, the present invention can be used for test features according to self-test principles at various levels of complexity.

According to an advantageous aspect, an integrated handshake circuit for being testable according to the present invention, comprises a plurality of testable functional components that are interconnected by handshake communication channels each terminating at respective functional components by an active communication initiating port and a passive communication awaiting port, respectively, and at least part of said channels being provided with an inbreaking junction or an outbreaking switch, thereby forming a set of test components that at other times than testing just form part of the in-channel handshaking, any said junctions having a first passive channel port for in-channel initiated communications and a second passive test port for externally initiated test communications, and a first active channel port for propagating both said types of initiated communications, any said switch having a third passive channel port for in-channel initiated communications, a second active channel port for in-channel propagation of these initiated communications and in each one of at least part of said switches a combination of a third active test port for extra-channel propagation of these initiated communications and a fourth passive control port for selecting for propagation between said second active channel port and said third active test port, said circuit furthermore having test control means for breaking in onto any said second passive test port with said externally initiated test pattern. The testable components may be rendered

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electronic part in common with some channelwise contiguous functional component. Such set-up would diminish the amount of extra hardware needed. Apart from such communality with a functional component, a contiguous junction/switch pair, in particular a concrete test component pair, may have certain electronic parts in common for thereby reducing hardware overhead.

Advantageously, the circuit according to the invention comprises acknowledge means in at least one functional component for upon completion of a prespecified test thereon outputting an acknowledge signal as extraneous to standard channel handshake signals from such functional component. Especially for a repeater functional element to be disclosed hereinafter, such signalization is a time-saving provision. The acknowledge may now be sent on the channels that are provided for the standard functions of the circuit.

Various advantageous aspects are recited in dependent Claims.

DEFINITIONS

For purpose of illustration, the following definitions apply:

- *Handshake circuit*: Graph, with channels as edges and handshake components as nodes, and with an provision for initialization.
- *Handshake component*: Electronic circuit, that interacts with its environment by communicating along intermediary channels. Each communication is organized as a handshake. The initiative to communicate may vary per communication. To illustrate the invention, it suffices to fix initiatives per channel.
- *Channel*: Bidirectional link of wires between a handshake component and its environment. To illustrate the invention, it suffices to regard channels as point-to-point connections, with unidirectional wires. The two terminals of a channel are called ports.
- *Port*: Channel terminal in a handshake component. If the component initiates the communications along the channel, the port is called active. If its environment takes the initiative, the port is called passive.
- *Communication*, or *handshake*: Finite sequence of communication events along a channel, organized as a handshake protocol, i.e. the initiative for the next event alternates between the communicating partners.

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- *Communication event*: Set of transitions along one or more of the wires of a channel, which set is provided with a completion criterion.

As reference model for the soundness and completeness of a test, we use the notion of test obligations. We assume that a correctness criterion for fabricated handshake circuits is available, and that the environment can detect whether or not the circuit halts in an initial state. Testing starts from initialized circuits. Theoretically, it may be impossible to drive a particular, faulty, circuit to its intended initial state, but the subsequent behaviour of the circuit will then even more betray such faultiness. The possibility of a faulty behaviour that is not detected is ignored.

- *Test obligation*: In time partially ordered set of communication events along the channels of the circuit, possibly with an initialization event at the end. Test obligations satisfy the constraint that a correct circuit responds to all events in the test obligation and terminates in an initial state.
- *Test*: Set of test obligations, satisfying the two constraints that every test obligation is passed successfully by a correct circuit, and that an incorrect circuit fails some test obligation, because it cannot respond to some event therein. This implies that by itself, a test is a complete set of stimuli and responses for attaining the object: to know whether or not the fabricated circuit is correct.
- *Test suite*: Set of tests, representing various possibilities to test the circuit.

BRIEF DESCRIPTION OF THE FIGURES

The invention will be described in detail hereinafter, with respect to a preferred embodiment of which various aspects are shown in the appended Figures according to:

Figure 1 shows a testable circuit according to the invention;

Figure 2 shows two functional components interconnected by a channel;

Figure 3 shows addition thereto of a switch and a junction as two test components;

Figure 4 has them interchanged according to the invention;

Figure 5 shows an electronic circuit for a sequencer handshake component;

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Figure 6 lists the consecutive state combinations therein when operating in a correct environment;

Figure 7 shows a full testability arrangement of a slightly more complicated circuit operating as a duplicator;

Figure 8 shows a configuration of testability components suited for boundary or interconnection testing;

Figures 9a..c show various handshake channel organizations;

Figures 10a..d give four basic handshake components as embodiments;

Figure 11 combines two such components to a duplicator;

Figure 12 shows an electronic circuit for a repeater handshake component;

Figure 13 shows an electronic circuit for a single-read, single-write variable handshake component;

Figure 14 shows an optimized version of Figure 4 for use in a preferred embodiment;

Figure 15 likewise shows an optimized version of Figure 7;

Figure 16 shows a full testability arrangement for the single-read, single-write variable;

Figures 17a, b show a partial testability arrangement for a duplicator chain with an exponential reduction in the test time;

Figures 18a..c show a slightly different implementation of a duplicator chain with a linear test time;

Figure 19 shows an efficient implementation for the mode of operation as exemplified by the multiplexer handshake component MIX.

In the disclosure, for brevity, external test machinery, the application of test patterns and any register level implementation, and also any test evaluation are not treated in detail inasmuch as such is considered standard art; only the communication channels and their relation to the testability feature are fully explained, as well as certain electronic subcircuit components that are either feasible or accessory to such testing. Moreover, the disclosure does not go into the transistor and only little into the gate level, inasmuch as these levels of realizing electronic circuitry are deemed common general knowledge.

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BACKGROUND PHILOSOPHY

As for synchronous circuits, the problem of finding tests for arbitrary handshake circuits is a complicated problem: increasing the size of the problem (such as the number of channels) renders the number of solutions (e.g. patterns) exponentially larger. In the synchronous scan test approach, the solution reduces the test complexity by controlling and observing internal points during testing. This involves extra hardware per point, thus affecting the performance. Test costs and performance can be tuned by judiciously choosing the internal points. The resulting circuit has two modes of operation: a standard mode for the original behaviour, and a test mode. The test approach for handshake circuits has some similarities.

Now, because the key to the testing of a handshake circuit is its communication behaviour, controllability and observability relate to channels. Therefore, to test a handshake circuit independently from its environment, an extra interface for testing is created by inserting testability handshake components in the intermediary channels.

First, Figure 1 shows a testable circuit according to the invention. The circuit 100 has four functional components 102..108. For brevity the nature of their functionalities is not discussed as not relating to the invention proper. The functional components operate asynchronously and are interconnected by handshake channels 110..116 that each have an inbreaking junction/outbreaking switch pair that will be discussed more in detail hereinafter. In certain situations, a channel may have only a single test component, either a junction or a switch as is explained hereinafter. In the Figure, the pairs are symbolized by blocks 120..126 that communicate, bidirectionally if required, with test control block 128. Circuit 100 communicates for executing its standard functionality with external circuitry, not shown for brevity, along channels 130, 132. The border between circuit 100 and the external world is symbolized by dummy functional components 142, 144 that do not add further functionality. Now, channels 130, 132, between functional components 106, 108 and their counterpart dummy components have an inbreaking junction/outbreaking switch pair 134, 136 respectively. In the Figure, also external channels 146, 158 have their respective inbreaking junction/outbreaking switch pair 138, 140, that do not communicate with test control block 128. For brevity, their own test control block has not been shown. Test

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control block 128 receives from the external world (test machine) an aggregate test signal. This may imply test initialization, test patterns, intended result patterns, and any further control that is necessary. This control can direct which tests or partial tests should be executed and in what sequence, control the deriving of the test patterns from the overall test signal, the prescription for aggregating the result patterns to an overall result signal, preprocess control of the result patterns, such as comparing with an expected result, and various others.

Now, Figure 2 shows two circuits, A and P interconnected by a channel c. Circuit A is connected to the channel by its active port, shown by a solid dot, circuit P likewise by its passive port, shown by an open dot. Data, if any, may go from left to right or opposite. The active/passive ports undertake a handshake. Note that data may be physically on a separate wire (fibre, frequency, etcetera) parallel to the handshaking channel shown. Alternatively, data itself may carry the handshake protocol. The channel may be interior to one integrated circuit or interconnect two integrated circuits. Of course, any functional component may have an arbitrary number of ports. Figure 3 shows the extra components S (switch) and J (junction) between handshake circuits A, P. Switch S is mode-controlled at its passive control input port external to the channel. Junction J does not need such control. In this set-up, communication actions initiated by circuit A and/or accepted by circuit P can be controlled and observed. Both controlling and observing are done through inbreaking on a first channel with first test signalizations on an inbreaking junction, and outbreaking at a second channel with second test signalizations at an outbreaking switch. Such observing and controling however, by S has only an outbreaking functionality with respect to circuit A, whereas junction J may be omitted from the view-point of circuit A. Likewise, as seen from the view-point of circuit P, switch S may be omitted.

However, a test using the configuration as shown in Figure 2, is not effective for the intermediate channel between switch S and junction J. Therefore, Figure 4 has switch and junction interchanged. Combined they now consitute a test component pair that have their test objects overlapping, as regards channel part c. For a specific channel, the choice between both testability configurations is determined by the fault distribution of the manufacturing process, the desired fault coverage, and the associated ease of testing. In the following, we mainly concentrate on the configuration

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shown in Figure 4. Now, the sequence of lines c^a, c, c^p represents the original channel between the circuits A and P. In this channel, there is a junction 22 that has a passive test port in the channel, a passive test port external to the channel, and an active port in the channel. The communications on the two passive ports are passed through the single active port, and must not overlap. Furthermore, the channel has switch 24 that has a passive port in the channel, an external passive mode control port, an active port in the channel and a second active test port external to the channel. A handshake communication on the channel is passed through one of the two active ports as depending on the mode. In this way all parts of the channel c^a, c, c^p are controllable and observable during testing. The junction allows for initiating communications (breaking in), the switch for intercepting communications (breaking out). If the test events on c_t^a and on c_t^p equal those on c^a and c^p respectively, then c_t^a and c_t^p have the same capabilities of controlling and observing the circuits A and P as c^a and c^p have. Often, weaker relations than equality between the in-channel communications and their test counterparts suffice to obtain these same capabilities.

About test generation, it is noted, that a test which is suitable for a basic component, will also test the same component in a configuration as shown in Figure 4, provided that we replace the channel communications by their test-counterparts and that we set the corresponding switches in test mode before starting. In a configuration like Figure 4, part of this test concerns signals that pass through switches forming part of the environment. These latter switches are therefore controlled in standard mode. This procedure may be refined to apply to the more elementary level of test obligations.

Now, abstracting from the testing of the testability components themselves, the above test procedure easily extends to handshake circuits in general by successively applying it to all basic components in the circuit. In fact, any composition of the local test procedures will do, as long as conflicting modes or communications do not occur simultaneously.

During the test, the testability components alternate between test and standard mode. It is possible to design them in such a way that their role in the testing of handshake circuits is self-diagnostic: through testing the original circuit, the entire organization for testability enhancement is tested automatically.

Figure 5 shows an electronic circuit for a sequencer handshake

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component, cf. the referenced Patent US-5,005,136. It executes the bare handshakes along three channels a(a0,a1), b(b0,b1) and c(c0,c1) that each consist of two physically unidirectional wires as shown. Internally, there are two AND gates 28, 30, each having one inverted input as indicated by an open circle. Finally, a so-called Muller C-element 32 is present. Such element has an output that has been shown twice (w) in the Figure and can have any number of inputs. Its output changes only if all inputs have the opposite value of the current output value; otherwise the output remains unchanged. Figure 6 lists the consecutive stable state combinations when operating in a correct environment: when activated along channel a, it communicates once along channel b0, and subsequently, once along channel c0, respectively.

Figure 7 shows a full arrangement of test provisions for a slightly more complicated circuit. Shown are a sequencer 34 that would correspond to the arrangement of Figure 5, and a mixer 36 that unconditionally directs any communication initiated on either passive port to its sole active port. This Figure illustrates that testability enhancement according to the invention considerably increases the number of external channels. This may be a problem for integrated circuits, with only a couple of dozens external channels. Partial integration of the test procedure can reduce the number of additional external channels to only a few, at the price of extra hardware. Like the testability components, this hardware can have a self-diagnostic role in the testing of the handshake circuit. Complete integration of the test procedures gives the synchronous equivalence of a circuit with a *built-in self test*, where only the external channels at the boundary of the circuit remain to be tested separately. The possibility to have a separate *boundary test* eases the testing of the interface between the circuit and its environment.

Figure 8 gives a possible configuration of junctions and switches along an interconnection channel c between two integrated circuits A and P, for example along channel 130/146 in Figure 1. The path taken during the interconnection test is indicated by the dotted line. Apart from interconnection channel c, no further parts of the two circuits are involved.

In design for testability, test and performance costs can be tuned by taking larger or smaller structures of handshake components as the basic components. Generally, such basic component is a cluster of electronic circuitry not having the

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provisions of Figure 4, supra.

Within the scope of the invention, there are many alternative solutions on the above theme of circuit accommodations for testing. It is often advantageous to use composite structures that combine original handshake components and inbreaking/outbreaking components: the resulting circuit will be smaller and faster than the juxtaposed constituents because intermediate channels are superfluous. Also, combinations with test procedures or elements thereof may significantly reduce the test problem.

PRELIMINARIES TO A PREFERRED EMBODIMENT

- Initializing a handshake circuit corresponds to making all external input wires low and waiting a certain amount of time for the circuit to settle in a stable state that is an initial state for a correctly functioning circuit. The settling time can be calculated from the circuit. So, the environment knows that the circuit is nominally in an initial state when all the external wires stay low for at least as long as the settling time.
- Channels are point-to-point connections, with unidirectional wires. The initiative to communicate is fixed per channel. A synchronization channel a has two wires: a_0 from the active port to the passive port, and a_1 from the passive port to the active port. A data channel has a single synchronization wire, on which data is requested or acknowledged, and a set of wires on which data is communicated. Data communications are unidirectional and in dual rail encoding, i.e. there are two wires per bit b, b0 for -zero- value, and b1 for -one- value, respectively. The schemes for the channel implementations are given in Figures 9a..c.
- The following communication events are distinguished:

  - set synchronization wire w: $w\uparrow$
  - reset synchronization wire w: $w\downarrow$
  - set data d: $b0\uparrow$ or $b1\uparrow$ for all data bits b in the set of data wires d; shorthand notation: $d\uparrow$, or $d\uparrow v$ if v is the data value concerned
  - reset data: $b0\downarrow$ or $b1\downarrow$ for all data bits b in the set of data wires d; shorthand notation: $d\downarrow$, or $d\downarrow v$ if v is the original data value concerned

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The corresponding completion criteria are as expected:

- $w\uparrow$ is complete when $w = 1$
- $w\downarrow$ is complete when $w = 0$
- $d\uparrow$ (d ↑ v) is complete when $b0 = 1$ or $b1 = 1$, but not both equal to 1, for all data bits b in d
- $d\downarrow$ (d ↓ v) is complete when $b0 = 1$ and $b1 = 1$, for all data bits b in d

- A communication is organized as a 4-phase handshake, during which data and synchronization wires are set and reset, respectively:

  $a_0\uparrow; a_1\uparrow; a_0\downarrow; a_1\downarrow$

Herein, a semicolon ';' indicates sequential ordering between signals prespecified and post-specified thereto, respectively. Furthermore, if a is a data channel, then either a_0 is the synchronization wire and a_1 is the collection of data wires, or vice versa (cf. Figure 9).

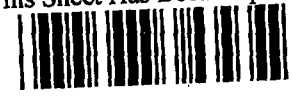
The following programming constructs are used to specify the behaviour at the ports of a handshake circuit in terms of the above events. Let E range over arithmetic expressions, and a over port names. We use superscripts to indicate that the initiative for a sequence of events at a port is internal (.$^\bullet$=active) or external (.$^\circ$=passive):

- a↑$^\circ$ is a shorthand notation for $a_0\uparrow; a_1\uparrow$, and a↓$^\circ$ for $a_0\downarrow; a_1\downarrow$, where the initiative is with the environment. Likewise for a↑$^\circ$?x, a↓$^\circ$?x, a↑$^\circ$!E, and a↓$^\circ$!E.
- a↑$^\bullet$ is a shorthand notation for $a_0\uparrow; a_1\uparrow$, and a↓$^\bullet$ for $a_0\downarrow; a_1\downarrow$, where the initiative is internal. Likewise for a↑$^\bullet$?x, a↓$^\bullet$?x, a↑$^\bullet$!E, and a↓$^\bullet$!E.

There are several ways to compose existing behaviours P_0 and P_1. Here, we use the operators (in decreasing order of priority) '*', ':', ';', ' | ', '□' ' ‖ ', as defined below. As usual, bracket pairs '(.)' and '[.]' are used to escape from priorities and to clarify the syntactic structure.

- Sequential composition $P_0; P_1$: first P_0, and then P_1.
- a$^\circ$ is a shorthand for a↑$^\circ$;a↓$^\circ$, and a$^\circ$?x for a↑$^\circ$?x;a↓$^\circ$?x. Likewise for a$^\circ$?x, a$^\circ$!E, a$^\bullet$, a$^\bullet$?x and a$^\bullet$!E.

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- Infinite repetition $*P_0$: infinitely often P_0
- Parallel composition $P_0 \parallel P_1$ meaning P_0 and P_1 in parallel
- $a\uparrow^\circ$: P_0 denotes $a_0\uparrow$; P_0; $a_1\uparrow$, and $a\downarrow^\circ$: P_0 denotes $a_0\downarrow$; P_0; $a_1\downarrow$, where the initiative for a is external.
- $a\uparrow^\bullet$: P_0 denotes $a_0\uparrow$; $(P_0 \parallel a_1\uparrow)$, where the initiative for a is internal.
- External nondeterminism $P_0 \mid P_1$: either P_0 or P_1, as chosen by the environment
- Internal nondeterminism $E_0 \rightarrow P_0 \,\square\, E_1 \rightarrow P_1$: either P_0 or P_1, depending on the validity of the corresponding boolean expressions E_0 and E_1.

An internal variable x of type T is declared as x: var T. Variable declarations are separated by '&' symbols. A passive port a for data of type T is declared as a°?T for inputs, and as a°!T for outputs. An active port a for data of type T is declared as $a^\bullet$?T for inputs, and as $a^\bullet$!T for outputs. A port a for synchronizations only is declared as a° for passive a, and as $a^\bullet$ if a is active. Port declarations are separated by ',' symbols. Program constructs for the basic handshake components are of the form:

(port declarations). [[variable declarations | P_0]]

or, without internal variable declarations:

(port declarations).P_0

SOME EXAMPLES OF HANDSHAKE COMPONENTS

Figures 10a..d give the icons for four basic handshake components: a sequencer (a), a multiplexer (b), a repeater (c), and a variable (d).

- Sequencer SEQ(a°,$b^\bullet$,$c^\bullet$) in Figure 10a when activated along *a* subsequently communicates along *b* and *c*, respectively. The specification in terms of communication events is:

  SEQ.(a°,$b^\bullet$,$c^\bullet$) =

  (a°,$b^\bullet$,$c^\bullet$).*[$a\uparrow^\circ$:($b^\bullet$;$c\uparrow^\bullet$);$a\downarrow^\circ$:$c\downarrow^\bullet$]

- Multiplexer MIX.(b°,c°,$d^\bullet$) in Figure 10b passes the communications along both *b* and *c* to *d*:

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MIX.(b°,c°,d•) =

(b°,c°,d°). *[b↑°:d↑•; b↓°:d↓•

| c↑°:d↑•; c↓°:d↓•

]

- Repeater REP.(a°,b•) in Figure 10c repeatedly communicates along b, once it is activated along *a*:

REP.(a°,b•) =

(a°,b•).a↑°:*[b•]

- Single-read, single-write, 1-bit variable $VAR_{(1,1)}$.(a°,b°) in Figure 10d, stores the last bit value input along *a* and sends it on request along *b*:

$VAR_{(1,1)}$.(a°,b°) =

(a°!1, b°?1)

[[x: var 1

| *[a°?x | b°!x]

]]

Figure 11 combines a sequencer and a multiplexer to a duplicator. For each communication along *a*, it initiates two communications along *d*.

SELECTED TEST MODEL

As for synchronous circuits, the correctness criterion for fabricated circuits is based on a fault model. In the fault models for handshake circuits, faults are related to erroneous communications, such as the inability to transmit certain values or to complete a communication (deadlock). In the following we concentrate on deadlocks. For a 4-phase handshake with dual rail data transmission, a deadlock corresponds to the inability to set or reset some channel wire. Deadlocks also cover faults in internal wires which can be illustrated at the hand of Figure 5. The intended behaviour is:

*[a_0↑°; b_0↑•; b_1↑°; w↑; b_0↓•; b_1↓°; c_0↑•;c_1↑°; a_1↑•; a_0↓°; w↓; c_0↓•; c_1↓°; a_1↓•] cf. SEQ(a°,b•,c•).

Both the setting and the resetting of internal channel *w* are followed by some external event: w ↑ by b_0↓, and w ↓ by c_0↓. If either of the internal events is disabled, e.g. as a result of a stuck-at fault on w, then so is the external event a_1↓, thus causing a deadlock on channel *a*.

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Figure 12 shows a concrete circuit for the basic component REP.(a°,b•), also from U.S. Patent Application 5,005,136. It illustrates what was already expressed earlier: the absence of event $a_1\uparrow$, and the necessity of initialization to end the computation and to test $a_0\downarrow$.

Figure 13 gives a concrete circuit for the basic component $VAR_{(1,1)}$.(a°,b°), according to Netherlands Patent Application 9000544, corresponding US Serial 659,805, herein incorporated by reference. By storing the value 0 into the variable and then reading it, the wires a_00, a_1, b_0 and b_10 are tested for stuck-at-0/1 faults, wire q0 is tested for stuck-at-1, and q1 is tested for stuck-at-0. Storing the value 1 and then reading it, tests the wires a_01, b_11 for stuck-at-0/1 faults, q0 for stuck-at-0, and q1 for stuck-at-1. A complete test is thus obtained by executing both in sequence. As a result of the dual-rail encoding, it is not necessary to check the received value against the stored value. Given the above test model, the following tests are suited for testing the basic components in Figure 10:

- The test suite for SEQ.(a°,b•,c•) contains a single test with a single test obligation, specified by:
  $a\uparrow^{\bullet}:(b^{\circ};c\uparrow^{\circ})$; $a\downarrow^{\bullet}:c\downarrow^{\circ}$
- The test suite for MIX.(b°,c°,d•) contains a single test with two test obligations:
  $b\uparrow^{\bullet}:d\uparrow^{\circ}$; $b\downarrow^{\bullet}:d\downarrow^{\circ}$ and $c^{\bullet}:d\uparrow^{\circ}$; $c\downarrow^{\bullet},d\downarrow^{\circ}$
- The test suite for REP.(a°,b•) contains an infinite number of singleton tests, such as $test_n$ with $n>0$ complete communications along *b*.
  $test_n = a\uparrow^{\bullet}:(b^{\circ})^n$; initialize
- The test suite for a variable contains a single test with two test obligations:
  $a^{\bullet}!0$; $b^{\bullet}?y$ and $a^{\bullet}!1$; $b^{\bullet}?y$

Where convenient, we henceforth define a singleton test by giving its single element.

TESTABILITY ENHANCEMENT

For circuits with dual rail data encoding it suffices to test the setting and resetting of data outputs, unlike circuits with single rail data encoding, where the values are important as well. Also for synchronizations per se, it is sufficient to test for setting and resetting of synchronization wires. The test interfaces for the inbreaking and

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outbreaking components can therefore be simpler than the standard interfaces (cf. Figure 14 as an optimized version of Figure 4). Herein, the uninterrupted arrow delimits the test trajectory for component A, the interrupted arrow delimits the test trajectory for component P.

- Breaking into a synchronization channel is done with the following type of junction:

$JUNCTION_{(-,-)}.(p_s^\circ, p_t^\circ, p^\bullet) =$
$(p_s^\circ, p_t^\circ, p^\bullet).$
$*[p_s\uparrow^\circ : p\uparrow^\bullet;\ p_s\downarrow^\circ p\downarrow^\bullet$
$\ |\ p_t\uparrow^\circ : p\uparrow^\bullet;\ p_t\downarrow^\circ : p\downarrow^\bullet$
$]$

Note that the multiplexer $MIX.(p_s^\circ, p_t^\circ, p^\bullet)$ matches this specification.

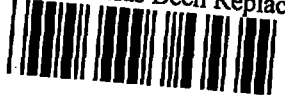
Junctions for breaking into data input channels with W bits are specified by:

$JUNCTION_{(?,W)}.(p_s^\circ, p_t^\circ, p^\bullet) =$
$(p_s^\circ\ ?W, p_t^\circ\ ?W, p^\bullet!W).$
$[\![$ x: var W
$\ |\ *[\ p_s\uparrow^\circ ?x: p\uparrow^\bullet !x;\ p_s\downarrow^\circ ?x: p\downarrow^\bullet !x$
$\quad |\ p_t\uparrow^\circ ?x: p\uparrow^\bullet !x;\ p_t\downarrow^\circ ?x: p\downarrow^\bullet !x$
$\quad]$
$]\!]$

Junctions for breaking into data output channels with W bits, $JUNCTION_{(!,W)}.(p_s^\circ, p_t^\circ, p^\bullet)$, are specified by:

$JUNCTION_{(!,w)}\ .\ (p_s^\circ, p_t^\circ, p^\bullet) =$
$(p_s^\circ\ !W, p_t^\circ, p^\bullet?W).$
$[\![$ x: var W
$\ |\ *[\ p_s\uparrow^\circ !x\ :\ p\uparrow^\bullet ?x;\ p_s\downarrow^\circ !x\ :\ p\downarrow^\bullet ?x$
$\quad |\ p_t\uparrow^\circ :\ p\uparrow^\bullet ?x\ ;\ p_t\downarrow^\circ : p\downarrow^\bullet ?x$
$\quad]$
$]\!]$

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- The mode of operation in the outbreaking components is controlled by a boolean

port a_m and an internal boolean variable *t: false* for standard mode, and *true* for non-standard or test mode. The switches for breaking out of synchronization channels are specified by:

$SWITCH_{(-,-)}.(a_s^\bullet, a_t^\bullet\ a_m^\circ, a^\circ) =$

$(a_s^\bullet, a_t^\bullet, a_m^\circ?\ \text{bool}, a^\circ)$

⟦ t: var bool

| * [a_m°?t

| $a\uparrow^\circ$:[$\neg t \rightarrow a_s\uparrow^\bullet$ □ t→skip];

| $a\downarrow^\circ$:[$\neg t \rightarrow a_s\downarrow^\bullet$ □ t→skip]

]

⟧

Switches for breaking out of input channels with W bits are specified by:

$SWITCH_{(?,W)}.(a_s^\bullet, a_t^\bullet, a_m^\circ, a^\circ) =$

$(a_s^\bullet?W, a_t^\bullet? W, a_m^\circ ?\ \text{bool}, a^\circ!W).$

⟦ t: var bool

& x: var W

| *[a_m°?t

|$a\uparrow^\circ$!X:[$\neg t \rightarrow a_s\uparrow^\bullet$?X□$t \rightarrow a_t\uparrow^\bullet$?X];

$a\downarrow^\circ$!X:[$\neg t \rightarrow a_s\downarrow^\bullet$?X□$t \rightarrow a_t\downarrow^\bullet$?]

]

⟧

Switches for breaking out of data output channels with W bits are specified by

$SWITCH_{(!,W)}.(a_s^\bullet, a_m^\circ, a^\circ) =$

$(a_s^\bullet? W, a_t^\bullet ? W, a_m^\circ?\text{bool}, a^\circ?W).$

⟦ t: var bool

& x: var W

| *[a_m°?t

|$a\uparrow^\circ$!x:[$\neg t \rightarrow a_s\uparrow^\bullet$!W□t→skip];

$a\downarrow^\circ$!x:[$\neg t \rightarrow a_s\downarrow^\bullet$!W□t→skip]

]

⟧

Figure 15 gives the counterpart of Figure 7 for the basic components

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SEQ.(a°,b•, c•) and MIX.(b°,c°,d•), in their combination as duplicator. The ports with index 0 are part of the test interface of the environment, the ports with index 1 form the test interface of SEQ.(a°,b•,c•), and those with index 2 form the test interface of MIX.(b°,c°,d•).

Figure 16 gives the corresponding counterpart to $VAR_{(1,1)}.(a°,b°)$, with junctions and switches for data.

TEST GENERATION

A possible test counterpart of SEQ.(a°,b•,c•) in the configuration of Figure 15 is:

$(a_m^{(0)\bullet}!false \parallel b_m^{(1)\bullet}!true \parallel c_m^{(1)\bullet}!true);\ a_t^{(1)\bullet}$

A possible test counterpart of MIX.(b°,c°,d•) in the configuration of Figure 15 is:

$(b_m^{(1)\bullet}!false \parallel c_m^{(1)\bullet}!false \parallel d_m^{(2)\bullet}!true);\ b_t^{(2)\bullet};\ c_t^{(2)\bullet}$

A test for the complete duplicator of Figure 15 includes the testing of the boundary, i.e. channels a_s and d_s. A possible boundary test is:

$(a_m^{(0)\bullet}!true \parallel d_m^{(2)\bullet}!false);\ (a_s^{\bullet} \parallel (d_t^{(0)}\uparrow^{\bullet}: d_s\uparrow^{\circ};\ d_t\downarrow^{\bullet}: d_s\downarrow^{\circ}))$

There are several possibilities to combine these to a test for the complete duplicator.

- An example where the components are successively tested is:

  $(a_m^{(0)\bullet}!false \parallel b_m^{(1)\bullet}!true \parallel c_m^{(1)\bullet}!true);\ a_t^{(1)\bullet};$

  $(b_m^{(1)\bullet}!false \parallel c_m^{(1)\bullet}!false \parallel d_m^{(2)\bullet}!true);\ b_t^{(2)\bullet};\ c_t^{(2)\bullet};$

  $(a_m^{(0)\bullet}!true \parallel d_m^{(2)\bullet}!false);\ (a_s^{\bullet} \parallel (d_t^{(0)}\uparrow^{\bullet}: d_s\uparrow^{\circ};\ d_t^{(0)}\downarrow^{\bullet}: d_s\downarrow^{\circ}))$

- An example where the tests are interleaved is:

  $(b_m^{(1)\bullet}!false \parallel c_m^{(1)\bullet}!true \parallel d_m^{(2)\bullet}!true);\ b_t^{(2)\bullet};$

  $(a_m^{(0)\bullet}!false \parallel b_m^{(1)\bullet}!true);\ a_t^{(1)\bullet};$

  $c_m^{(1)\bullet}!false;\ c_t^{(2)\bullet};$

  $(a_m^{(0)\bullet}!true \parallel d_m^{(2)\bullet}!false);\ (a_s^{\bullet} \parallel (d_t^{(0)}\uparrow^{\bullet}: d_s\uparrow^{\circ};\ d_t^{(0)}\downarrow^{\bullet}: d_s\downarrow^{\circ}))$

Note that the behaviour of all the junctions during these tests covers the test obligations as given for MIX.(.°, .°, .•): the junctions play a self-diagnostic role. This is also true for the switches.

Testing a handshake component with data in an equally enhanced configuration is similar. A test for the basic handshake component $VAR_{(1,1)}.(a°,b°)$ in Figure 16 is for example:

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$(a_m^{(0)}!false \parallel b_m^{(0)}!false)\ ;\ a_t^{(1)\bullet}!0\ ;\ b_t^{(1)\bullet}\ ;\ a_t^{(0)\bullet}!1\ ;\ b_t^{(1)\bullet}$

VARIOUS OPTIMIZATIONS

That test application and performance costs can be tuned by judiciously choosing the internal points for testability enhancement, is illustrated using Figures 17 a, b. Without testability enhancement, as in Figure 17a, the number of test events in this chain of n duplicators is $O(2^{n+1})$. Insertion of testability provisions half-way down the chain, as in Figure 17b, gives a significant exponential reduction to $O(2^{\frac{n+1}{2}})$ test events.

Another solution is shown in Figure 18a, where a new basic component $MIX^t.(m^\circ, b^\circ, c^\circ, d^\bullet)$ has been substituted for $MIX.(b^\circ, c^\circ, d^\bullet)$. The new component is a composition of the original one with a switch for breaking out of channel c (cf. Figure 18b). Its behaviour is as follows:

$MIX^t(m^\circ, b^\circ, c^\circ, d^\bullet) =$

$(m^\circ?bool, b^\circ, c^\circ, d^\bullet).$

```
[[ t : var bool
 | *[ m°?t
      |b↑° : d↑• ; b↓° : d↑•
      |c↑° : [¬t→d↑• □ t → skip]
       c↓° : [¬t→d↓• □ t → skip]
    ]
]]
```

A possible test for $MIX^t.(m^\circ, b^\circ, c^\circ, d^\bullet)$ that links up nicely with the $SEQ.(a^\circ, b^\bullet, c^\bullet)$-components in the duplicator is:

$m^\bullet!true;\ b\uparrow^\bullet : d\uparrow^\circ\ ;\ b\downarrow^\bullet : d\downarrow^\circ\ ;\ c^\bullet\ ;\ m^\bullet!false$

This validates the following test for the complete chain in Figure 18a:

$(m_1{}^\bullet!true \parallel \ldots \parallel m_n{}^\bullet!true)\ a\uparrow^\bullet{:}d^\circ\ ;\ a\downarrow^\bullet\ ;\ (m_1{}^\bullet!false \parallel \ldots \parallel m_n{}^\bullet!false)$

The corresponding number of test events is O(n).

Because the test language is similar to the programming language, an automatic (partial) integration of the test can be facilitated by the compiler. If, for

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example, the parts

$(m_1^\bullet !true \parallel \ldots \parallel m_n^\bullet !true) \,.\, (m_1^\bullet !false \parallel \ldots \parallel m_n^\bullet !false)$

are built-in, the number of additional external channels is reduced to 2: m and s. The circuit test reduces to:

$(s^\bullet \parallel m^\bullet !true \,;\, a\uparrow^\bullet : d^\circ \,;\, a\downarrow^\bullet \,;\, (s^\bullet \parallel m^\bullet !false)$

A considerable amount of circuitry is added, however.

An alternative solution, with the same advantages, but without the overhead in circuitry, is to use a single wire to set the circuit in the appropriate mode of operation (cf. Figure 19). This wire, here referred to as t, is both an external input and an external output of the circuit, and is routed through all the basic components having a test mode. This can be done such that, in all handshake components with a test mode, the events at the output side of t serve as acknowledgement of the events at the input side of t:

after the events at the input side of t become observable at the output side of t, the rest of the circuit is set in the appropriate mode before a fixed amount of time has passed.

As for initialization, the amount of time to settle can be calculated from the circuit. Thus, t can be conceived as a channel with two wires. Here, we take a two-phase handshake protocol to communicate along t, where t=1 represents the test mode and t=0 the standard mode of operation. The components with a test mode, i.e. where the behaviour under test is different from the standard behaviour, are slightly changed. A possible specification for $MIX^t.(t^\circ, b^\circ, c^\circ, d^\bullet)$ is given below.

$MIX^t.(t^\circ, b^\circ, c^\circ, d^\bullet) =$

$(t^\circ, b^\circ, c^\circ, d^\bullet)$

$*[\; t\uparrow^\circ$

$\;\; | \; t\downarrow^\circ$

$\;\; | \; b\uparrow^\circ : d\uparrow^\bullet \,;\, b\downarrow^\circ : d\uparrow^\bullet$

$\;\; | \; c\uparrow^\circ : [t=0 \rightarrow d\uparrow^\bullet \;\square\; t=1 \rightarrow skip]$

$\;\;\;\; c\downarrow^\circ : [t=0 \rightarrow d\downarrow^\bullet \;\square\; t=1 \rightarrow skip]$

$\;]$

The test for the complete chain is now:

$t\uparrow^\bullet \,;\, a\uparrow^\bullet : d^\circ \,;\, a\downarrow^\bullet \,;\, t\downarrow^\bullet .$

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CLAIMS:



1. A method for testing electronic circuitry having a plurality of functional components interconnected by handshake communication channels each channel terminating at respective functional components by an active port from which a communication is initiated and a passive port where such communication is awaited, respectively, said method comprising providing one of said channels with an inbreaking junction thereby forming a first test component that at other times than testing just forms part of the in-channel handshaking, said method comprising breaking in via a passive port of said junction with a first test signalization as an alternative to any in-channel signalization towards the in-channel passive port of said junction, said first test signalization representing the test signalization for said channel in a test on any component with a passive port on said channel and inclusive of any channel part between said any component and said test component.

2. A method for testing electronic circuitry having a plurality of functional components interconnected by handshake communication channels each terminating at respective functional components by an active port from which a communication is initiated and a passive port where such communication is awaited, respectively, said method comprising providing one or more of said channels with an inbreaking junction and/or one or more of said channels with an outbreaking switch thereby forming a set of test components that at other times than testing just form part of the in-channel handshaking, said method comprising breaking in via a passive port of a first channel's junction with a first test signalization as an alternative to any in-channel signalization towards the in-channel passive port of said junction, under control of an external control signal to a control port of a switch on a second channel breaking out therefrom a second test signalization via an active extra-channel port thereof as an alternative to any further in-channel signalization via any active further port of said second channel's switch, said first c.q. second test signalization being the test signalization for said first c.q. second channel in a test on any component with a passive port on said first channel c.q. with

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with an active port on said second channel, and inclusive of any channel part between said components and said test components.

3. A method as claimed in Claim 1 or 2, comprising providing at least one channel with a switch that in its test signalization is controlled both in test mode for breaking out of in-channel signalizations within said at least one channel as well as in non-test mode for continuing in-channel signalizations.

4. A method as claimed in Claim 1 to 3 for executing a plurality of tests on respective functional components by presenting to said circuitry an aggregate test signal including aggregate control signals, extracting therefrom first test signalizations for inbreaking onto various junctions and also respective external control signals for presentation to various switches and also respective second test signalizations for breaking out from various switches.

5. A method as claimed in any Claim 1 to 4, for testing said electronic circuitry having a plurality of integrated circuits, by assigning to any channel crossing any border between separate integrated circuits a dummy functional component at said border for so at either side of said border creating a separate channel as a respective one of said handshake channels and for executing an interconnection test by means of inbreaking and outbreaking of respective test signalizations on said respective separate channels pairwise joined by an associated said dummy functional component.

6. An integrated circuit that is testable according to a method as claimed in any of Claims 1 to 5, and comprises a plurality of testable functional components that are interconnected by handshake communication channels each terminating at respective functional components by an active communication initiating port and a passive communicating awaiting port, respectively, and at least part of said channels being provided with an inbreaking junction or an outbreaking switch, thereby forming a set of test components that at other times than testing just form part of the in-channel handshaking, any said junctions having a first passive channel port for in-channel initiated communications and a second passive test port for externally initiated test communications, and a first active channel port for propagating both said types of initiated communications, any said switch having a third passive channel port for in-channel initiated communications, a second active channel port for in-channel propagation of these initiated communications and in each one of at least part of said

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switches a combination of a third active test port for extra-channel propagation of these initiated communications and a fourth passive control port for selecting for propagation between said second active channel port and said third active test port, said circuit furthermore having test control means for breaking in onto any said second passive test port with said externally initiated test pattern.

7. An integrated circuit according to Claim 6, and wherein at least one channel comprises both a junction and a switch that together constitute a test component pair, thereby allowing both inbreaking and outbreaking test facilities for said at least one channel.

8. An integrated circuit as claimed in Claim 6 or 7 and comprising a further channel terminating in a dummy functional component for attachment to a further integrated circuit and said further channel being provided with a junction and a switch as a test component pair.

9. A circuit as claimed in any of Claims 6 to 8, and comprising self-test means for receiving an external activation signal and having developing means for developing from a provided aggregate test signal including control signal various elementary test signalizations and control signalizations for said junctions and switches, and for receiving and aggregating various elementary result signalizations to an aggregate result signal for inspection outside said circuit.

10. A circuit as claimed in any of Claims 6 to 9, and wherein at least one junction has an electronic part in common with some channelwise contiguous component and wherein at least one switch has an electronic part in common with some channelwise contiguous component.

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