

DISPLAY DEVICE

BACKGROUND

Technical Field

[0001] The disclosure relates to an electronic apparatus, and particularly to a display apparatus.

Description of Related Art

[0002] With the development of display technology, people demand more from display apparatus than optical characteristics, such as high resolution, high contrast, and wide viewing angle. People also expect to see elegance in the appearance of display apparatus. For example, people expect the display apparatus to have a narrow bezel, even without a bezel.

[0003] Generally speaking, a display apparatus includes pixel structures configured in a display area, a data driving circuit configured below the display area, and gate driving circuits configured on the left, right, or both sides of the display area. In order to reduce the widths of the left and right sides of the bezel of the display apparatus, both the gate driving circuit and the data driving circuit may be arranged on the lower side of the display area. When the gate driving circuit is configured on the lower side of the display area, the horizontal gate lines need to be electrically connected to the gate driving circuit through the vertical gate line. However, the gate-on pulse signal of the vertical gate lines may affect the potentials of some pixel structures, thereby causing abnormal display.

SUMMARY

[0004] The disclosure provides a display apparatus with excellent performance.

[0005] The disclosure also provides another display apparatus with excellent performance as well.

[0006] A display apparatus of the disclosure includes a first substrate, multiple data lines, multiple first gate lines, multiple pixel structures, multiple second gate lines, multiple first common lines, a second substrate, and a display medium. The data lines are configured on the first substrate, and are

arranged in a first direction. The first gate lines are configured on the first substrate, and are configured in a second direction, in which the first direction crisscrosses the second direction. The pixel structures are configured on the first substrate, and are electrically connected to the scan lines and the data lines. The second gate lines are configured on the first substrate, in which the data lines and the second gate lines are arranged in the first direction, and the second gate lines are electrically connected to the first gate lines. The first common lines are configured on the first substrate, in which the pixel structures are arranged in pixel columns, and the pixel columns are arranged in the first direction. Each of the first common lines and the corresponding second gate line are configured between two adjacent pixel columns of the pixel columns. The first common line and the corresponding second gate line are respectively configured on the opposite sides of the first gate line which is electrically connected to the second gate line. And the first common line and the corresponding second gate line are structurally separated. The second substrate is configured to be opposite to the first substrate. The display medium is configured between the first substrate and the second substrate.

[0007] Another display apparatus of the disclosure includes a first substrate, multiple data lines, multiple first gate lines, multiple pixel structures, multiple second gate lines, a second substrate, and a display medium. The data lines are configured on the first substrate, and are arranged in a first direction. The first gate lines are configured on the first substrate, and are arranged in a second direction, in which the first direction crisscrosses the second direction. The pixel structures are configured on the first substrate, electrically connected to the data lines and the first gate lines, and arranged in x number of pixel columns and y number of pixel rows. The x number of pixel columns are arranged in the first direction, the y number of pixel rows are arranged in the second direction, x and y are positive integers greater than 2, and the pixel structure has a first width a1 and a second width a2 respectively in the first direction and the second direction. The second gate lines are configured on the first substrate, in which the data lines and the second gate lines are arranged in the

first direction, and the second gate lines are electrically connected to the first gate lines. The second substrate is configured to be opposite to the first substrate. The display medium is configured between the first substrate and the second substrate. Each of the first gate lines is electronically connected to n number of the second gate lines. $(a1 \cdot x + a2 \cdot y) < 2000000$, and $n=2$; or $2000000 < (a1 \cdot x + a2 \cdot y) < 2400000$, and $n=3$; or $2400000 < (a1 \cdot x + a2 \cdot y) < 3000000$, and $n=4$; or $(a1 \cdot x + a2 \cdot y) > 3000000$, and $n=5$.

[0008] In an embodiment of the disclosure, a signal of the first common line as described above and a gate-off signal of the second gate line are substantially the same.

[0009] In an embodiment of the disclosure, each of the first gate lines as described above is electrically connected to the n number of the second gate lines, in which n is a positive integer. Each of the first gate lines and the n number of the second gate lines have the 1st to nth connection points arranged in sequence in the first direction. The second gate lines include the 1st to nth second gate line groups arranged in sequence in the first direction. The second gate lines of the mth second gate line group of the 1st to nth second gate line groups and the correspond first gate lines have the mth connection point of the 1st to nth connection points, in which m is a positive integer, and $n \geq m \geq 1$. The display apparatus further includes a common electrode, multiple common pad groups, multiple first transfer elements, n number of second common pads, and n number of second transfer elements. The common electrode is configured on the second substrate, and is located between the second substrate and the display medium. The common pad groups are configured on the first substrate, and are configured to correspond respectively to the 1st to nth second gate line groups, in which the pixel structures have a first side and a second side opposite to each other. The common pad groups are configured on the second side of the pixel structures, and each of the common pad groups includes multiple first common pads. The first transfer elements are configured respectively on the first common pads of the common pad groups, and are electrically connected to the first common pads of the common pad groups and the common electrode. The n number of the second common pads are

configured on the first substrate, and are configured to correspond respectively to the 1st to nth second gate line groups, and are located on the first side of the pixel structures. The n number of the second transfer elements are configured respectively on the n number of the second common pads, and are electrically connected to the n number of the second common pads and the common electrode. A common pad group and a second common pad correspond to the same second gate line group, and the potential of the second common pad is greater than the potentials of the first common pads of the common pad group.

[0010] In an embodiment of the disclosure, the display as described above further includes a third common pad, which is configured on the first substrate and is located on the first side of pixel structures. The third common pad and the second common pads are arranged in sequence in the first direction and are structurally separated from each other. The third common pad is configured to correspond to the 1st second gate line group of the 1st to nth second gate line groups. And the potential of the third common pad is greater than the potentials of the corresponding second common pads.

[0011] In an embodiment of the disclosure, the display apparatus as described above further includes multiple second common lines, a first peripheral line, and a second peripheral line. The second common lines are configured on the first substrate, and the second gate lines and the second common lines are arranged in the first direction, in which each of the second common lines is configured between two adjacent pixel columns of the pixel columns. The first peripheral line is configured on the first substrate and is located on the first side of the pixel structures, in which the first common lines are electrically connected to the first peripheral line. The second peripheral line is configured on the first substrate and is located on the second side of the pixel structures, in which the two ends of each of the second common lines are electrically connected respectively to the first peripheral line and the second peripheral line.

[0012] In an embodiment of the disclosure, the first gate lines as described above include an odd

number of the first gate lines and an even number of the first gate lines. The odd number of the first gate lines include the $(1+2\cdot K)^{\text{th}}$ first gate lines, in which $K=0, 1, \dots, p$, and p is a positive integer greater than or equal to 2. The even number of the first gate lines include the $2L^{\text{th}}$ first gate lines, in which $L=1, 2, \dots, q$, and q is a positive integer greater than or equal to 3. The second gate lines include the 1^{st} to $(p+1)^{\text{th}}$ second gate lines and the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines arranged in sequence in the first direction. The 1^{st} to $(p+1)^{\text{th}}$ second gate lines are electrically connected to the $(1+2\cdot K)^{\text{th}}$ first gate line, and the $(p+2)$ to the $(p+q+1)^{\text{th}}$ second gate lines are electrically connected to the $2L^{\text{th}}$ first gate line.

[0013] In an embodiment of the disclosure, the connection points of the 1^{st} to $(p+1)^{\text{th}}$ second gate lines and the $(1+2\cdot K)^{\text{th}}$ first gate line as well as the connection points of the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines and the $2L^{\text{th}}$ first gate line are generally distributed along multiple diagonal lines parallel to each other.

[0014] In an embodiment of the disclosure, the connection points of the 1^{st} to the $(p+1)^{\text{th}}$ second gate lines and the $(1+2\cdot K)^{\text{th}}$ first gate line as well as the connection points of the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines and the $2L^{\text{th}}$ first gate line are generally distributed in a V-shaped pattern.

[0015] In an embodiment of the disclosure, the display apparatus as described above further includes multiple first common lines configured on the first substrate. Each of the first common lines and the corresponding second gate line are configured between two adjacent pixel columns of x number of the pixel columns. The first common line and the corresponding second gate line are configured respectively on the opposite sides of the first gate line electrically connected to the second gate line. And the first common line and the corresponding second gate line are structurally separated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Fig. 1 is a schematic cross-sectional view of a display apparatus 10 according to an

embodiment of the disclosure.

[0017] Fig. 2 is a schematic top view of a pixel array substrate 100, a plurality of first transfer elements T1, a plurality of second transfer elements T2, and a third transfer element T3 according to an embodiment of the disclosure.

[0018] Fig. 3 is a schematic top view of an opposite substrate 200, a plurality of first transfer elements T1, a plurality of second transfer elements T2, and a third transfer element T3 according to an embodiment of the disclosure.

[0019] Fig. 4 is a schematic top view of a pixel array substrate 100A, a plurality of first transfer elements T1, a plurality of second transfer elements T2, and a third transfer element T3 according to an embodiment of the disclosure.

[0020] Fig. 5 is a schematic top view of a pixel array substrate 100B and a plurality of first transfer elements T1 according to an embodiment of the disclosure.

[0021] Fig. 6 is a schematic top view of a pixel array substrate 100C and a plurality of first transfer elements T1 according to an embodiment of the disclosure.

[0022] Fig. 7 is a schematic top view of a pixel array substrate 100D and a plurality of first transfer elements T1 according to an embodiment of the disclosure.

[0023] Reference numbers in the drawings:

10: display apparatus

100, 100A, 100B, 100C, 100D: substrate

110: first substrate

120: element layer

200: opposite substrate

210: second substrate

220: common electrode

221: first part

222: second part

223: third part

300: display medium

a1: first width

a2: second width

Cpx: pixel column

C、C1、C2、C3: connection point

CL1、CL11、CL12、CL13、CL14、CL15、CL16: first common line

CL2: second common line

D1: first direction

D2: second direction

DL: data line

Gvg、Gvg1、Gvg2、Gvg3: second gate line group

Gp1a、Gp1b、Gp1c: common pad group

HG、HG1、HG2、HG3、HG4、HG5、HG6: first gate line

K: diagonal line

L1: first peripheral line

L2: second peripheral line

Lp1a、Lp1b、Lp1c、Lp2a、Lp2b、Lp2c、Lp3、Ll1、Ll2: wire

PX: pixel structure

p1a、 p1b、 p1c: first common pad

p2a、 p2b、 p2c: second common pad

p3: third common pad

Rpx: pixel row

S1: first side

S2: second side

T1: first transfer element

T2: second transfer element

T3: third transfer element

VG、 VG1、 VG2、 VG3、 VG4、 VG5、 VG6: second gate line

DESCRIPTION OF THE EMBODIMENTS

[0024] References of the exemplary embodiments of the disclosure are to be made in detail. Examples of the exemplary embodiments are illustrated in the drawings. If applicable, the same reference numerals in the drawings and the descriptions indicate the same or similar parts.

[0025] It should be understood that when an element, such as a layer, a film, an area, or a substrate, is indicated to be “on” another element or “connected to” another element, it may be directly on another element, connected to another element, or an element may exist in the middle. In contrast, when an element is indicated to be “directly on another element” or “directly connected to” another element, an element does not exist in the middle. For example, the term “connect(ed)” indicated in the specification may indicate a physical and/or electrical connection. Furthermore, the phrase “electrically connect(ed)” or “couple(d)” may also be used when other elements exist between two elements.

[0026] The usages of “approximately”, “similar to”, “essentially”, or “substantially” indicated throughout the specification include the indicated value and an average value having an acceptable deviation range, which is a certain value confirmed by people skilled in the art, and is a certain amount considered the discussed measurement and measurement-related deviation (that is, the limitation of measurement system). For example, “approximately” may indicate to be within one or more standard deviations of the indicated value, such as being within $\pm 30\%$, $\pm 20\%$, $\pm 10\%$, or $\pm 5\%$. Furthermore, the usages of “approximately”, “similar to”, or “substantially” indicated throughout the specification may refer to a more acceptable deviation scope or standard deviation depending on optical properties, etching properties, or other properties, and all properties may not be applied with one standard deviation.

[0027] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as they are commonly understood by those of ordinary skill in the art. It should be further understood that terms such as those defined in the common dictionaries should be interpreted in the context of the relevant technology and the present disclosure with whom the meanings of the terms are consistent, and the terms should not be interpreted in an idealized or excessively formal way unless they are explicitly defined as such herein.

[0028] Fig. 1 is a schematic cross-sectional view of a display apparatus 10 according to an embodiment of the present disclosure.

[0029] As shown in Fig.1, the display apparatus 10 includes a pixel array substrate 100, an opposite substrate 200, and a display medium 300, in which the display medium 300 is configured between the pixel array substrate 100 and the opposite substrate 200. The pixel array substrate 100 includes a first substrate 110 and an element layer 120, in which the element layer 120 is configured on the first substrate 110 and is located between the display medium 300 and the first substrate 110. The opposite substrate 200 includes a second substrate 210, in which the second substrate 210 is configured to be opposite to the first substrate 110, and the display medium 300 is located between

the first substrate 110 and the second substrate 210.

[0030] In the present embodiment, a material of the first substrate 110 may be glass, quartz, organic polymer, or other applicable materials; a material of the second substrate 210 may be glass, quartz, organic polymer, or other applicable materials.

[0031] In the present embodiment, the display medium 300 may be, for example, a liquid crystal. However, the present embodiment is not limited thereto. In other embodiments, the display medium 300 may also be an organic electroluminescent layer or other applicable materials.

[0032] Fig. 2 is a schematic top view of a pixel array substrate 100, a plurality of first transfer elements T1, a plurality of second transfer elements T2, and a third transfer element T3 according to an embodiment of the disclosure.

[0033] As shown in Fig. 1 and Fig. 2, the element layer 120 of the pixel array substrate 100 includes a plurality of data lines DL, a plurality of first gate lines HG, a plurality of pixel structures PX, and a plurality of second gate lines VG.

[0034] As shown in Fig. 2, the data lines DL are configured on the first substrate 110 and are arranged in a first direction D1. The first gate lines HG are configured on the first substrate 110, and are arranged in a second direction D2, in which the first direction D1 crisscrosses the second direction D2. For example, in the present embodiment, the first direction D1 and the second direction D2 may be substantially perpendicular to each other, but the present disclosure is not limited thereto.

[0035] In the present embodiment, the data lines DL and the first gate lines HG belong to different film layers. For example, in the present embodiment, the first gate lines HG may belong to a first metal layer while the data lines DL may belong to a second metal layer, but the present disclosure is not limited thereto. Based on consideration of conductivity, in the present embodiment, the data lines DL and the first gate lines HG are made of metal materials, but the disclosure is not limited thereto. In other embodiments, the data lines DL and/or the first gate lines HG may also be made

of other conductive materials, such as alloys, nitrides of metal materials, oxides of metal materials, oxynitrides of metal materials, or stacked layers of metal materials and other conductive materials.

[0036] The pixel structures PX are configured on the first substrate 110 and are electrically connected to the data lines DL and the first gate lines HG. Specifically speaking, in the present embodiment, each of the pixel structures PX may include a thin-film transistor (not illustrated) and a pixel electrode (not illustrated), in which the thin-film transistor has a first end, a second end, and a control end. The first end of the thin-film transistor is electrically connected to a corresponding data line DL. The control end of the thin-film transistor is electrically connected to a corresponding first gate line HG. And the second end of the thin-film transistor is electrically connected to the pixel electrode.

[0037] The second gate lines VG are configured on the first substrate 110, in which the data lines DL and the second gate lines VG are arranged in the first direction, and the second gate lines VG are electrically connected to the first gate lines HG.

[0038] Specifically speaking, in the present embodiment, the pixel structures PX are arranged in a plurality of pixel columns Cpx and a plurality of pixel rows Rpx. The pixel columns Cpx are arranged in the first direction D1, and the pixel structures PX of each of the pixel columns Cpx are arranged in the second direction D2. The pixel rows Rpx are arranged in the second direction D2, and the pixel structures PX of each of the pixel rows Rpx are arranged in the first direction D1. In the top view of the pixel array substrate 100, each of the second gate lines VG is configured between two adjacent pixel columns Cpx. In other words, the second gate lines VG are interwoven in an active area of the pixel array substrate 100, and each of the second gate lines VG is electrically connected to at least one corresponding first gate line HG in the active area.

[0039] For example, in the present embodiment, the first gate lines HG include a first gate line HG1, a first gate line HG2, a first gate line HG3, a first gate line HG4, a first gate line HG5, and a first gate line HG6, which are arranged in sequence in the second direction D2; and the second gate

lines VG include a second gate line VG1, a second gate line VG2, a second gate line VG3, a second gate line VG4, a second gate line VG5, and a second gate line VG6, which are arranged in sequence in the first direction D1 and may be electrically connected respectively to the first gate line HG1, the first gate line HG2, the first gate line HG3, the first gate line HG4, the first gate line HG5, and the first gate line HG6. However, the present embodiment is not limited thereto. In other embodiments, the second gate lines VG may also be connected to the first gate lines HG by other means.

[0040] In Fig. 1 and Fig. 2, it is worthy of note that the element layer 120 of the pixel array substrate 100 further includes a plurality of first common lines CL1. As shown in Fig. 2, the first common lines CL1 are configured on the first substrate 110. In a top view of the pixel array substrate 100, each of the first common lines CL1 and the corresponding second gate line VG are configured between two adjacent pixel columns Cpx. The first common line CL1 and the corresponding second gate line VG are configured respectively on the opposite sides of the first gate line HG which is electrically connected to the second gate line VG. And the first common line CL1 is structurally separated from the corresponding second gate line VG.

[0041] For example, in the present embodiment, the second gate lines VG include the second gate line VG1, the second gate line VG2, the second gate line VG3, the second gate line VG4, the second gate line VG5, and the second gate line VG6, which are respectively electrically connected to the first gate line HG1, the first gate line HG2, the first gate line HG3, the first gate line HG4, the first gate line HG5, and the first gate line HG6. The first common lines CL1 include a first common line CL11, a first common line CL12, a first common line CL13, a first common line CL14, a first common line CL15, and a first common line CL16, which correspond respectively to the second gate line VG1, the second gate line VG2, the second gate line VG3, the second gate line VG4, the second gate line VG5, and the second gate line VG6. In a top view of the pixel array substrate 100, the first common line CL11 and the second gate line VG1 are respectively configured on the opposite sides of the first gate line HG1 which is electrically connected to the second gate line VG1, and the first

common line CL11 is structurally separated from the second gate line VG1; the first common line CL12 and the second gate line VG2 are respectively configured on the opposite sides of the first gate line HG2 which is electrically connected to the second gate line VG2, and the first common line CL12 is structurally separated from the second gate line VG2; the first common line CL13 and the second gate line VG3 are respectively configured on the opposite sides of the first gate line HG3 which is electrically connected to the second gate line VG3, and the first common line CL13 is structurally separated from the second gate line VG3; the first common line CL14 and the second gate line VG4 are respectively configured on the opposite sides of the first gate line HG4 which is electrically connected to the second gate line VG4, and the first common line CL14 is structurally separated from the second gate line VG4; the first common line CL15 and the second gate line VG5 are respectively configured on the opposite sides of the first gate line HG5 which is electrically connected to the second gate line VG5, and the first common line CL15 is structurally separated from the second gate line VG5; and the first common line CL16 and the second gate line VG6 are respectively configured on the opposite sides of the first gate line HG6 which is electrically connected to the second gate line VG6, and the first common line CL16 is structurally separated from the second gate line VG6.

[0042] It is worthy of note that, whether or not the second gate lines VG are provided next to the pixel structures PX, with the configuration of the first common lines CL1, the pixel structures PX may sense the same or similar distribution of electric field, and thereby improving the display quality.

[0043] In the present embodiment, a signal of the first common lines CL1 and a gate-off signal of the second gate lines VG are substantially the same. Specifically speaking, in the present embodiment, whether a signal of the second gate lines VG is a gate-close signal or a gate-open signal, a signal of the first common lines CL1 may be fixed to be the gate-close signal. For example, in the present embodiment, the gate-close signal may be a DC signal between -9 volts and -10 volts, but the disclosure is not limited thereto.

[0044] In the present embodiment, the first common lines CL1 and the first gate lines HG belong

to different film layers. For example, in the present embodiment, the first gate lines HG may belong to a first metal layer while the first common lines CL1 may belong to a second metal layer, but the disclosure is not limited thereto. Based on the consideration of conductivity, in the present embodiment, the material of the first common lines CL1 is a metal material. However, the disclosure is not limited thereto. In other embodiments, the first common lines CL1 may also be made of other conductive materials, such as alloys, nitrides of a metal material, oxides of a metal material, oxynitrides of a metal material, or a stacked layer of metal materials and other conductive materials.

[0045] As shown in Fig. 1 and Fig. 2, in the present embodiment, the element layer 120 of the pixel array substrate 100 further includes a first peripheral line L1. As shown in Fig. 2, the first peripheral line L1 is configured on the first substrate 110 and is located on a first side S1 of the pixel structures PX. The first common lines CL1 are electrically connected to the first peripheral line L1.

[0046] As shown in Fig. 1 and Fig. 2, in the present embodiment, the element layer 120 of the pixel array substrate 100 further includes a plurality of second peripheral lines CL2. As shown in Fig. 2, the second common lines CL2 are configured on the first substrate 110, the second gate lines VG and the second common lines CL2 are arranged in the first direction D1, and each of the second common lines CL2 is configured between two adjacent pixel columns Cpx. Specifically speaking, there are multiple layout areas between the pixel columns Cpx, and the second common lines CL2 are configured on the layout areas where the second gate lines VG and the first common lines CL1 are not provided.

[0047] In the present embodiment, the second common lines CL2 and the first gate lines HG belong to different film layers. For example, in the present embodiment, the first gate lines HG may belong to a first metal layer while the second common lines CL2 may belong to a second metal layer, but the disclosure is not limited thereto. Based on the consideration of conductivity, in the present embodiment, the material of the second common lines CL2 is a metal material. However, the

disclosure is not limited thereto. In other embodiments, the second common lines CL2 may also be made of other conductive materials, such as alloys, nitrides of a metal material, oxides of a metal material, oxynitrides of a metal material, or a stacked layer of metal materials and other conductive materials.

[0048] As shown in Fig. 1 and Fig. 2, in the present embodiment, the element layer 120 of the pixel array substrate 100 further includes a second peripheral line L2. As shown in Fig. 2, the second peripheral line L2 is configured on the first substrate 110 and is located on a second side S2 of the pixel structures PX, and the second common lines CL2 are electrically connected to the second peripheral line L2.

[0049] In the present embodiment, an end of each of the second common lines CL2 being close to the second peripheral line L2 is electrically connected to the second peripheral line L2, and the other end of each of the second common lines CL2 being remote from the second peripheral line L2 may be separated from the first peripheral line L1 selectively, but the disclosure is not limited thereto.

[0050] As shown in Fig. 2, each of the first gate lines HG is electrically connected to n number of the second gate lines VG, in which n is a positive integer, and each of the first gate lines HG and the n number of the second gate lines VG have the 1st to nth connection points (or contact points) C arranged in sequence in the first direction D1. And the second gate lines VG include the 1st to nth second line groups Gvg arranged in sequence in the first direction D1, and the second gate lines VG of the mth second gate line group Gvg of the 1st to nth second gate line groups Gvg and the corresponding first gate lines HG have the mth connection point C of the 1st to nth connection points C, in which m is a positive integer, and $n \geq m \geq 1$.

[0051] For example, in the present embodiment, $n=3$; thus, each of the first gate lines HG is electrically connected to three corresponding second gate lines VG, and each of the first gate lines HG and the three corresponding second gate lines VG have the 1st to 3rd connection points C1, C2, and C3 arranged in sequence in the first direction D1. And the second gate lines VG include the 1st

to 3rd second gate line groups Gvg1, Gvg2, and Gvg3 arranged in sequence in the first direction D1, in which the second gate lines VG1 to VG6 of the first second gate line group Gvg1 and the corresponding first gate lines HG1 to HG6 have the 1st connection points C1, the second gate lines VG1 to VG6 of the 2nd second gate line group Gvg2 and the corresponding first gate lines HG1 to HG6 have the 2nd connection points C2, and the second gate lines VG1 to VG6 of the 3rd second gate line group Gvg3 and the corresponding first gate lines HG1 to HG6 have the 3rd connection points C3.

[0052] Fig. 3 is a schematic top view of an opposite substrate 200, a plurality of first transfer elements T1, a plurality of second transfer elements T2, and a third transfer element T3 according to an embodiment of the disclosure.

[0053] As shown in Fig. 1 and Fig. 3, in the present embodiment, the opposite substrate 200 of the display apparatus 10 may include selectively a common electrode 220, in which the common electrode 220 is configured on the second substrate 210 and is located between the second substrate 210 and the display medium 300. As shown in Fig.2 and Fig. 3, in the present embodiment, the common electrode 220 is a wall-shaped electrode which overlaps all the pixel structures PX, but the disclosure is not limited hereto.

[0054] In the present embodiment, the common electrode 220 may be, for example, a transparent conductive layer which includes metal oxides, such as indium tin oxide, indium zinc oxide, aluminum tin oxide, aluminum zinc oxide, indium germanium zinc oxide, or other suitable oxides, or a stacked layer of at least two of the above, but the disclosure is not limited thereto.

[0055] As shown in Fig. 1 and Fig. 2, in the present embodiment, the element layer 120 of the pixel array substrate 100 further includes a plurality of common pad groups Gp1a, Gp1b, and Gp1c as well as n number of a plurality of second common pads p2a, p2b, and p2c. As shown in Fig. 2, the common pad groups Gp1a, Gp1b, and Gp1c are configured on the first substrate 110, and are configured to correspond respectively to the 1st to nth second gate line groups Gvg1, Gvg2, and Gvg3,

and are located on the second side S2 of the pixel structures PX. Each of the common pad groups Gp1a, Gp1b, and Gp1c include a plurality of first common pads p1a, p1b, and p1c which are structurally separated. And the n number of the second common pads p2a, p2b, and p2c are configured on the first substrate 110, and are configured to correspond respectively to the 1st to nth second gate line groups Gvg1, Gvgl2, and Gvgl3, and are located on the first side S1 of the pixel structures PX.

[0056] For example in the present embodiment, n=3; thus, the pixel array substrate 100 includes three common pad groups Gp1a, Gp1b, and Gp1c as well as three second common pads p2a, p2b, and p2c. The three common pad groups Gp1a, Gp1b, and Gp1c are configured to correspond to the 1st to 3rd second gate line groups Gvg1, Gvgl2, and Gvgl3, and are located on the second side S2 of the pixel structures PX. The three second common pads p2a, p2b, and p2c are configured on the first substrate 110, and are configured to correspond respectively to the 1st to 3rd second gate line groups Gvg1, Gvgl2, and Gvgl3, and are located on the first side S1 of the pixel structures PX.

[0057] In the present embodiment, the first common pads p1a of the same common pad group Gp1a are dispersed on one side of the second gate lines VG1 to VG6 of the corresponding second gate line group Gvg1; the second common pad p2a which corresponds to the second gate line group Gvg1 is configured on the other side of the second gate lines VG1 to VG6 of the second gate line group Gvg1; and, the second common pad p2a may be located next to the longest second gate line VG6 of the second gate line group Gvg1.

[0058] As shown in Fig. 1, Fig. 2, and Fig. 3, in the present embodiment, the display apparatus 10 further includes the first transfer elements T1 which are configured between the element layer 120 of the pixel array substrate 100 and the common electrode 220 of the opposite substrate 200. The first transfer elements T1 are configured respectively on the first common pads p1a, p1b, and p1c of the common pad groups Gp1a, Gp1b, and Gp1c, and are electrically connected to the first common pads p1a, p1b, and p1c and a first part 221 of the common electrode 220.

[0059] In the present embodiment, the display apparatus 10 further includes n number of the second transfer elements T2 which are configured between the element layer 120 of the pixel array substrate 100 and the common electrode 220 of the opposite substrate 200. And the n number of the second transfer elements T2 are configured respectively on the n number of the second common pads p2a, p2b, and p2c, and are electrically connected to the n number of the second common pads p2a, p2b, and p2c and a second part 222 of the common electrode 220.

[0060] In the present embodiment, the common pad group Gp1a and the second common pad p2a correspond to the same second gate line group Gvg1, and the potential of the second common pad p2a is greater than the potentials of the first common pads p1a of the common pad group Gp1a. By doing so, a potential distribution forms between the first part 221 and the second part 222 of the common electrode 220 which are electrically connected respectively to the first transfer element T1 configured on the first common pad p1a and the second transfer element T2 configured on the second common pad p2a. The potential distribution may compensate for the difference in brightness caused by the different impedances of the second gate lines VG1 to VG6 of the second gate line group Gvg1.

[0061] In the present embodiment, the first common pads p1a, p1b, and p1c are electrically connected to a drive element (not illustrated) respectively through a plurality of wires Lp1a, Lp1b, and Lp1c, and the second common pads p2a, p2b, and p2c are electrically connected to a drive element (not illustrated) respectively through a plurality of wires Lp2a, Lp2b, and Lp2c, and the wires Lp1a, Lp1b, Lp1c, Lp2a, Lp2b, and Lp2c are structurally separated from each other. In other words, the potentials of the first common pads p1a, p1b, and p1c and the second common pads p2a, p2b, and p2c may be controlled independently. The magnitude of the potentials of the first common pads p1a, p1b, and p1c and the second common pads p2a, p2b, p2c may be adjusted according to actual needs.

[0062] As shown in Fig. 1 and Fig. 2, in the present embodiment, the element layer 120 of the pixel array substrate 100 further includes a third common pad p3. As shown in Fig. 2, the third common

pad p3 is configured on the first substrate 110, and is located on the first side S1 of the pixel structures PX. The third common pad p3 and the second common pads p2a, p2b, and p2c are arranged in sequence in the first direction D1 and are structurally separated from each other. The third common pad p3 is configured to correspond to the 1st second gate line group Gvg1. And the potential of the third common pad p3 is greater than the potentials of the second common pads p2a, p2b, and p2c. In the present embodiment, the potential of the third common pad p3 is also greater than the potentials of the first common pads p1a, p1b, and p1c. For example, the potential difference between the third common pad p3 and any one of the first common pads p1a, p1b, and p1c may be 1 volt or more, but the disclosure is not limited thereto.

[0063] As shown in Fig. 1, Fig. 2, and Fig. 3, in the present embodiment, the display apparatus 10 further includes the third transfer elements T3 which is configured between the element layer 120 of the pixel array substrate 100 and the common electrode 220 of the opposite substrate 200. The third transfer element T3 is configured on the third common pad p3, and is electronically connected to the third common pad p3 and a third part 223 of the common electrode 220.

[0064] In the present embodiment, the third common pad p3 is electrically connected to the drive element through a wire Lp3, and the wire Lp3 are structurally separated from the wires Lp1a, Lp1b, Lp1c, Lp2a, Lp2b, and Lp2c which are electrically connected to the first common pads p1a, p1b, and p1c and the second common pads p2a, p2b, and p2c. In other words, the potential of the third common pad p3 may be controlled independently. And the magnitude of the potential of the third common pad p3 may be adjusted according to actual needs.

[0065] In the present embodiment, the first transfer element T1, the second transfer element T2, and the third transfer element T3 include a conductive ball (for example, a gold ball), but the disclosure is not limited thereto.

[0066] It is to be noted that the following embodiments use the reference numerals and a part of the contents of the above embodiments, and the same reference numerals are used to denote the same

or similar elements, and the description of the same technical contents is omitted. For the description of the omitted part, reference may be made to the above embodiments, and its details are not described in the following embodiments.

[0067] Fig. 4 is a schematic top view of a pixel array substrate 100A, a plurality of first transfer elements T1, a plurality of second transfer elements T2, and a third transfer element T3 according to an embodiment of the disclosure.

[0068] The pixel array substrate 100A of Fig. 4 is similar to the pixel array substrate 100 of Fig. 2. The difference between the two is that in the embodiment of Fig. 4, both ends of each second common line CL2 may be electrically connected to a first peripheral line L1 and a second peripheral line L2.

[0069] As shown in Fig. 4, in the present embodiment, a signal input to the first peripheral line L1 and a signal input to the second peripheral line L2 may be controlled independently. Specifically speaking, the first peripheral line L1 and the second peripheral line L2 are electrically connected to the drive element through respective wire L11 and wire L12, and the wire L11 and wire L12 are structurally separated from each other. For example, in the present embodiment, a signal input to the first peripheral line L1 and a signal input to the second peripheral line L2 may be selectively the same. For example, a signal input to the first peripheral line L1 and a signal input to the second peripheral line L2 may both be the same with a gate-close signal of a plurality of second gate lines VG. However, the disclosure is not limited thereto. In other embodiments, a signal input to the first peripheral line L1 and a signal input to the second peripheral line L2 may also be different.

[0070] Fig. 5 is a schematic top view of a pixel array substrate 100B and a plurality of first transfer elements T1 according to an embodiment of the disclosure.

[0071] The pixel array substrate 100B of Fig. 5 is similar to the pixel array substrate 100 of Fig. 2. The difference between the two is that in the embodiment of Fig. 2, n is 3, that is, each of the first gate lines HG are electrically connected to three second gate lines VG. However, in the embodiment of Fig. 5, n is 4, that is, each of a plurality of first gate lines HG is electrically connected to four

second gate lines VG. However, the disclosure is not limited thereto. The number (i.e., n) of the second gate lines VG electrically connected to each of the first gate lines HG may be determined according to actual needs.

[0072] Specifically speaking, the pixel structures PX are arranged in x number of pixel columns Cpx and y number of pixel rows Rpx, in which the x number of the pixel columns Cpx are arranged in a first direction D1 and y number of pixel rows Rpx are arranged in a second direction D2. In the above arrangement, x and y are positive integers greater than 2. Each pixel structure PX has a first width a1 and a second width a2 respectively in the first direction D1 and the second direction D2. The first width a1 may refer to the following distances: the distance between two adjacent second gate lines VG located respectively on the left and right sides of the same pixel structure PX, the distance between a second gate line VG and a first common line CL1 which are adjacent to each other and located respectively on the left and right sides of the same pixel structure PX, the distance between two adjacent first common lines CL1 located on the left and right sides of the same pixel structure PX, the distance between a first common line CL1 and a second common line CL2 adjacent to each other and located respectively on the left and right sides of the same pixel structure PX, or the distance between a second gate line VG and a second common line CL2 which are adjacent to each other and located respectively on the left and right sides of the same pixel structure PX. The second width a2 may refer to the distance between two adjacent first gate lines HG located on the upper and lower sides of the same pixel structure PX. If $(a1 \cdot x + a2 \cdot y) < 2000000$, then n is preferably equal to 2. If $2000000 < (a1 \cdot x + a2 \cdot y) < 2400000$, then n is preferably equal to 3. If $2400000 < (a1 \cdot x + a2 \cdot y) < 3000000$, then n is preferably equal to 4. If $(a1 \cdot x + a2 \cdot y) > 3000000$, then n is preferably equal to 5.

[0073] Fig. 6 is a schematic top view of a pixel array substrate 100C and a plurality of first transfer elements T1 according to an embodiment of the disclosure.

[0074] The pixel array substrate 100C of Fig. 6 is similar to the pixel array substrate 100 of Fig. 2.

The difference between the two is that the methods of connecting the second gate lines VG and the first gate lines HG are different.

[0075] As shown in Fig. 6, specifically speaking, in the present embodiment, a plurality of first gate lines HG are arranged in sequence in a second direction D2, and the first gate lines HG include an odd number of the first gate lines HG and an even number of the first gate lines HG. The odd number of the first gate lines HG include the $(1+2\cdot K)^{\text{th}}$ first gate line HG, in which $K=0, 1, \dots, p$, and p is a positive integer greater than or equal to 2. The even number of the first gate lines HG include the $2L^{\text{th}}$ first gate line HG, in which $L=1, 2, \dots, q$, and q is a positive integer greater than or equal to 3. The second gate lines VG include the 1^{st} to $(p+1)^{\text{th}}$ second gate lines VG and the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines VG arranged in sequence in the first direction D1. The 1^{st} to $(p+1)^{\text{th}}$ second gate lines VG are electrically connected respectively to the $(1+2\cdot K)^{\text{th}}$ first gate line HG, and the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines VG are electrically connected respectively to the $2L^{\text{th}}$ first gate line HG.

[0076] For example, in the present embodiment, $p=2$, $K=0, 1$, and 2 , and the odd number of the first gate lines HG include the 1st, 3rd, and 5th first gate lines HG1, HG3, and HG5; $q=3$, $L=1, 2$, and 3 , the even number of the first gate lines HG include the 2nd, 4th, and 6th first gate lines HG2, HG4, and HG6; the second gate lines VG include the 1^{st} to 3^{rd} second gate lines VG1 to VG3 and the 4th to 6th second gate lines VG4 to VG6 arranged in sequence in the first direction D1; the 1^{st} to 3^{rd} second gate lines VG1 to VG3 are electronically connected respectively to the 1^{st} , 3^{rd} , and 5^{th} first gate lines HG1, HG3, and HG5, and the 4^{th} to 6^{th} second gate lines VG4 to VG6 are electrically connected respectively to the 2^{nd} , 4^{th} , and 6^{th} gates lines HG2, HG4, and HG6. In other words, in the present embodiment, the connection points C of the second gate lines VG from the same second gate line group Gvg and the first gate lines HG (for example: the connection points C of the 1^{st} to 3^{rd} second gate lines VG1 to VG3 and the 1^{st} , 3^{rd} , and 5^{th} first gate lines HG1, HG3, and HG5, and the connection points C of the 4^{th} to 6^{th} second gate lines VG4 to VG6 and the 2^{nd} , 4^{th} , and 6^{th} of the first

gate lines HG2, HG4, and HG6) may be distributed generally along multiple diagonal lines K that are parallel to each other.

[0077] Fig. 7 is a schematic top view of a pixel array substrate 100D and a plurality of first transfer elements T1 according to an embodiment of the disclosure.

[0078] The pixel array substrate 100D of Fig. 7 is similar to the pixel array substrate 100 of Fig. 2. The difference between the two is that the methods of connecting the second gate lines VG and the first gate lines HG are different.

[0079] As shown in Fig. 7, specifically speaking, in the present embodiment, a plurality of first gate lines HG are arranged in sequence in a second direction D2, and the first gate lines HG include an odd number of first gate lines HG and an even number of first gate lines HG. The odd number of the first gate lines HG include the $(1+2\cdot K)^{\text{th}}$ first gate line HG, in which $K=0, 1, \dots, p$, and p is a positive integer greater than or equal to 2. The even number of the first gate lines HG include the $2L^{\text{th}}$ first gate line HG, in which $L=1, 2, \dots, q$, and q is a positive integer greater than or equal to 3. The second gate lines VG include the 1^{st} to $(p+1)^{\text{th}}$ second gate lines VG and the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines VG arranged in sequence in the first direction D1. The 1^{st} to $(p+1)^{\text{th}}$ second gate lines VG are electrically connected respectively to the $(1+2\cdot K)^{\text{th}}$ first gate lines HG, and the $(p+1)$ to $(p+q+1)^{\text{th}}$ second gate lines VG are electrically connected respectively to the $2L^{\text{th}}$ first gate line HG.

[0080] For example, in the present embodiment, $p=2$, $K=0, 1$, and 2 , and the odd number of the first gate lines HG include the 1^{st} , 3^{rd} , and 5^{th} first gate lines HG1, HG3, and HG5; $q=3$, $L=1, 2$, and 3 , the even number of the first gate lines HG include the 2^{nd} , 4^{th} , and 6^{th} first gate lines HG2, HG4, and HG6; the second gate lines VG include the 1^{st} to 3^{rd} second gate lines VG1 to VG3 and the 4^{th} to 6^{th} second gate lines VG4 to VG6 arranged in sequence in the first direction D1; the 1^{st} to 3^{rd} second gate lines VG1 to VG3 are electronically connected respectively to the 1^{st} , 3^{rd} , and 5^{th} first gate lines HG1, HG3, and HG5, and the 6^{th} to 4^{th} second gate lines VG6 to VG4 are electrically connected respectively to the 2^{nd} , 4^{th} , and 6^{th} first gates lines HG2, HG4, and HG6. In other words, in the

present embodiment, a plurality of connection points C of the second gate lines VG from the same second gate line group Gvg and the first gate lines HG (for example, the connection points C of the 1st to 3rd second gate lines VG1 to VG3 and the 1st, 3rd, and 5th first gate lines HG1, HG3, and HG5, and the connection points C of the 6th to 4th second gate lines VG6 to VG4 and the 2nd, 4th, and 6th of the first gate lines HG2, HG4, and HG6) are distributed generally in a V-shaped pattern.

WHAT IS CLAIMED IS:

1. A display apparatus, comprising:

a first substrate;

a plurality of data lines, configured on the first substrate and arranged in a first direction;

a plurality of first gate lines, configured on the first substrate, and arranged in a second direction, wherein the first direction crisscrosses the second direction;

a plurality of pixel structures, configured on the first substrate and electrically connected to the data lines and the first gate lines;

a plurality of second gate lines, configured on the first substrate, wherein the data lines and the second gate lines are arranged in the first direction, and the second gate lines are electrically connected to the first gate lines;

a plurality of first common lines, configured on the first substrate, wherein the pixel structures are arranged in a plurality of pixel columns, the pixel columns are arranged in the first direction, each of the first common lines and the corresponding second gate line are configured between two adjacent pixel columns of the pixel columns, the first common line and the corresponding second gate line are configured respectively on the opposite sides of the first gate line which is electrically connected to the second gate line, and the first common line and the corresponding second gate line are structurally separated;

a second substrate, configured to be opposite to the first substrate; and

a display medium, configured between the first substrate and the second substrate.

2. The display apparatus according to claim 1, wherein a signal of the first common line and a gate-off signal of the second gate line are substantially the same.

3. The display apparatus according to claim 1, wherein each of the first gate lines is electrically connected to n number of the second gate lines, n is a positive integer, each of the first gate lines and the n number of the second gate lines have 1st to nth connection points arranged in

sequence in the first direction, the second gate lines include 1st to nth second gate line groups arranged in sequence in the first direction, the second gate lines of mth second gate line group of the 1st to nth second gate line groups and the corresponding first gate lines have mth connection point of the 1st to nth connection points, m is a positive integer, and $n \geq m \geq 1$, and the display apparatus further comprising:

a common electrode, configured on the second substrate and located between the second substrate and the display medium;

a plurality of common pad groups, configured on the first substrate, and configured to correspond respectively to the 1st to nth second gate line groups, wherein the pixel structures have a first side and a second side opposite to each other, the common pad groups are configured on the second side of the pixel structures, and each of the common pad groups includes a plurality of first common pads;

a plurality of first transfer elements, configured respectively on the first common pads of the common pad groups, and electrically connected to the first common pads of the common pad groups and the common electrode;

n number of a plurality of second common pads, configured on the first substrate, and configured to correspond respectively to the 1st to nth second gate line groups, and located on the first side of the pixel structures; and

n number of a plurality of second transfer elements, configured respectively on the n number of the second common pads, and electrically connected to the n number of the second common pads and the common electrode,

wherein a common pad group of the common pad groups and a second common pad of the n number of the second common pads correspond to the same second gate line group, and a potential of the second common pad is greater than a plurality of potentials of the first common pads of the common pad group.

4. The display apparatus according to claim 3, further comprising:

a third common pad, configured on the first substrate, and located on the first side of the pixel structures, wherein the third common pad and the second common pads are arranged in sequence in the first direction and are structurally separated from each other, the third common pad is configured to correspond to the 1st second gate line group of the 1st to nth second gate line groups, and a potential of the third common pad is greater than a plurality of potentials of the corresponding second common pads; and

a third transfer element, configured on the third common pad, and electrically connected to the third common pad and the common electrode.

5. The display apparatus according to claim 1, further comprising:

a plurality of second common lines, configured on the first substrate, and the second gate lines and the second common lines are arranged in the first direction, wherein each of the second common lines is configured between two adjacent pixel columns of the pixel columns;

a first peripheral line, configured on the first substrate and located on a first side of the pixel structures, wherein the first common lines are electrically connected to the first peripheral line; and

a second peripheral line, configured on the first substrate and located on a second side of the pixel structures, wherein two ends of each of the second common lines are electrically connected respectively to the first peripheral line and the second peripheral line.

6. The display apparatus according to claim 1, wherein the first gate lines include an odd number of the first gate lines and an even number of the first gate lines, the odd number of the first gate lines include $(1+2\cdot K)^{\text{th}}$ first gate line, $K=0, 1, \dots, p$, and p is a positive integer greater than or equal to 2, the even number of the first gate lines include $2L^{\text{th}}$ first gate line, $L=1, 2, \dots, q$, and q is a positive integer greater than or equal to 3; the second gate lines include 1st to $(p+1)^{\text{th}}$ second gate lines and $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines arranged in sequence in the first

direction; the 1st to (p+1)th second gate lines are electrically connected to the (1+2·K)th first gate line, and the (p+2) to (p+q+1)th second gate lines are electrically connected to the 2Lth first gate line.

7. The display apparatus according to claim 6, wherein a plurality of connection points of the 1st to (p+1)th second gate lines and the (1+2·K)th first gate line as well as a plurality of connection points of the (p+2) to (p+q+1)th second gate lines and the 2Lth first gate line are generally distributed along a plurality of diagonal lines parallel to each other.

8. The display apparatus according to claim 6, wherein a plurality of connection points of the 1st to (p+1)th second gate lines and the (1+2·K)th first gate line as well as a plurality of connection points of the (p+2) to (p+q+1)th second gate lines and the 2Lth first gate line are distributed generally in a V-shaped pattern.

9. A display apparatus, comprising:

a first substrate;

a plurality of data lines, configured on the first substrate and arranged in a first direction;

a plurality of first gate lines, configured on the first substrate, and arranged in a second direction, wherein the first direction crisscrosses the second direction;

a plurality of pixel structures, configured on the first substrate, electrically connected to the data lines and the first gate lines, and arranged in x number of pixel columns and y number of pixel rows, wherein the x number of pixel columns are arranged in the first direction, the y number of pixel rows are arranged in the second direction, and x and y are positive integers greater than 2;

a plurality of second gate lines, configured on the first substrate, wherein the data lines and the second gate lines are arranged in the first direction, and the second gate lines are electrically connected to the first gate lines;

a plurality of first common lines, configured on the first substrate;

a second substrate, configured to be opposite to the first substrate; and

a display medium, configured between the first substrate and the second substrate,

wherein each of the first common lines and the corresponding second gate line are configured between two adjacent pixel columns of the x number of the pixel columns, the first common line and the corresponding second gate line are configured respectively on the opposite sides of the first gate line which is electrically connected to the second gate line, and the first common line and the corresponding second gate line are structurally separated; and

wherein each of the first gate lines is electronically connected to n number of the second gate lines.

10. The display apparatus according to claim 9, wherein a signal of the first common line and a gate-off signal of the second gate line are substantially the same.

11. The display apparatus according to claim 9, wherein each of the first gate lines is electrically connected to the n number of the second gate lines, n is a positive integer, each of the first gate lines and the n number of the second gate lines have 1st to nth connection points arranged in sequence in the first direction, the second gate lines include 1st to nth second gate line groups arranged in sequence in the first direction, and the second gate lines of mth second gate line group of the 1st to nth second gate line groups and the corresponding first gate lines have mth connection point of the 1st to nth connection points, m is a positive integer, and $n \geq m \geq 1$, and the display apparatus further comprising:

a common electrode, configured on the second substrate and is located between the second substrate and the display medium;

a plurality of common pad groups, configured on the first substrate, and configured to correspond respectively to the 1st to nth second gate line groups, wherein the pixel structures have a first side and a second side opposite to each other, the common pad groups are configured on the

second side of the pixel structures, and each of the common pad groups includes a plurality of first common pads;

a plurality of first transfer elements, configured respectively on the first common pads of the common pad groups, and electrically connected to the first common pads of the common pad groups and the common electrode;

n number of a plurality of second common pads, configured on the first substrate, configured to correspond respectively to the 1st to nth second gate line groups, and located on the first side of the pixel structures; and

n number of a plurality of second transfer elements, configured respectively on the n number of the second common pads, and electrically connected to the n number of the second common pads and the common electrode,

wherein a common pad group of the common pad groups and a second common pad of the n number of the second common pads correspond to the same second gate line group, and a potential of the second common pad is greater than a plurality of potentials of the first common pads of the common pad group.

12. The display apparatus according to claim 11, further comprising:

a third common pad, configured on the first substrate, and located on the first side of the pixel structures, wherein the third common pad and the second common pads are arranged in sequence in the first direction and are structurally separated from each other, the third common pad is configured to correspond to the 1st second gate line group of the 1st to nth second gate line groups, and a potential of the third common pad is greater than a plurality of potentials of the corresponding second common pads; and

a third transfer element, configured on the third common pad, and electrically connected to the third common pad and the common electrode.

13. The display apparatus according to claim 9, further comprising:

a plurality of second common lines, configured on the first substrate, and the second gate lines and the second common lines are arranged in the first direction, wherein each of the second common lines is configured between two adjacent pixel columns of the pixel columns;

a first peripheral line, configured on the first substrate and located on a first side of the pixel structures, wherein the first common lines are electrically connected to the first peripheral line; and

a second peripheral line, configured on the first substrate and located on a second side of the pixel structures, wherein two ends of each of the second common lines are electrically connected respectively to the first peripheral line and the second peripheral line.

14. The display apparatus according to claim 9, wherein the first gate lines include an odd number of the first gate lines and an even number of the first gate lines, the odd number of the first gate lines include $(1+2\cdot K)^{\text{th}}$ first gate line, $K=0, 1, \dots, p$, and p is a positive integer greater than or equal to 2, the even number of the first gate lines include $2L^{\text{th}}$ first gate line, $L=1, 2, \dots, q$, and q is a positive integer greater than or equal to 3; the second gate lines include 1^{st} to $(p+1)^{\text{th}}$ second gate lines and $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines arranged in sequence in the first direction; the 1^{st} to $(p+1)^{\text{th}}$ second gate lines are electrically connected to the $(1+2\cdot K)^{\text{th}}$ first gate line, and the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines are electrically connected to the $2L^{\text{th}}$ first gate line.

15. The display apparatus according to claim 14, wherein a plurality of connection points of the 1^{st} to $(p+1)^{\text{th}}$ second gate lines and the $(1+2\cdot K)^{\text{th}}$ first gate line as well as a plurality of connection points of the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines and the $2L^{\text{th}}$ first gate line are generally distributed along a plurality of diagonal lines parallel to each other.

16. The display apparatus according to claim 14, wherein a plurality of connection points of the 1^{st} to $(p+1)^{\text{th}}$ second gate lines and the $(1+2\cdot K)^{\text{th}}$ first gate line as well as a plurality of connection

points of the $(p+2)$ to $(p+q+1)^{\text{th}}$ second gate lines and the $2L^{\text{th}}$ first gate line are distributed generally in a V-shaped pattern.