WHAT IS CLAIMED IS:

1. A data processing circuit, comprising:

a first bank group and a second bank group;

a write circuit comprising a write input cache circuit, the write circuit being configured to: receive stored data from a write bus through the write input cache circuit, write the stored data into the first bank group through a first read-write bus, and write the stored data into the second bank group through a second read-write bus; and

a read circuit comprising a read output cache circuit, the read circuit being configured to: read the stored data from the first bank group through the first read-write bus, read the stored data from the second bank group through the second read-write bus, and transmit the stored data to a read bus through the read output cache circuit;

wherein the write circuit further comprises:

a write control circuit, respectively connected to the write input cache circuit, a first write output cache circuit and a second write output cache circuit, the write control circuit being configured to transmit the stored data transmitted by the write input cache circuit to the first write output cache circuit or the second write output cache circuit;

the first write output cache circuit connected to the first bank group and configured to transmit the stored data transmitted by the write control circuit to the first bank group; and

the second write output cache circuit connected to the second bank group and configured to transmit the stored data transmitted by the write control circuit to the second bank group;

wherein the write input cache circuit is configured to receive the stored data through a first control signal, and a frequency of the first control signal being same as a clock frequency configured for writing the stored data;

wherein the first write output cache circuit is configured to write the stored data into the first bank group through a second control signal, the second write output cache circuit being configured to write the stored data into the second bank group through a third control signal, a frequency of the second control signal and a frequency of the third control signal both being a half of the frequency of the first control signal, and a falling edge of the second control signal and a falling edge of the third control signal alternating.

2. A data processing circuit, comprising:

a first bank group and a second bank group;

a write circuit comprising a write input cache circuit, the write circuit being configured to: receive stored data from a write bus through the write input cache circuit, write the stored data into the first bank group through a first read-write bus, and write the stored data into the second bank group through a second read-write bus; and

a read circuit comprising a read output cache circuit, the read circuit being configured to: read the stored data from the first bank group through the first read-write bus, read the stored data from the second bank group through the second read-write bus, and transmit the stored data to a read bus through the read output cache circuit;

wherein read circuit comprises:

a first read input cache circuit, connected to the first bank group and configured to read the stored data from the first bank group;

a second read input cache circuit, connected to the second bank group and configured to read the stored data from the second bank group; and

a read control circuit respectively connected to the first read input cache circuit and the second read input cache circuit, the read control circuit being configured to transmit the stored data transmitted by the first read input cache circuit or the second read input cache circuit to the read output cache circuit;

wherein the first read input cache circuit is configured to read the stored data through a fourth control signal, the second read input cache circuit being configured to read the stored data through a fifth control signal, a frequency of the fourth control signal being same as that of the fifth control signal, and a falling edge of the fourth control signal and a falling edge of the fifth control signal alternating;

wherein the read output cache circuit is configured to transmit the stored data to the read bus through a sixth control signal, a frequency of the sixth control signal being twice that of the fourth control signal.

3. The data processing circuit according to claim 1 or 2, wherein the first read-write bus and the second read-write bus are arranged crosswise.

4. The data processing circuit according to claim 3, wherein the first read-write bus comprises a first sub-bus with a plurality of bits, the second read-write bus comprising a second sub-bus with a plurality of bits, and the first sub-bus and the second sub-bus corresponding to the same bit extending to a same height and being connected to the first bank group and the second bank group, respectively.

5. The data processing circuit according to claim 1 or 2, wherein the write circuit and the read circuit are arranged in parallel on a first straight line, the first bank group and the second bank group being arranged in parallel on a second straight line, and the first straight line being parallel to the second straight line.

6. The data processing circuit according to claim 5, wherein a first region where the write circuit and the read circuit are positioned and a second region where the first bank group and the second bank group are positioned are arranged in parallel on a third straight line, the third straight line being perpendicular to the first straight line.

7. The data processing circuit according to claim 1 or 2, wherein the first bank group and the second bank group are different in data read-write time, the first bank group being same as the second bank group in data read-write logic.

8. A memory, comprising two data processing circuits according to any one of claims 1 to 7, write circuits in the two data processing circuits being connected to same write bus, and read circuits in the two data processing circuits being connected to same read bus.

9. The memory according to claim 8, wherein the memory is a double data rate dynamic random access memory DDR DRAM.

10. The memory according to claim 8 or 9, wherein write circuits and read circuits of the two data processing circuits are positioned in a central region, the first bank group and the

second bank group of one of the two data processing circuits being positioned on a side of the central region, and the first bank group and the second bank group of other one of the two data processing circuits being positioned on another side of the central region.

11. An electronic device, comprising the memory according to any one of claims 8 to 10.