"Semiconductor Integrated Circuit Device".

The present invention relates to a semiconductor integrated circuit device and, more particularly, to a semiconductor integrated circuit device having a digital signal processing circuit and an analog signal processing circuit.

It may be desired to make a semiconductor integrated circuit device such as a device constituting a digital controller capable of processing an analog signal as well as a digital signal. since the analog signal usually has a relatively large quantity of information, the use of the semiconductor integrated circuit device capable of processing the analog signal is beneficial for a highly precise process control. In the semiconductor integrated circuit device, a multi-layer wiring such as a double layer wiring or a triple layer wiring can be effected by the well-known multi-layer wiring technique with a view to improving the integration density. In this case, the semiconductor integrated circuit device has its internal circuits or circuit elements connected with each other or one another through the multi-layer wiring.

In the case where the digital signal processing circuit and the analog signal processing circuit are formed into a single semiconductor integrated circuit device, although not limitative, a first wiring layer made of a conductive polysilicon layer formed on a semiconductor substrate through a field insulating film may be used as an analog signal line, and a second wiring layer made of an aluminium layer formed on the first wiring layer through an inter-layer insulating film may be used as a digital signal line.

However, the interlayer insulating film, which is formed in the semiconductor integrated circuit, has a relatively small thickness. Therefore, it should be noted that a relatively high capacitance is established in a portion in which the two wiring layers intersect. The undesirable capacity to be formed between the wiring layers establishes such a crosstalk as will adversely affect the circuit operations.

Especially in the case where the analog signal line is connected with an electronic circuit having a high input impedance such as an analog/digital (A/D) converter, the crosstalk to be imparted from the digital signal line to the analog signal line through the electrostatic coupling is increased. A malfunction is caused in the analog signal

processing operation by the undesired fluctuations of the analog signal level. More specifically, when the level of the digital signal is changed, this level change is transmitted through the above referred to capacitance to the analog signal line in order to thereby change the level of the analog signal. As a result, a malfunction takes place in the A/D converter.

In the case of such a circuit as is disclosed in our copending Japanese Patent Application No. 55 - 18986 i.e. in the case where a common external terminal is selectively used as an analog input terminal or a digital input/output terminal, the above referred to crosstalk is substantially increased.

It is an object of the present invention to provide a semiconductor integrated circuit device which will reduce the undesirable crosstalk to be imparted toan analog signal circuit.

According to the present invention there is provided a semiconductor integrated circuit device including:

(a) an analog signal transmission link formed on a semiconductor substrate in a first prescribed geometrical pattern;

(b) a first prescribed, analog signal-handling, electronic circuit formed on said substrate and coupled to said analog signal transmission link so that analog signals may be exchanged between said first prescribed

circuit and said analog signal transmission link;

(c) a digital signal transmission link comprised of a plurality of digital signal conveying paths and formed on said substrate in a second prescribed geometrical pattern separated from said first prescribed geometrical pattern so as not to overlap said first pattern;

(d) a second prescribed, digital signal-handling, electronic circuit formed on said substrate and coupled to said digital signal transmission link so that digital signals may be exchanged between said second prescribed circuit and said digital signal transmission link;

(e) a plurality of bonding pad electrodes arranged on said substrate at positions adjacent to and separating respective ones of said digital signal conveying paths from said analog signal transmission link;

(f) first means for coupling respective ones of said digital signal conveying paths to said plurality of bonding pad electrodes; and

(g) second means for selectively coupling selected ones of said bonding pad electrodes to said analog signal transmission link.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings wherein:-

Figure 1 is a block diagram showing one preferred form of semiconductor integrated circuit device, and an electronic device coupled thereto;

Figure 2 is a circuit diagram showing in detail a portion of the micro-processor contained in the circuit block shown in Figure 1;

Figure 3 is a top plan view showing the pattern of the semiconductor integrated circuit device for the embodiment shown in Figure 1;

Figure 4 is a section taken along line A-A' of Figure 3; and

Figure 5 is a section taken along line B-B' of Figure 3.

Referring first to Figure 1, circuit blocks 2 to 18 together constitute a micro-processor 1. This micro-processor 1 is formed as a monolithic semiconductor integrated circuit on a semiconductor chip. The respective circuit blocks include MSIFETs (i.e. insulated gate field effect transistors) which are formed on a semiconductor substrate by a well-known

semiconductor integrated circuit technique.

An accumulator 2, an accumulator latch 3, a temporary register 4 and an arithmetic logic unit 5 together constitute an arithmetic unit.

The arithmetic logic unit 5 performs either the arithmetic operation such as addition or subtraction or the logic judgement such as a logic sum (OR), a logic product (AND) or an exclusive logic sum, and has its operation controlled by the controller 8. The information generated by the temporary register 4 and the information generated by the accumulator latch 3 made receptive of the output of the accumulator 2 are calculated by the arithmetic logic unit 5. When a suitable control signal is provided from the control circuit 8 on the basis of an instruction, the arithmetic result output from the arithmetic logic unit 5 is fed through an internal data bus BUS to a suitable circuit corresponding to the aforementioned control instruction. The arithmetic result is fed out through the internal data bus BUS to the accumulator 2, for example.

An instruction register 6, an instruction decoder and machine cycle encoder 7 and the timing controller 8 together constitute a control unit.

The instruction register 6 is provided to receive the program instruction which is written in a ROM (Read Only Memory) 19 or a RAM (Random Access

Memory) 20. The instruction received by the instruction register 6 is encoded by the instruction decoder in the circuit 7. The machine cycle encoder in the circuit 7 generates a variety of timing signals on the basis of the signal generated by the instruction decoder. Namely, the program instruction is converted into the various timing signals by the circuit 7.

The timing control circuit 8 generates both a bus control signal for feeding an input/output port 11 with the data, which are fed to an external data bus DT, and a strobe signal for reading out the data, which are to be supplied to the external data bus DT, to the input/out port 11. The output timings of these signals are determined in accordance with the clock signal which is supplied to the timing control circuit 8 through a group of external control terminals CONT. Moreover, the timing control circuit 8 receives a series of external input signals such as an interruption signal, a hold signal for stopping the circuit operation or a reset signal through the grouped external control terminals CONT. Upon reception of those external input signals, the timing control circuit 8 outputs a series of signals such as a signal indicative of the reception of the interruption or a signal indicative of the reception of the demand of the hold to the outside.

A register unit 9 is formed from a number of

registers such as a working register for general use, a stack pointer or a program counter. The detail of these various circuits are not shown.

The general working register in the register unit 9 is used to hold the data to be processed and to store the address information upon reference to a memory. The stack pointer is used to store the address to which a subroutine jump. The program counter is a register for storing the memory address in which an instruction to be subsequently read out is stored. The content of the program counter is increased one by one each time one instruction other than the jump instruction is executed.

An address decoder 18 generates a signal for controlling the circuits 15 to 17, which will be described hereinafter, when it receives the output of the general working register of the register unit 9. Due to the provision of the address decoder 18, the circuits 15 to 17 can be controlled even by a reduced number of general working registers.

An address buffer 10 generates an address signal which is to be fed to an external address bus line coupled to the ROM 19, the RAM 20 and a peripheral equipment controller 21.

The input/output port 11 is provided to act as a data buffer and conduct the give-and-take of the data between the external data bus DT and the internal

data bus BUS.

An input/output port 12 is provided to make possible the giving and receiving of the digital signal between an object to be process-controlled and the micro-processor 1. For this purpose, the input/output port 12 has its digital signald input/output terminals coupled to the external terminals P_4 to P_7 of the micro-processor 1. Between the input/output port 12 and the internal data bus BUS, there is connected a register 15 which is controlled by the address decoder 18. The giving and receiving of the signal between the input/output port and the internal data bus BUS is accordingly performed through the register 15.

A multiplexer 13 is provided to selectively feed a plurality of analog signals to an A/D converter 14.

The plurality of input terminals attached to the multiplexer 13 are connected in a common manner with the terminals P_4 and P_5, as shown. As a result, the terminals P_4 and P_5 constitute common terminals which can be used either as the analog signal input or as the digital signal input and output. The plurality of input terminals other than those attached to the multiplexer 13 are connected with input terminals P_1 to P_3 and are used exclusively for the analog signals.

Between the A/D converter 14 and the internal

data bus BUS, there is connected a register 16 which has its operation controlled by the address decoder 18.

Accordingly, the digital output signal generated by the A/D converter 14 is transmitted through the register 16 to the internal data bus BUS.

The A/D converter 14 is of sequential comparison type. The operational amplifier or comparator, which forms a part of the A/D converter of sequential comparison type and which is to be fed with the analog signal to be converted, has a high input impedance.

The multiplexer controller 17 generates a selective signal to be fed to the multiplexer 13. This controller 17 includes a control register (or a latch circuit), which is controlled by the address decoder 18 in order to thereby read in the signal of the internal data bus BUS, and a decoder which decodes the output of that control register in order to thereby form the above referred to selective signal.

When the common terminals P_4 and P_5 are used as the digital signal input terminal or the digital signal output terminal, either the selection of the terminals P_4 and P_5 by the multiplexer 13 or the feed of the undesirable data from the register 16 to the internal data bus BUS is substantially prohibited. On the contrary, when the common terminals P_4 and P_5 are to be used as the analog input terminal, the selection of the terminals P_4 and P_5 by the input/output

port 12 is substantially prohibited. At this time, that output circuit in the input/output port 12, which has its output terminals coupled to the terminals P_4 and P_5, respectively, is made to have a high output impedance. As a result, the level of the analog signal to be fed to the terminals P_4 and P_5 is prevented from being undesirably changed by the output circuit in the input/output port 12.

Referring now to Figure 2, the multiplexer controller 17 consists of a latch circuit 17a and a decoder 17b. The analog multiplexor 13 is constituted by transmission gate MISFETs Q_{16} to Q_{20} whose gate electrodes are controlled from the outputs of the decoder 17b. Transmission gate MISFETs Q_1 to Q_3 are connected between the latch circuit 17a and the internal data bus BUS. The latch circuit 17a is fed with a predetermined address. When an address signal assigning the latch circuit 17a is supplied from the register unit 9 shown in Figure 1, the signal for selecting the transmission gate MISFETs Q_1 to Q_3 is accordingly supplied from the address decoder 18. As a result, the suitably coded multiplexer control data are fed through the internal data bus BUS and the transmission gate MISFETs Q_1 to Q_3 to the latch circuit 17a. The decoder 17b decodes the control data, which are set in the latch circuit 17a, in order to generate the selective signal which is to be fed to the multiplexer 13. Thus, when the specific address given

to the multiplexer controller 17 is assigned and when the multiplexer control data are supplied to the internal data bus BUS, the operations of the multiplexer 13 are accordingly controlled. One of the analog signals to be supplied to the terminals P_1 to P_5 is fed through the multiplexer 13 to the A/D converter 14. Incidentally, the selecting operation of the multiplexer 13 is prohibited when the data, which are coded so as not be decoded by the decoder 17b, are set in the latch circuit 17a.

Transmission gate MISFETs Q_4 to Q_6 are connected between the output terminals of the register 16 to be fed with the A/D converted output and the individual bit lines B_1 to B_8 of the internal data bus BUS. When predetermined address data indicative of the register 16 are supplied from the register unit 9 shown in Figure 2, a signal at a high level is accordingly fed out of the address decoder 18 to a control line CL_2. As a result, the MISFETs Q_4 to Q_6 are rendered conducting so that the A/D converted output held in the register 16 is supplied to the internal data bus BUS.

The input/output port 12 for the digital signal is formed by input and output buffer amplifiers 12a and 12b which are coupled to the terminals P_4 to P_n, respectively. The output buffer amplifier 12b has a gate terminal coupled to a line GL

so that its operation is controlled by the gate signal. The output of that output buffer amplifier 12b is made, if the gate signal is at a high level, to take a high or low level corresponding to its input signal. Moreover, the output of the output buffer amplifier 12b is held in a floating or high output impedance state, if the gate signal is at a low level, irrespective of its input signal.

The register 15 is constituted by a plurality of latch circuits of which three are gathered into one group. of these latch circuits 15a to 15c belonging the one group: the latch circuit 15a has its input terminal I coupled to the output terminal of the input buffer amplifier 12a; the latch circuit 15b has its output terminal Q coupled to the input terminal of the output buffer amplifier 12b; and the latch circuit 15c has its output terminal Q coupled to the gate input of the output buffer amplifier 12b. The output terminal Q of the latch circuit 15a, the input terminal I of the latch circuit 15b and the input terminal I of the latch circuit 15c are connected through transmission gate MISFETs Q_7 to Q_9 to the bit line B_1 of the internal data bus BUS. Likewise, the remaining latch circuits of the register 15 are connected through transmission gate MISFETs Q_{10} to Q_{15} with the respective bit lines B_2 to B_8 of the internal data bus BUS. The transmission gate MISFETs Q_7 to Q_{15} are respectively fed with predetermined addresses and

rendered conducting and inconducting by the control of the output of the address decoder 18.

In accordance with the construction shown, the analog input converted into a digital value and the digital input are fed to the common internal data bus BUS. The receptions of those two inputs are conducted by making different the address assigning timings of the registers 16 and 15.

Whic of the following terminals is used: the analog signal input terminal, the digital signal input terminal and the digital signal output terminal; as the common terminals P_4 and P_5, is determined by the program which has been written in advance in the ROM 19 shown in figure 1.

For example, in the case where the terminals P_4 and P_5 are used as the digital signal input or output terminal, they are not selected by the multiplexer 13. For this purpose, the program is so constructed that the data for selecting those terminals are not set in the controller 17. At the same time, the program processes the digital signal which contains the address assigning instructions of the latch circuits 15a and 15b in the register 15 as correspond to the terminals P_4 and P_5. The interchange of the input and output of the digital signals corresponding to the terminals P_4 and P_5, i.e. the direction of the signal at the input/output port 12 is designated by setting and resetting the latch circuit 15c of the register 15. More specifically, in the case where

the output of the latch circuit 15c is set at "0", as has been described previously, the output impedance of the output buffer amplifier 12b is made high. At this time, the digital input signal is processed. On the contrary, in the case where the latch circuit 15c is set at "1", the output buffer amplifier 12b is operated so that the digital output signal is generated at the terminal P_4. In the case where the common terminals P_4 and P_5 are to be used as the analog input terminal, the code data for selecting those terminals is set in the multiplexer controller 17 by the execution of a predetermined program instruction. At this time, the output of the latch circuit 15c for setting the directivity is so held at "0" that the analog input signal can be fed to the terminals P_4 and P_5, whereby the output buffer amplifier 12b of the input/output port 12 is made to have a high output impedance. In this case, the addresses of the latch circuits 15a, 15b and 15c of the register 15, which correspond to the terminals P_4 and P_5, are not assigned.

The giving and receiving of the digital signal to and from the uncommon terminal for the digital signal of the terminals P_4 to P_7 is conducted by selecting the address of the register 15 at such a timing as is made different from the address assigned timing of the register 16.

In a practical example, the integrated circuit 1 of Figure 1 is used to control an internal combustion engine.

For this purpose, a thermistor DET_1 for detecting the temperature of engine cooling water is connected between the terminal P_1 and earth. A load register R_1 is connected between that thermistor DET_1 and a power source terminal V_B. This power source terminal V_B is fed with the output voltage of a constant voltage circuit 40 which in turn is fed with the output voltage of a battery B through an ignition switch S_o. The output voltage of the constant voltage circuit 40 is fed to the micro-processor 1 and to a variety of such circuits as will be described hereinafter. By using a thermistor having a negative temperature coefficient as the thermistor DET_1, the voltage to be applied to the terminal P_1 is lowered with a rise in the temperature of the cooling water.

Likewise, there are connected with the terminal P_2 a thermistor DET_2 for detecting the temperature of the intake air of the engine and a load resistor R_2 of the thermistor DET_2.

To the terminal P_3, there is connected an intake flow meter DET_3. This intake flow meter DET_3 includes a resistor member and a slide contact which has its position changed relative to that resistor member in accordance with the flow rate of the

intake air. As a result, the intake flow meter thus constructed generates a voltage at such a level which is proportional to the intake flow rate.

To the terminal P_4, there is connected an engine tachometer DET_4. This tachometer feeds the terminal P_4 with an analog voltage which is proportional to the engine R.P.M.

A starter switch SW is connected to the terminal P_5.

To the terminal P_6, there is connected an engine crank angle sensor DET_5. This sensor DET_5 generates a pulse signal when the engine crank angle takes a predetermined value, e.g. 0 degrees.

The terminal P_7 is used as an output terminal for giving a warning of excessive engine termperature. A lamp PL is energized through a buffer circuit 30 which receives the outpput of the terminal P_7 and is lit when the engine temperature reaches an excessive value.

The peripheral equipment controller 21 is fed with the control signals from the grouped external terminals CONT, the address signal from an external address bus AD and the data from the data bus DT. That peripheral equipment controller 21 is provided with a plurality of output lines l_1 to l_4 and includes memory circuits (although not shown), which are selected by the address signals of the address

bus AD, respectively, and which have their states determined by the data signal of the data bus DT.

The signal on the output line l_1 of the peripheral equipment circuit 21 is fed through an output buffer circuit 22 to an ignition coil 26 whereas the signal on the output line l_2 is fed through an output buffer circuit 23 to a solenoid 27 for adjusting the opening of the throttle valve of the intake manifold of the engine. On the other hand, the signal on the output line l_3 is fed through an output buffer circuit 24 to an electromagnetic type fuel pump 28, whereas the signal on the line l_4 is fed to a relay 29 for driving the sel-motor of the engine.

The read only memory (ROM) 19 for engine control stores the interpolation data, which are determined by the characteristics of the engine to be controlled, as well as the program.

When the ignition switch S_0 is turned on, the power source voltage is supplied from the battery B to the constant voltage circuit 40, from which the power source voltage V_B is supplied to the various above described circuits. Accordingly, the micro-processor 1 is brought into its operative state.

The analog data such as those temperatures of the engine cooling water or the intake air, which are obtained from the thermistor DET_1 or DET_2, are converted into digital data in a time-dividing manner

by the action of the analog-to-digital converter 14. The respective digital data thus converted are written in the RAM 20 through the data bus.

The fuel pump 28 is brought into its operative state by the output which is fed out of the peripheral equipment controller 21 through the line l_3.

When the starter switch SW is turned on, the relay 29 is energized so that the sel-motor (although not shown) starts its operation.

In order to reduce the capacity of the ROM 19, its data concerning the ignition timing, for example, are made to correspond only to a predetermined engine R.P.M. sampled.

Therefore, the ignition timing data for the tachometer DET_4 and for an arbitrary R.P.M. are deduced by the calculations, in which the interpolation data at a sampled R.P.M. in the vicinity of the artibrary engine R.P.M. in the ROM 19 are corrected by the artibrary R.P.M.

The actual ignition timing is deduced by the calculations from both the reference time of ignition, which is based upon the output from the crank angle sensor DET_5, and the ignition timing data which are deduced by the above referred to calculations. In accordance with that actual ignition timing, the ignition coil 26 is energized.

By means of the engine R.P.M. data and the engine cooling water temperature data, and the

interpolation data of the ROM 19, the pulse control signal for controlling the throttle valve is generated after the appropriate calculations have been performed. By means of this pulse controlling signal, the duty ratio of the pulse current supplied to the solenoid 27 coupled through the peripheral equipment controller 21 is changed. The solenoid 27 has its mean current varied in accordance with the duty ratio of the pulse current. As a result, the opening of the throttle valve is controlled in accordance with the duty ratio.

In a system which is intended to make the analog input terminal and the digital input/output terminals common, such as the semiconductor integrated circuit device constituting the micro-processor described above, if the analog signal line and the digital signal line prepared by the multi-layer wiring technique intersect or overlap, the above referred to undesirable capacitance is established between the analog signal line and the digital signal line. Accordingly, a malfunction takes place in the analog signal processing operation, as has been described above. More specifically, if the state of the starter switch SW is changed while the A/D converter 14 is converting the analog voltage according to the engine R.P.M. which is fed out of the tachometer DET_4, into the digital signal, the level of the digital singal at the terminal P_5 is changed

in accordance with the change in the state of the starter switch SW. The change in the digital signal level at both the terminal P_5 and the line coupled to the terminal P_5 is transmitted through the capacitance to the analog signal line which is coupled to the A/D converter 14. As a result, the A/D converter 14 converts the analog signal, which set at an undesirably high or low level relative to the analog voltage at a proper level, into the digital signal. In other words, a malfunction takes place in the analog signal processing operation in the A/D converter 14.

Incidentally, the level of the digital signal is changed within a relatively short period of time from 5 volts to 0 volts or vice versa, for example. in other words, the level is a substantial change in a relatively short period of time. As a result, the change in the level is transmitted to the input of the A/D converter 14 through the capacitance.

In Figure 3, there is shown the top plan pattern of a portion of the semiconductor integrated circuit device which enables a reduction in the crosstalk of the digital signal fed to the analog signal to be achieved. In Figures 4 and 5, there are shown the sections of the semiconductor substrate, which correspond to the section lines A-A' and B-B' of Figure 3. The portion of the semiconductor integrated circuit shown in Figures 3 to 5, relates to the

multiplexer 13. Incidentally, in order to allow the layout pattern of the circuit to be easily understood, the portions in which the circuit blocks 12, 14 and 17 shown in Figures 1 and 2 are indicated by blocks 12, 14 and 17 in Figure 3.

The semiconductor integrated circuit device shown is manufactured by the known local oxidation technique and self-alignment technique. A semiconductor substrate 100, which is made of p-type single crystalline silicon and which has its main surface arranged in parallel with the crystalline surface (100), is formed on its surface with a field oxide film 101 which is prepared by the local oxidation technique to have a relatively large thickness, e.g., about 1.2μm. That portion of the surface of the semiconductor substrate 100, which is to be formed into active regions, i.e. the portion which is not covered with the field oxide film 101 is formed with an n^+-type poly-crystalline silicon layer 103a having a thickness of about 0.35μm through a gate oxide film 102 having a small thickness, e.g. about 500 Å. The n^+-type poly-crystalline silicon layer 103a constitutes the gate electrodes of the MISFETs. The field oxide film 101 is formed on its surface with an n^+-type poly-crystalline silicon layer 103b which is formed with that n^+-type poly-crystalline silicon layer 103a. Therefore, the poly-crystalline silicon layer 103b

constitutes the first wiring layer.

The semiconductor substrate 100 is formed on its surface with n^+-type semiconductor regions 104a, 104b and 104c which have a depth of about 1μm by using the field oxide film 101 and the poly-crystalline silicon layer 103a as an impurity doping mask. Those n^+-type semiconductor regions are used as the source and drain regions and the semiconductor wiring regions of the MISFETs. The field oxide film 101 and the poly-crystalline silicon layers are formed thereon with an interlayer insulating film 105 which is made of phospho silicate glass to have a thickness of about 0.6μm. The interlayer insulating film 105 is formed thereon with semiconductor layers 106a, 106b and 106c which are made of evaporated aluminium to have a thickness of about 1μm. These evaporated aluminium layers are held in ohmic contact with the n^+-type semiconductor regions 104a, 104b and 104c at the contact portions formed in the interlayer insulating film 105. The evaporated aluminium layers constitute the second wiring layer.

The analog signal line and the digital signal line are respectively formed in the areas which are divided along the array of the bonding electrodes P_1 to P_6 connected with the external terminals. Incidentally, in Figure 3, the pattern of the aluminium layer constituting the bonding electrodes and the second wiring layer is indicated by solid

lines, and the pattern of the conductive poly-crystalline silicon layers constituting both the gate electrodes of the MISFETs Q_{16} to Q_{20} acting as the multiplexer and the first wiring layer is indicated by double-dotted lines. On the other hand, the pattern of the diffusion layers acting as the source and drain regions of the MISFETs is indicated by broken lines. In the surface of the semiconductor substrate, the portions, which extend between the paired semiconductor regions such as the semiconductor regions 104a and 104b, are used as the channel regions of the MISFETs. In Figure 3, rectangular patterns indicated as symbols X indicate the constact portions. In these contact portions, the semiconductor regions and the second aluminium layers are connected, as has been described previously.

The respective bonding electrodes P_1 to P_6 are arranged on the peripheral portions of the semiconductor chip 1, and an analog signal line L_A made of an aluminium wiring layer is formed in the area between the array of the electrodes P_1 to P_6 and the edge SL of the semiconductor chip 1. That analog signal line L_A is coupled to the input terminal of the A/D converter 14. Moreover, the analog signal line L_A is connected with the semiconductor regions 104b to 104f of the MISFETs Q_{16} to Q_{20} acting as the multiplexer.

For the array of the bonding electrodes P_1 to P_6, on the other hand, the inner area IL of the semiconductor chip 1 is formed with the digital signal lines L_D, e.g. L_{D1} to L_{D3}, which are formed by the aluminium layers, and the digital control lines CL_{61} to CL_{65} which are formed by the conductive poly-crystalline silicon layers. Of those, the digital signal lines L_{D1} to L_{D3}, which are formed by the aluminium layers, connect the diffusion regions of the MISFETs Q_{16} to Q_{20} acting as the multiplexer and the input/output port 12. Incidentally, the bonding electrode P_5 and the digital signal line L_{D2}, may be formed of the continuous aluminium layer likewise the bonding electrode P_6 and the signal line L_{D1} coupled to the electrode P_6.

The digital control lines CL_1 to CL_5, which are made of the conductive poly-crystalline silicon layers integrated with the gate electrodes of the MISFETs Q_{16} to Q_{20}, are connected with the output terminals of the control register 17.

Incidentally, the semiconductor substrate 100 is sealed by such a well-known resin-molding technique as will be described in the following. Specifically, first of all, a lead frame is prepared. The semiconductor substrate 100 is adhered to the tab portion of the lead frame. The bonding electrodes on the semiconductor substrate 100 and the lead portions

of the lead frame are connected by the well-known nail head bonding technique which uses a connector wire in the form of a thin gold wire having a diameter of about 40μm. Next, the semiconductor substrate 100 is moulded from resin. The semiconductor integrated circuit device is completed by removing the unnecessary portion or portions of the lead frame.

In the embodiment thus far described, the analog signal lines and the digital signal lines can be formed on the semiconductor chip 1 without any intersection so that the above mentioned malfunction in the analog signal processing operation can be obviated. A relatively high parasitic capacitance is established between the control line 103b, which is formed by the conductive polycrystalline silicon layer, and the digital signal line L_{D3}, which is formed by the aluminium layer, as shown in Figures 3 and 5, because the two lines intersect through the relatively thin interlayer insulating film 105. However, that parasitic capacitance can be substantially neglected, as will be evident from the following.

Specifically, the transmission gates MISFETs Q_{16} to Q_{20} constituting the multiplexer 13 have relatively high "ON" resistances. The MISFETs Q_{16} to Q_{20} are brought into their "OFF" states after the analog signal has been sampled. As a result, the analog signal line L_A has a relatively high

impedance. If the analog signal line L_A and one of digital signal lines or digital control lines intersect, a relatively high parasitic capacitance is established at that intersection so that relatively high potential fluctuations or noises are imparted to the analog signal line L_A.

On the contrary, the potential fluctuations or noises to be fed from the digital control line 103b to the signal line L_{D3} and the bonding pad P_4, as shown in Figures 3 to 5, are reduced to a sufficiently low level by the relatively low output impedance of the circuit such as the analog sensor which is coupled to the bonding pad P_4. As a result, the parasitic capacitance to be established between the lines 103b and L_{D3} can be substantially obviated.

Moreover, if the analog signal line L_A is so arranged as is shown in Figure 3, the not-shown connector lines, which are connected with the bonding electrodes P_4 and P_5, and the analog signal line L_A are made to three-dimensionally intersect. The connector lines can be made to have a relatively large diameter, e.g. about 40μm, as has been described hereinbefore. In this case, however, the distances between the connector lines, which are connected with the electrodes P_4 and P_5 by the nail head bonding technique, and the analog signal line L_A can be made to have such a sufficiently high value according to

the curvatures of the connector lines as is higher than 0.1 mm. As a result, the stray capacitance to be established between the connector lines and the analog signal line L_A can be made to have a sufficiently low value.

In the case where the analog input terminal and the digital input/output terminal are made common, as has been shown in Figures 1 and 2, the number of the terminals to be attached to the micro-processor 1 can be reduced. Moreover, the use of one kind of the micro-processor 1 makes it possible to conduct a variety of process controls, in which the number of the analog signal inputs and the number of the digital signal inputs and outputs are different. As a result, the wide usability of the various process controls such as the controls of the automotive engine by the micro-processor can be improved. Moreover, the system change such as the conversion of the digital input to the analog input for ensuring the high quality of the process control, i.e. the highly dense control can be performed merely by changing a portion of the program to be written in the ROM 19.

In modified forms, the analog signal lines, the digital singal lines and the digital control lines may make use of a semiconductor diffusion layer in addition to the aluminium layer and the conductive

poly-crystalline silicon layer thus far described, and their combinations can be modified in various ways.

Moreover, the analog signal lines and digital signal lines need not be connected with the bonding electrodes, but the present invention can be widely applied to the semiconductor integrated circuit which is equipped with both the analog signal lines connected with the analog signal processing circuit having the high input impedance and the digital signal lines.

Furthermore, the analog signal lines and digital signal lines may be connected either independently of one another, or partially or wholly commonly with the bonding electrodes. In this modification, for the simplification or high density of the wiring layout, it is desired that the analog and digital signal lines be respectively formed in the areas which are divided along the array of the bonding electrodes. Furthermore, the bonding electrodes need not be arranged in the periphery of the semiconductor chip but may be formed in the middle portion of the semiconductor chip in accordance with the increase in the size of the semiconductor chip.



CLAIMS.

1. A semiconductor integrated circuit device including:

(a) an analog signal transmission link formed on a semiconductor substrate in a first prescribed geometrical pattern;

(b) a first prescribed, analog signal-handling, electronic circuit formed on said substrate and coupled to said analog signal transmission link so that analog signals may be exchanged between said first prescribed circuit and said analog signal transmission link;

(c) a digital signal transmission link comprised of a plurality of digital signal conveying paths and formed on said substrate in a second prescribed geometrical pattern separated from said first prescribed geometrical pattern so as not to overlap said first pattern;

(d) a second prescribed, digital signal-handling, electronic circuit formed on said substrate and coupled to said digital signal transmission link so that digital signals may be exchanged between said second prescribed circuit and said digital signal transmission link;

(e) a plurality of bonding pad electrodes arranged on said substrate at positions adjacent to and separating respective ones of said digital signal conveying paths from said analog signal transmission link;

(f) first means for coupling respective ones of said digital signal conveying paths to said plurality of bonding pad electrodes; and

(g) second means for selectively coupling selected ones of said bonding pad electrodes to said analog signal transmission link.

2. A semiconductor integrated circuit device according to claim 1, wherein said plurality of bonding pad electrodes are arranged adjacent a peripheral portion of said substrate, and wherein said analog transmission link is arranged along said peripheral portion of said substrate and said bonding pad electrodes.

3. A semiconductor integrated circuit device according to claim 1, wherein said second means includes a plurality of selectively controlled field effect transistors located between respective ones of said bonding pad electrodes and said analog signal transmission link.

4. A semiconductor integrated circuit device according to claim 3, wherein said second means includes a multiplexer having control signal paths coupled to respective gate electrodes of said first effect transistors.

5. A semiconductor integrated circuit device according to claim 4, wherein said device is formed as part of a microprocessor for controlling an internal combustion engine.

6. A semiconductor integrated circuit device according to claim 1, wherein said first prescribed

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electronic circuit comprises an analog-to-digital converter.

7. A semiconductor integrated circuit device according to claim 6, wherein said second prescribed electronic circuit comprises a digital signal input circuit.

8. A semiconductor integrated circuit device according to claim 6, wherein said second prescribed electronic circuit comprises a digital signal input/output circuit.

9. A semiconductor integrated circuit device according to cliam 8, further including a control circuit for controlling the coupling of analog signals over said analog signal transmission link to said analog-to-digital converter, and the coupling of digital signals between said digital signal transmission link and said digital signal input/output circuit.

10. A semiconductor integrated circuit device according to claim 9, wherein said digital signal input/output circuit includes an input signal circuit portion and an output signal circuit portion, and further including means for causing said output signal circuit portion to have a large output impedance when said bonding pad electrode receives a signal from an external source to be coupled to either one of said signal transmission links.

11. A semiconductor integrated circuit device constructed and arranged to operate substantially as described with reference to and as illustrated in the accompanying drawings.