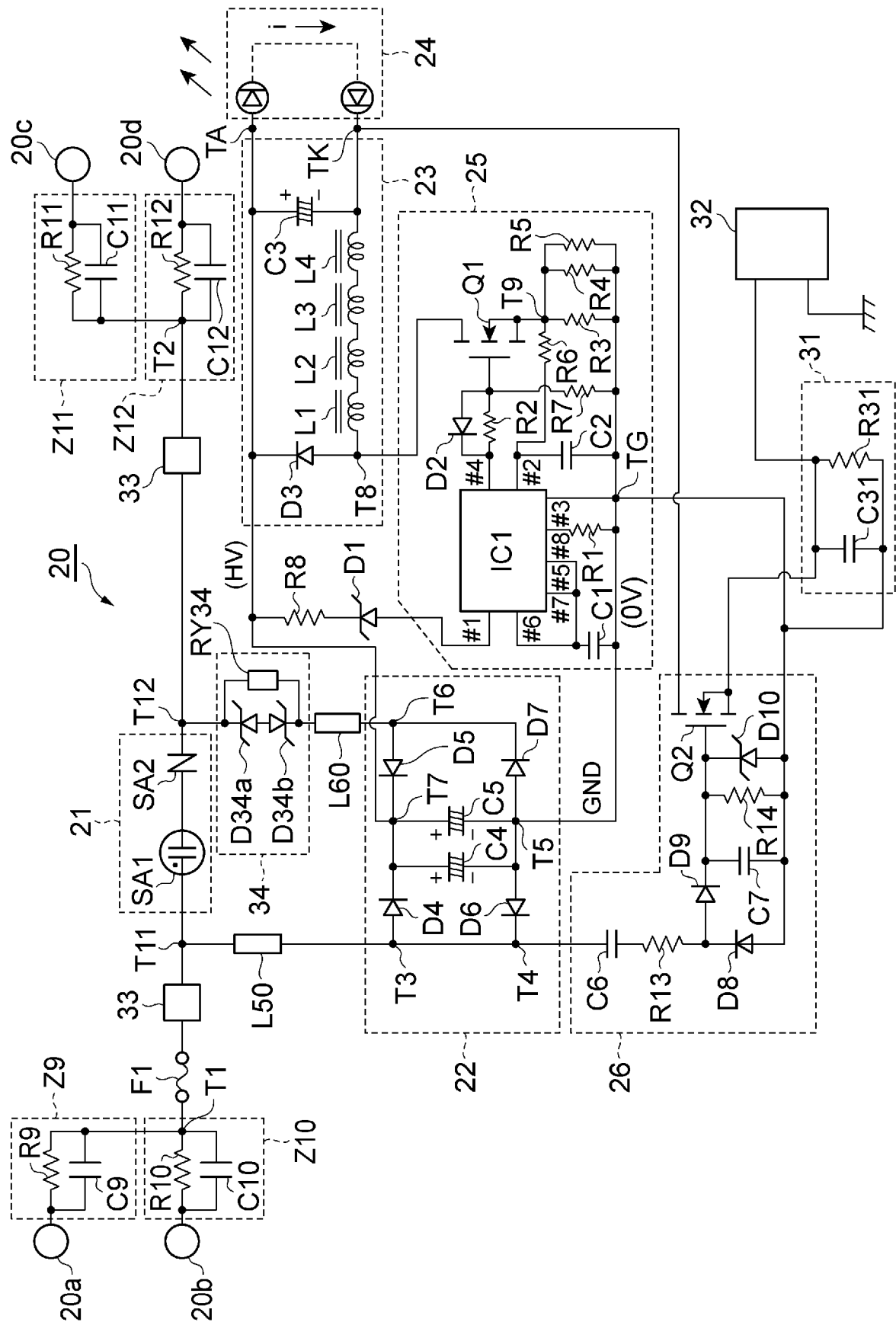
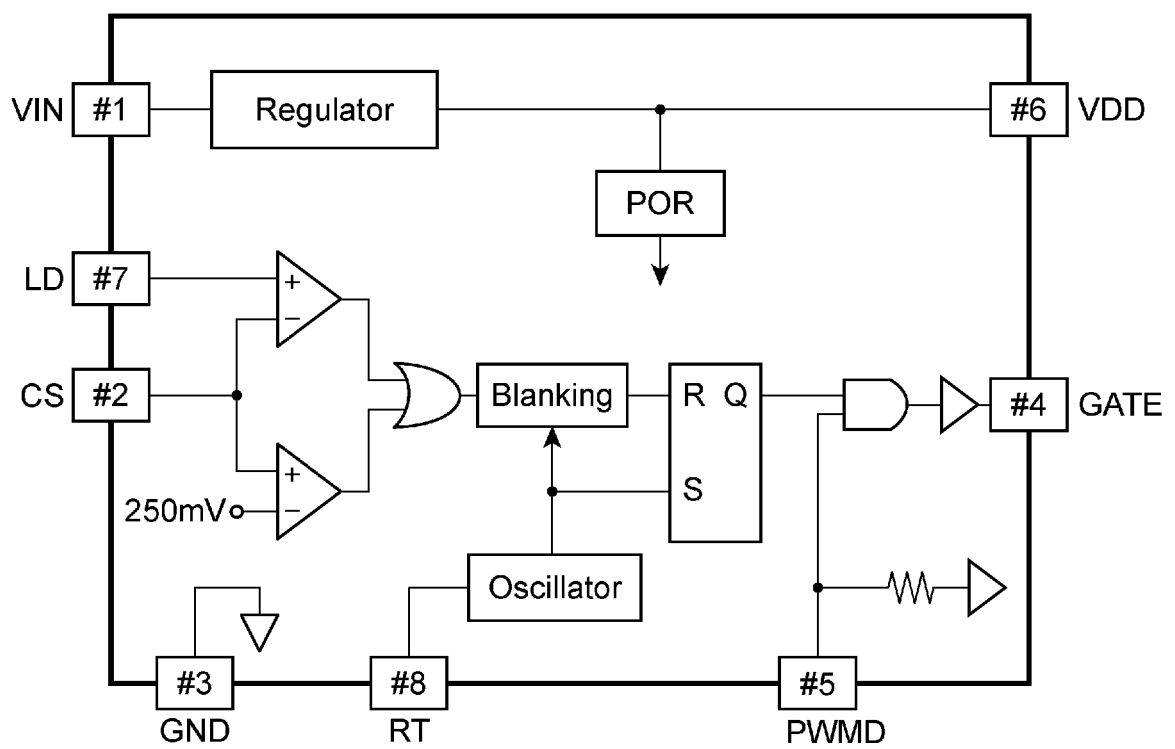


[illegible]

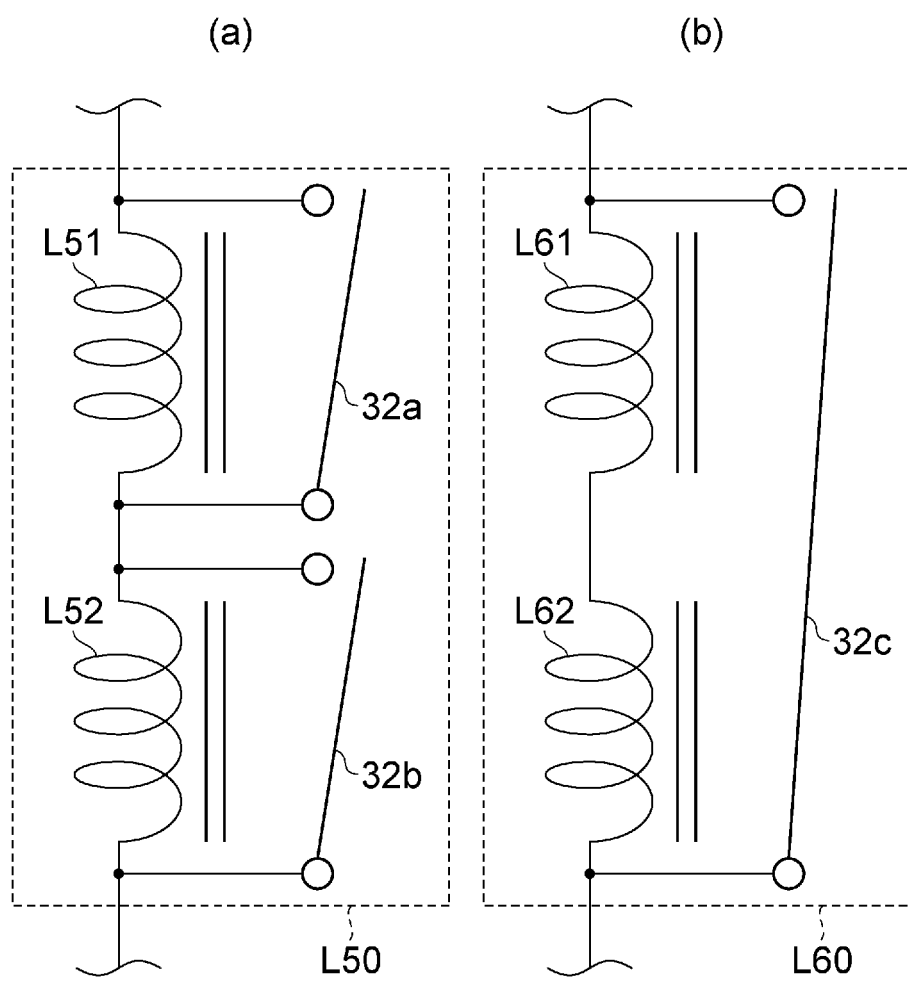
[図2]



[図3]



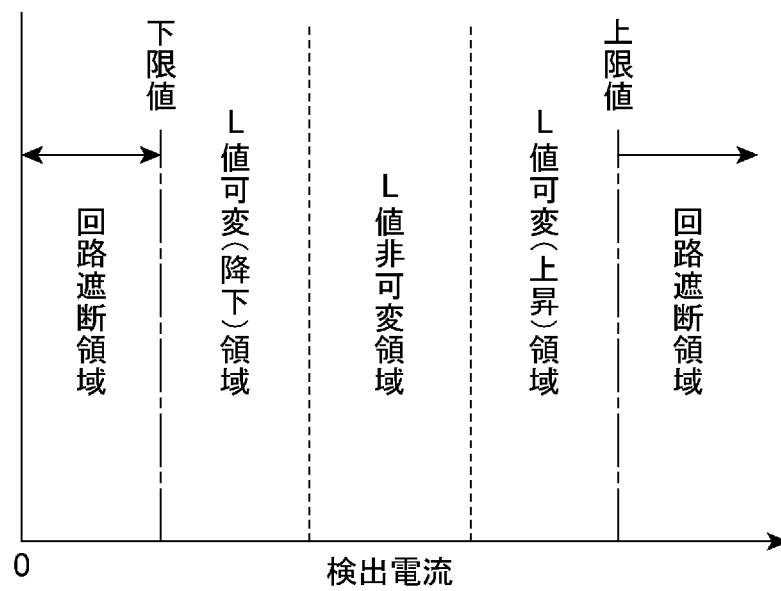
[図4]



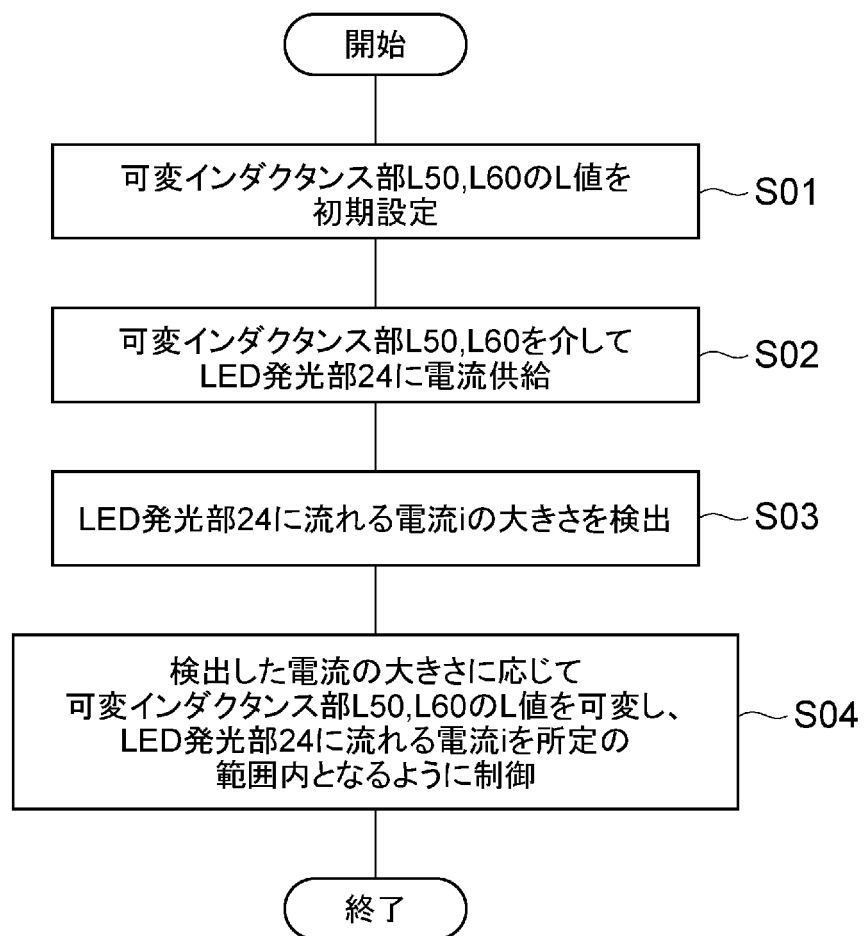
[図5]

スイッチ 素子	パターン1	パターン2	パターン3
32a	OFF	ON	ON
32b	OFF	OFF	ON
32c	OFF	OFF	ON
L値	L51,L52, L61,L62 の総和	L52,L61, L62 の総和	$0\mu\text{H}$

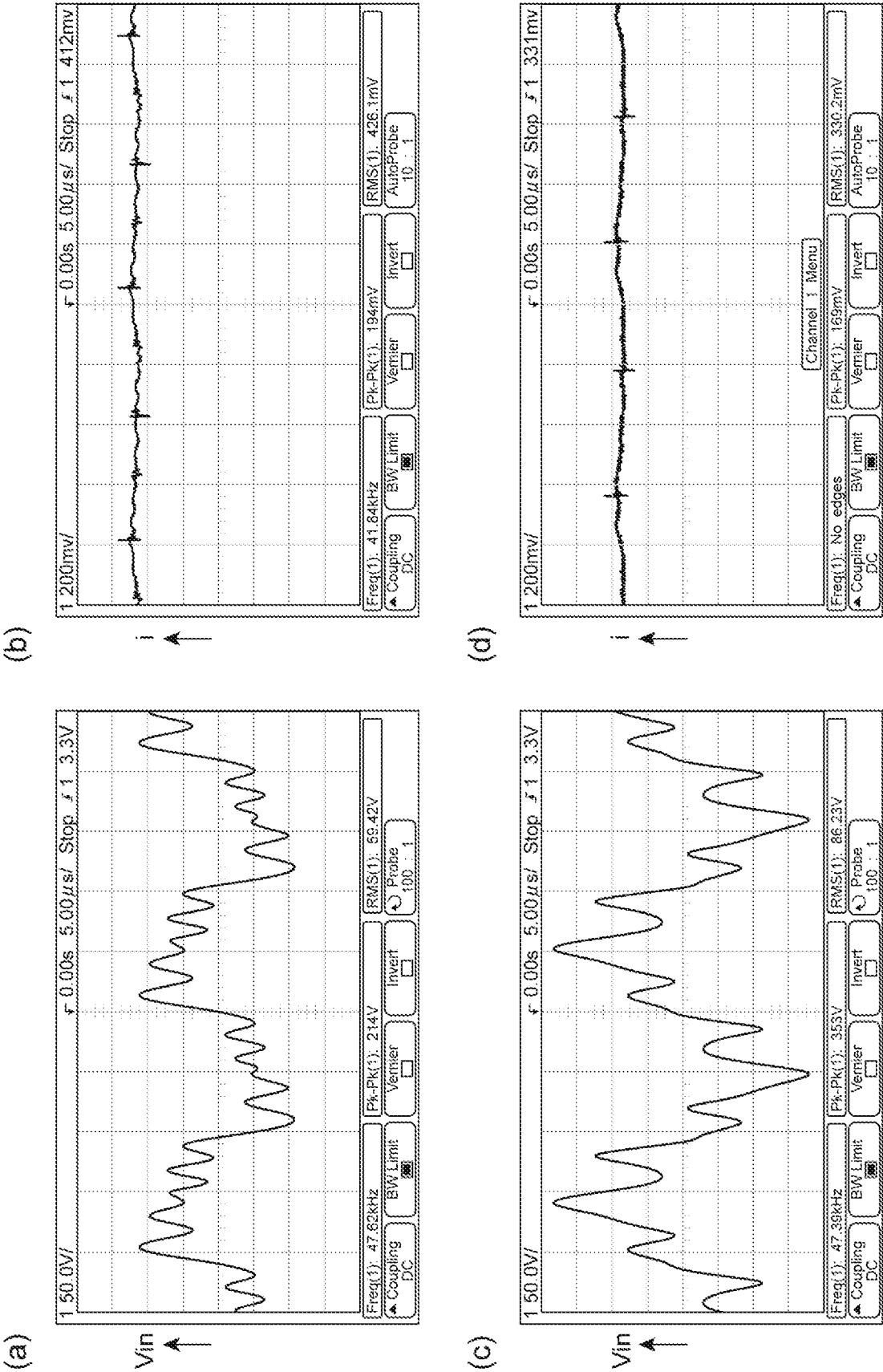
[図6]



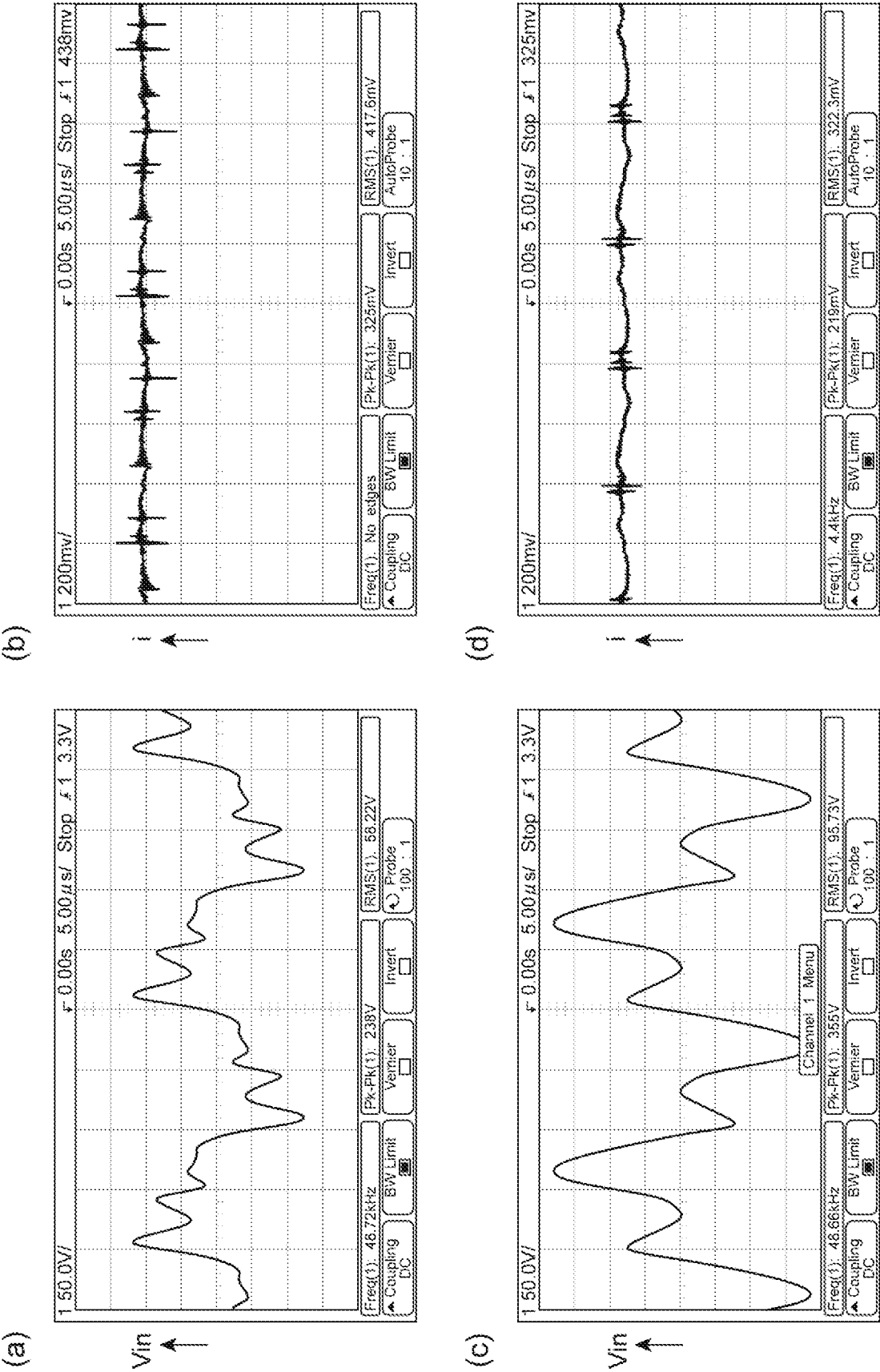
[図7]



[図8]

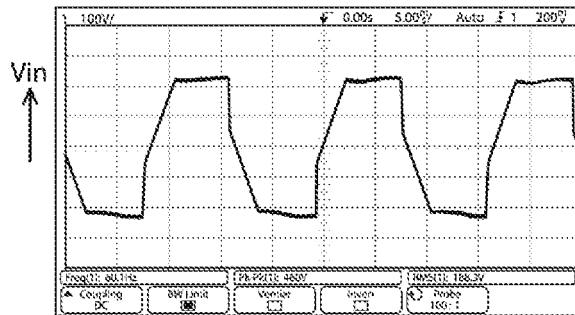


[図9]

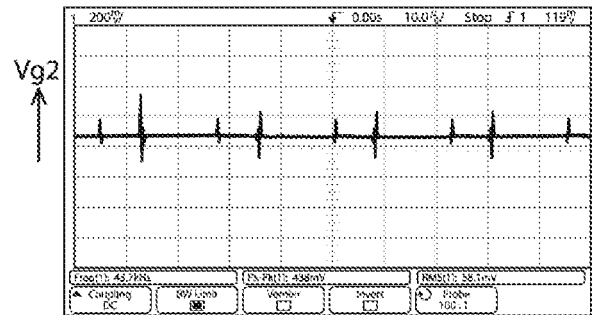


[図10]

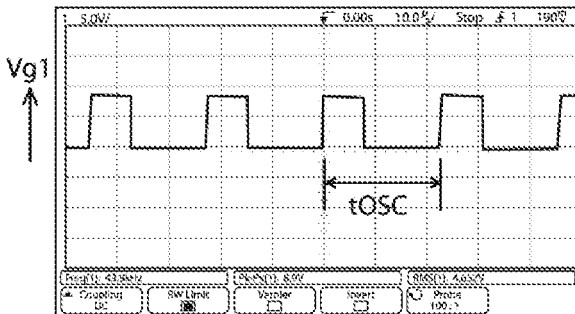
(a)



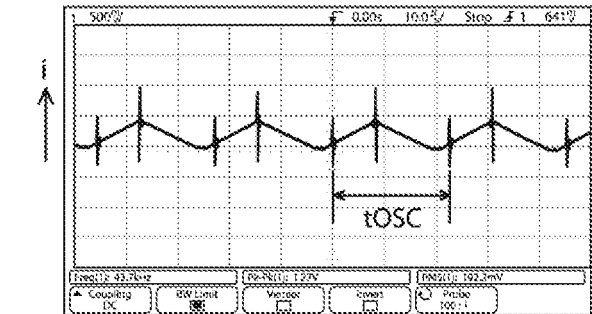
(d)



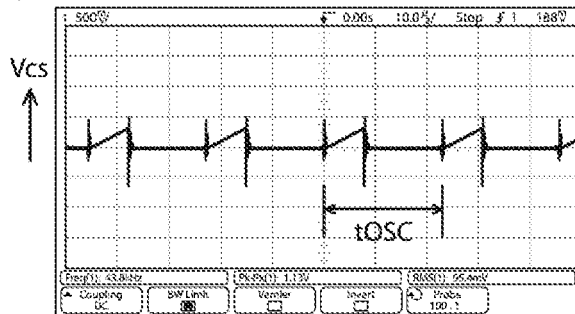
(b)



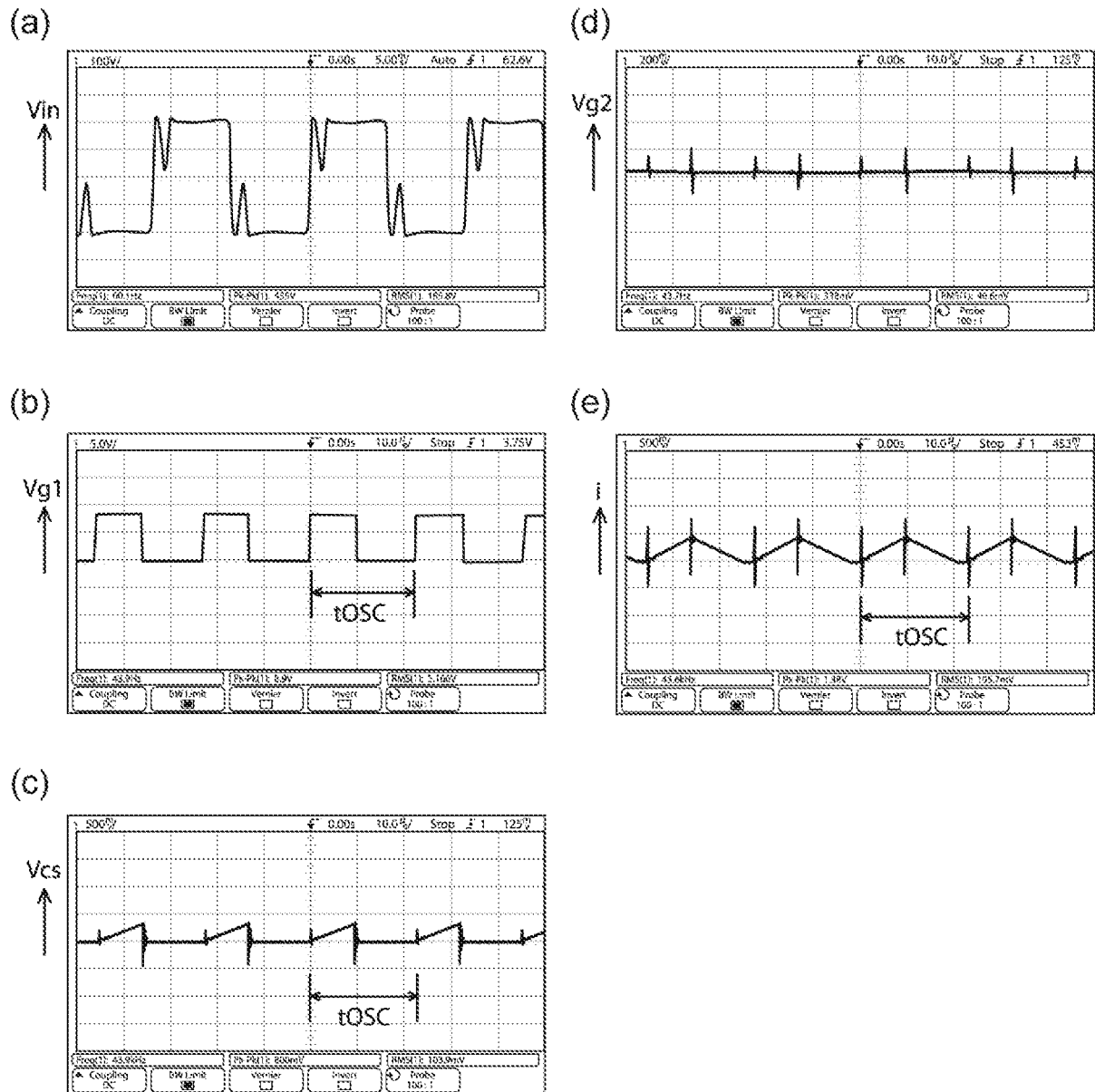
(e)



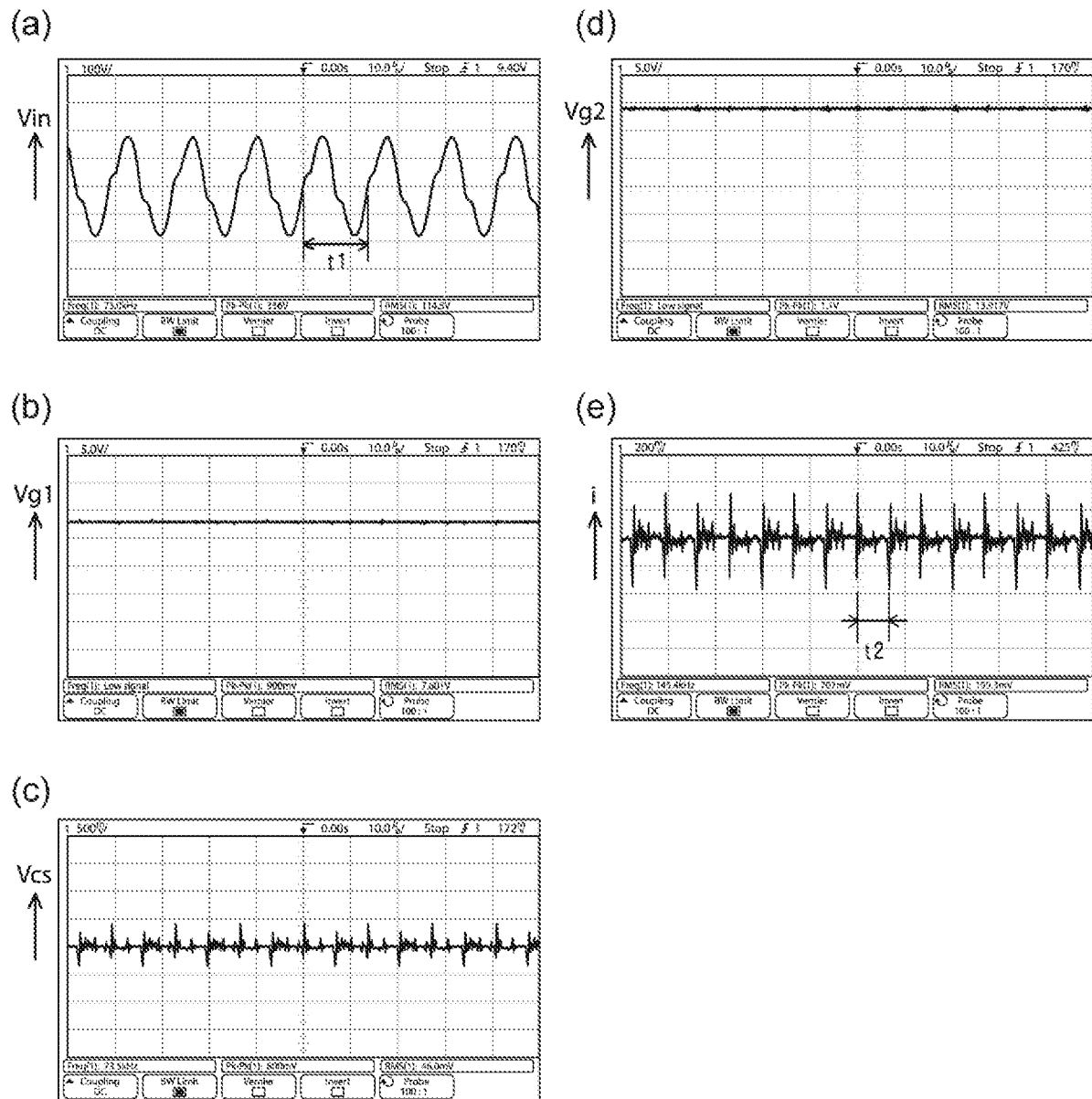
(c)



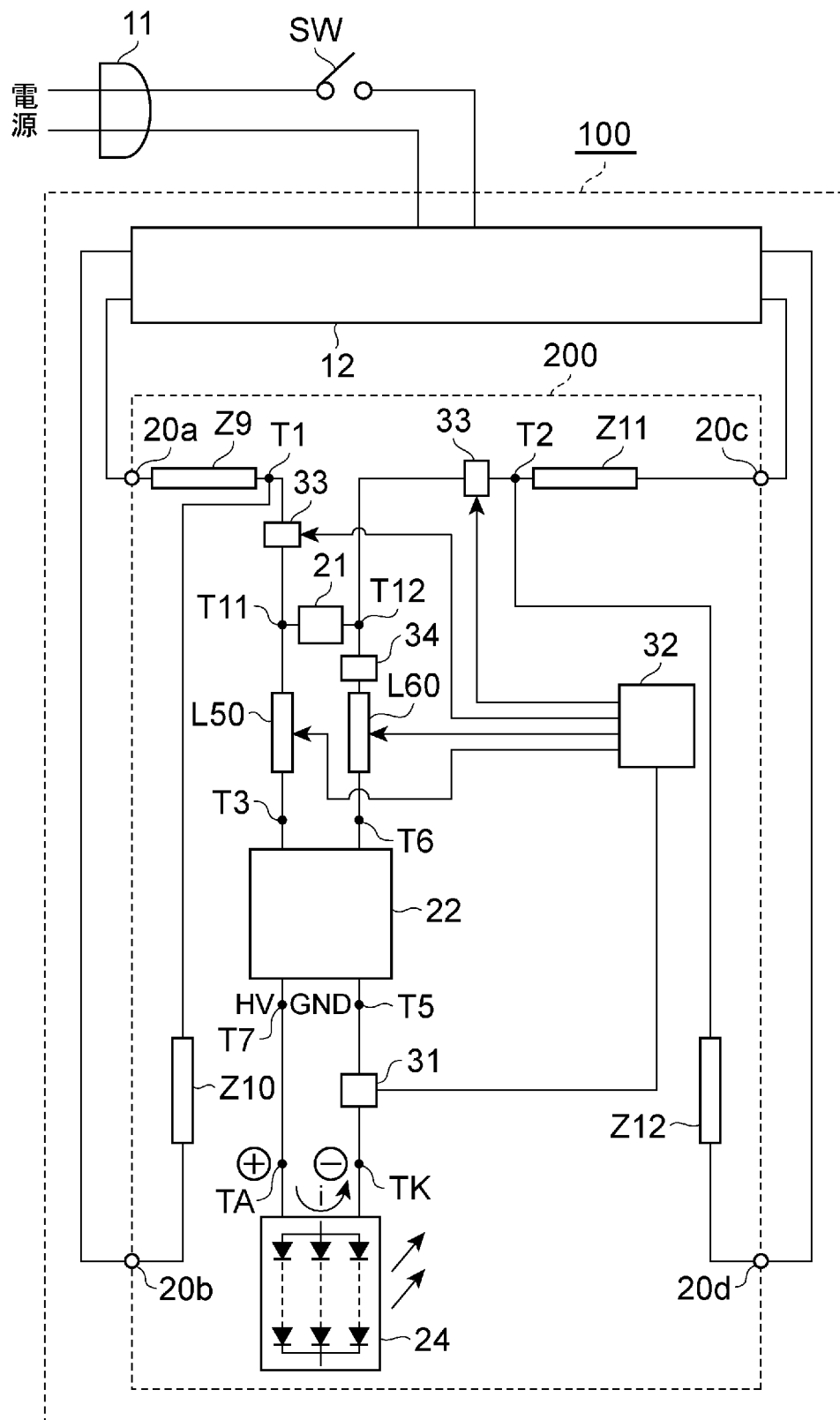
[図11]



[図12]

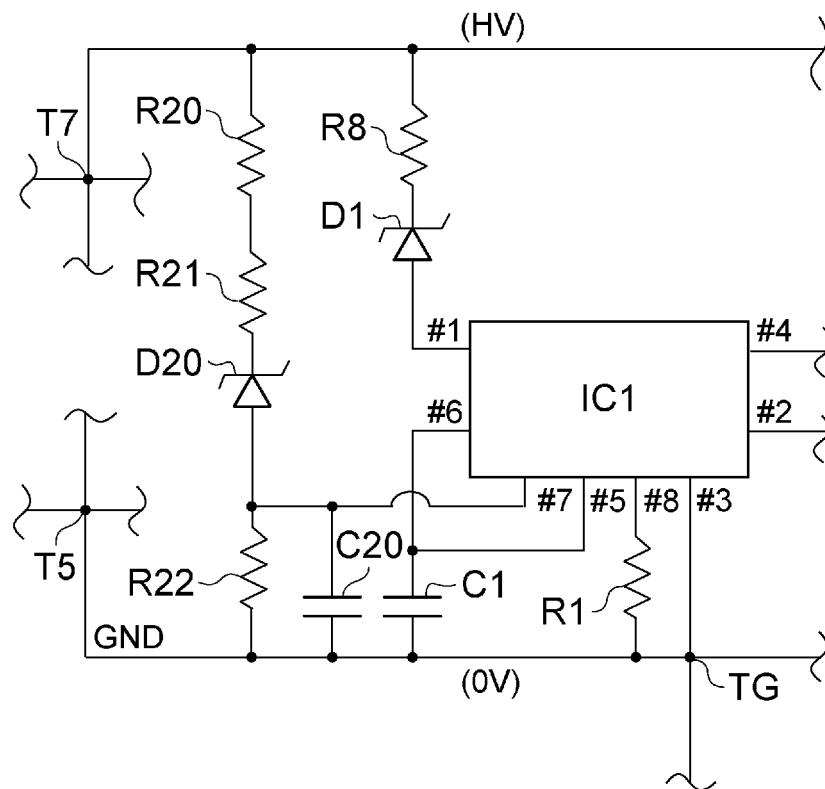


[図13]

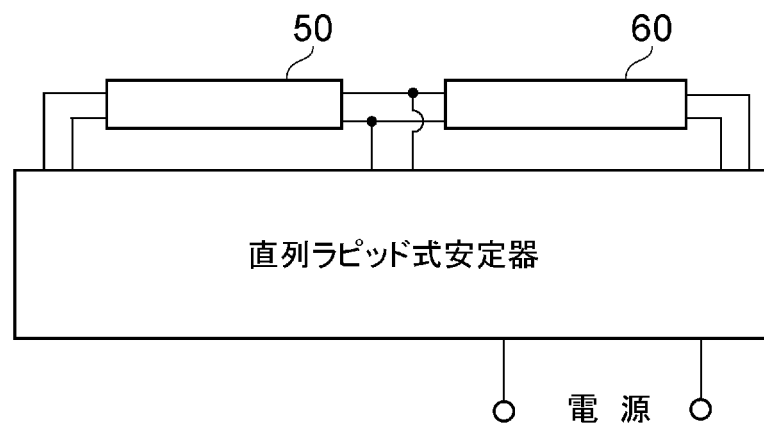


[図14]

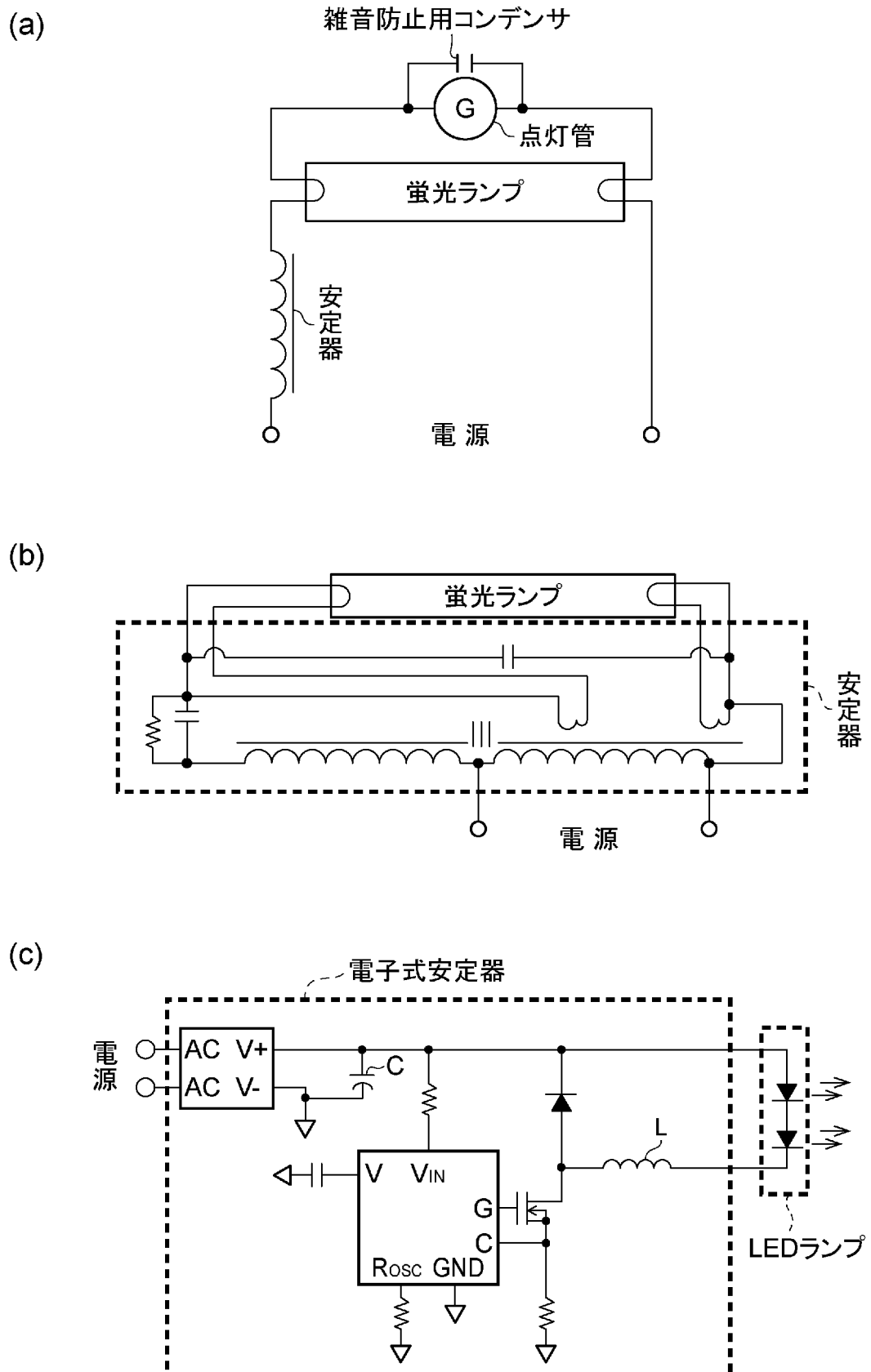
(a)



(b)



[図15]



[図16]

