CLAIMS

1. A liquid crystal display device comprising:

a substrate that constitutes a display panel;

a plurality of video signal lines which transmit video signals;

a plurality of scanning signal lines which intersect the plurality of video signal lines;

a plurality of pixel formation portions arranged in a matrix so as to correspond to the plurality of video signal lines and the plurality of scanning signal lines;

a scanning signal line drive circuit that includes a shift register made of a plurality of bistable circuits which are provided so as to correspond to the plurality of scanning signal lines and sequentially output pulses based on a clock signal, and that selectively drives the plurality of scanning signal lines based on the pulses outputted from the shift register;

a power supply circuit that generates, based on a power supply given from an outside, a scanning signal line selection potential as a potential for turning the scanning signal lines to a selected state, and a scanning signal line non-selection potential as a potential for turning the scanning signal lines to a non-selected state;

a drive control unit that generates the clock signal, a clear signal for initializing states of the plurality of bistable circuits, and a reference potential as a potential serving as a reference of operations of the plurality of bistable circuits, and controls an operation of the scanning signal line drive circuit; and

a power supply state detection unit that gives a

predetermined power supply OFF signal to the drive control unit upon detecting an OFF state of the power supply,

wherein the plurality of video signal lines, the plurality of scanning signal lines, the plurality of pixel formation portions, and the scanning signal line drive circuit are formed on the substrate,

each of the bistable circuits includes:

an output node connected to the scanning signal line;

an output control switching element in which a second electrode is given the clock signal, and a third electrode is connected to the output node;

a first node connected to a first electrode of the output control switching element; and

a first first-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the first node, and a third electrode is given the reference potential,

the power supply circuit generates, as the scanning signal line selection potential, a first scanning signal line selection potential and a second scanning signal line selection potential, which are different from each other in change state of a potential level when the power supply is turned to an OFF state,

the drive control unit:

sets a potential of the clock signal at the first scanning signal line selection potential or the scanning signal line non-selection potential;

sets a potential of the clear signal at the second scanning signal line selection potential or the scanning signal

line non-selection potential;

sets the reference potential at the first scanning signal line selection potential or the scanning signal line non-selection potential; and

upon receiving the power supply OFF signal, sequentially performs first discharge processing for setting the potential of the clock signal and the reference potential at the first scanning signal line selection potential, and second discharge processing for setting the potential of the clear signal at the second scanning signal line selection potential, and

at a point of time when the second discharge processing is started, the first scanning signal line selection potential is equalized to a ground potential, and the second scanning signal line selection potential is maintained at a potential level at which the switching elements included in each of the bistable circuits are turned to an ON state.

2. The liquid crystal display device according to claim 1, wherein each of the bistable circuits further includes:

a second first-node control switching element in which a second electrode is connected to the first node, and a third electrode is given the reference potential;

a second node connected to a first electrode of the second first-node control switching element; and

a second-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the second node, and a third electrode is given the reference potential.

3. The liquid crystal display device according to claim 1, wherein, when the power supply is turned to the OFF state, the first scanning signal line selection potential is changed gradually with a constant gradient from a potential at a point of time when the power supply is turned to the OFF state to the ground potential.

4. The liquid crystal display device according to claim 3, wherein the power supply circuit includes a first scanning signal line selection potential generation line for generating the first scanning signal line selection potential based on a predetermined potential generated by the power supply, and a second scanning signal line selection potential generation line for generating the second scanning signal line selection potential based on the predetermined potential, the first scanning signal line selection potential generation line being connected to a first capacitor and a first resistor, the second scanning signal line selection potential generation line being connected to a second capacitor and a second resistor, and

a discharge time constant determined by the second capacitor and the second resistor is larger than a discharge time constant determined by the first capacitor and the first resistor.

5. The liquid crystal display device according to claim 1, wherein the drive control unit sets the potential of the clear signal at the scanning signal line non-selection potential in an event of the first discharge processing.

6. The liquid crystal display device according to claim 1, wherein, when the drive control unit receives the power supply OFF signal, the drive control unit performs initialization processing for setting the potential of the clear signal at the second scanning signal line selection potential and setting the reference potential at the scanning signal line non-selection potential, before the first discharge processing.

7. The liquid crystal display device according to claim 6, wherein the drive control unit sets the potential of the clock signal at the scanning signal line non-selection potential in an event of the initialization processing.

8. The liquid crystal display device according to claim 1, wherein each of the bistable circuits further includes an output-node control switching element, in which a first electrode is given the clock signal, a second electrode is connected to the output node, and a third electrode is given the reference potential.

9. The liquid crystal display device according to any one of claims 1 to 8, wherein the switching elements included in each of the bistable circuits are thin film transistors made of an oxide semiconductor.

10. The liquid crystal display device according to claim 9, wherein the oxide semiconductor is indium gallium zinc oxide (IGZO).

11. A driving method of a liquid crystal display device

including: a substrate that constitutes a display panel; a plurality of video signal lines which transmit video signals; a plurality of scanning signal lines which intersect the plurality of video signal lines; a plurality of pixel formation portions arranged in a matrix so as to correspond to the plurality of video signal lines and the plurality of scanning signal lines; a scanning signal line drive circuit that drives the plurality of scanning signal lines; a power supply circuit that generates, based on a power supply given from an outside, a scanning signal line selection potential as a potential for turning the scanning signal lines to a selected state, and a scanning signal line non-selection potential as a potential for turning the scanning signal lines to a non-selected state; and a drive control unit that controls an operation of the scanning signal line drive circuit, the driving method comprising:

a power supply state detection step of detecting ON/OFF states of the power supply given from the outside; and

an electric charge discharging step of discharging electric changes in the display panel, the electric charge discharging step being executed when the OFF state of the power supply is detected in the power supply state detection step,

wherein the scanning signal line drive circuit includes a shift register made of a plurality of bistable circuits which are provided so as to correspond to the plurality of scanning signal lines and sequentially output pulses based on a clock signal,

the drive control unit generates the clock signal, a clear signal for initializing states of the plurality of bistable circuits, and a reference potential as a potential serving as a reference of operations of the plurality of bistable circuits,

each of the bistable circuits includes:

an output node connected to the scanning signal line;

an output-control switching element in which a second electrode is given the clock signal, and a third electrode is connected to the output node;

a first node connected to a first electrode of the output-control switching element; and

a first first-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the first node, and a third electrode is given the reference potential,

the power supply circuit generates, as the scanning signal line selection potential, a first scanning signal line selection potential and a second scanning signal line selection potential, which are different from each other in change state of a potential level when the power supply is turned to the OFF state,

the electric charge discharging step includes:

a first discharge step of setting the potential of the clock signal and the reference potential at the first scanning signal line selection potential; and

a second discharge step of setting the potential of the clear signal at the second scanning signal line selection potential, and

at a point of time when the second discharge step is started, the first scanning signal line selection potential is equalized to a ground potential, and the second scanning signal line selection potential is maintained at a potential level at which the switching elements included in each of the bistable

circuits are turned to an ON state.

12. The driving method according to claim 11,

wherein each of the bistable circuits further includes:

a second first-node control switching element in which a second electrode is connected to the first node, and a third electrode is given the reference potential;

a second node connected to a first electrode of the second first-node control switching element; and

a second-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the second node, and a third electrode is given the reference potential.

13. The driving method according to claim 11, wherein, when the power supply is turned to the OFF state, the first scanning signal line selection potential is changed gradually with a constant gradient from a potential at a point of time when the power supply is turned to the OFF state to the ground potential.

14. The driving method according to claim 13,

wherein the power supply circuit includes a first scanning signal line selection potential generation line for generating the first scanning signal line selection potential based on a predetermined potential generated by the power supply, and a second scanning signal line selection potential generation line for generating the second scanning signal line selection potential based on the predetermined potential, the first scanning signal line selection potential generation line being connected to a first capacitor and a first resistor, the

second scanning signal line selection potential generation line being connected to a second capacitor and a second resistor, and

a discharge time constant determined by the second capacitor and the second resistor is larger than a discharge time constant determined by the first capacitor and the first resistor.

15. The driving method according to claim 11, wherein the potential of the clear signal is set at the scanning signal line non-selection potential in the first discharge step.

16. The driving method according to claim 11, wherein the electric charge discharging step further includes, as a step performed before the first discharge step, an initialization step of setting the potential of the clear signal at the second scanning signal line selection potential and setting the reference potential at the scanning signal line non-selection potential.

17. The driving method according to claim 16, wherein the potential of the clock signal is set at the scanning signal line non-selection potential in the initialization step.

18. The driving method according to claim 11, wherein each of the bistable circuits further includes an output-node control switching element in which a first electrode is given the clock signal, a second electrode is connected to the output node, and a third electrode is given the reference potential.

19. The driving method according to any one of claims 11 to 18, wherein the switching elements included in each of the bistable circuits are thin film transistors made of an oxide semiconductor.

20. The driving method according to claim 19, wherein the oxide semiconductor is indium gallium zinc oxide (IGZO).

CLAIMS

1. A liquid crystal display device comprising:

a substrate that constitutes a display panel;

a plurality of video signal lines which transmit video signals;

a plurality of scanning signal lines which intersect the plurality of video signal lines;

a plurality of pixel formation portions arranged in a matrix so as to correspond to the plurality of video signal lines and the plurality of scanning signal lines;

a scanning signal line drive circuit that includes a shift register made of a plurality of bistable circuits which are provided so as to correspond to the plurality of scanning signal lines and sequentially output pulses based on a clock signal, and that selectively drives the plurality of scanning signal lines based on the pulses outputted from the shift register;

a power supply circuit that generates, based on a power supply given from an outside, a scanning signal line selection potential as a potential for turning the scanning signal lines to a selected state, and a scanning signal line non-selection potential as a potential for turning the scanning signal lines to a non-selected state;

a drive control unit that generates the clock signal, a clear signal for initializing states of the plurality of bistable circuits, and a reference potential as a potential serving as a reference of operations of the plurality of bistable circuits, and controls an operation of the scanning signal line drive circuit; and

a power supply state detection unit that gives a

predetermined power supply OFF signal to the drive control unit upon detecting an OFF state of the power supply,

wherein the plurality of video signal lines, the plurality of scanning signal lines, the plurality of pixel formation portions, and the scanning signal line drive circuit are formed on the substrate,

each of the bistable circuits includes:

an output node connected to the scanning signal line;

an output control switching element in which a second electrode is given the clock signal, and a third electrode is connected to the output node;

a first node connected to a first electrode of the output control switching element; and

a first first-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the first node, and a third electrode is given the reference potential,

the power supply circuit generates, as the scanning signal line selection potential, a first scanning signal line selection potential and a second scanning signal line selection potential, which are different from each other in change state of a potential level when the power supply is turned to an OFF state,

the drive control unit:

sets a potential of the clock signal at the first scanning signal line selection potential or the scanning signal line non-selection potential;

sets a potential of the clear signal at the second scanning signal line selection potential or the scanning signal

line non-selection potential;

sets the reference potential at the first scanning signal line selection potential or the scanning signal line non-selection potential; and

upon receiving the power supply OFF signal, sequentially performs first discharge processing for setting the potential of the clock signal and the reference potential at the first scanning signal line selection potential, and second discharge processing for setting the potential of the clear signal at the second scanning signal line selection potential, and

at a point of time when the second discharge processing is started, the first scanning signal line selection potential is equalized to a ground potential, and the second scanning signal line selection potential is maintained at a potential level at which the switching elements included in each of the bistable circuits are turned to an ON state.

2. The liquid crystal display device according to claim 1, wherein each of the bistable circuits further includes:

a second first-node control switching element in which a second electrode is connected to the first node, and a third electrode is given the reference potential;

a second node connected to a first electrode of the second first-node control switching element; and

a second-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the second node, and a third electrode is given the reference potential.

3. The liquid crystal display device according to claim 1, wherein, when the power supply is turned to the OFF state, the first scanning signal line selection potential is changed gradually with a constant gradient from a potential at a point of time when the power supply is turned to the OFF state to the ground potential.

4. The liquid crystal display device according to claim 3, wherein the power supply circuit includes a first scanning signal line selection potential generation line for generating the first scanning signal line selection potential based on a predetermined potential generated by the power supply, and a second scanning signal line selection potential generation line for generating the second scanning signal line selection potential based on the predetermined potential, the first scanning signal line selection potential generation line being connected to a first capacitor and a first resistor, the second scanning signal line selection potential generation line being connected to a second capacitor and a second resistor, and

a discharge time constant determined by the second capacitor and the second resistor is larger than a discharge time constant determined by the first capacitor and the first resistor.

5. The liquid crystal display device according to claim 1, wherein the drive control unit sets the potential of the clear signal at the scanning signal line non-selection potential in an event of the first discharge processing.

6. The liquid crystal display device according to claim 1, wherein, when the drive control unit receives the power supply OFF signal, the drive control unit performs initialization processing for setting the potential of the clear signal at the second scanning signal line selection potential and setting the reference potential at the scanning signal line non-selection potential, before the first discharge processing.

7. The liquid crystal display device according to claim 6, wherein the drive control unit sets the potential of the clock signal at the scanning signal line non-selection potential in an event of the initialization processing.

8. The liquid crystal display device according to claim 1, wherein each of the bistable circuits further includes an output-node control switching element, in which a first electrode is given the clock signal, a second electrode is connected to the output node, and a third electrode is given the reference potential.

9. The liquid crystal display device according to claim 1, wherein the switching elements included in each of the bistable circuits are thin film transistors made of an oxide semiconductor.

10. The liquid crystal display device according to claim 9, wherein the oxide semiconductor is indium gallium zinc oxide (IGZO).

11. A driving method of a liquid crystal display device

including: a substrate that constitutes a display panel; a plurality of video signal lines which transmit video signals; a plurality of scanning signal lines which intersect the plurality of video signal lines; a plurality of pixel formation portions arranged in a matrix so as to correspond to the plurality of video signal lines and the plurality of scanning signal lines; a scanning signal line drive circuit that drives the plurality of scanning signal lines; a power supply circuit that generates, based on a power supply given from an outside, a scanning signal line selection potential as a potential for turning the scanning signal lines to a selected state, and a scanning signal line non-selection potential as a potential for turning the scanning signal lines to a non-selected state; and a drive control unit that controls an operation of the scanning signal line drive circuit, the driving method comprising:

a power supply state detection step of detecting ON/OFF states of the power supply given from the outside; and

an electric charge discharging step of discharging electric changes in the display panel, the electric charge discharging step being executed when the OFF state of the power supply is detected in the power supply state detection step,

wherein the scanning signal line drive circuit includes a shift register made of a plurality of bistable circuits which are provided so as to correspond to the plurality of scanning signal lines and sequentially output pulses based on a clock signal,

the drive control unit generates the clock signal, a clear signal for initializing states of the plurality of bistable circuits, and a reference potential as a potential serving as a reference of operations of the plurality of bistable circuits,

each of the bistable circuits includes:

an output node connected to the scanning signal line;

an output-control switching element in which a second electrode is given the clock signal, and a third electrode is connected to the output node;

a first node connected to a first electrode of the output-control switching element; and

a first first-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the first node, and a third electrode is given the reference potential,

the power supply circuit generates, as the scanning signal line selection potential, a first scanning signal line selection potential and a second scanning signal line selection potential, which are different from each other in change state of a potential level when the power supply is turned to the OFF state,

the electric charge discharging step includes:

a first discharge step of setting the potential of the clock signal and the reference potential at the first scanning signal line selection potential; and

a second discharge step of setting the potential of the clear signal at the second scanning signal line selection potential, and

at a point of time when the second discharge step is started, the first scanning signal line selection potential is equalized to a ground potential, and the second scanning signal line selection potential is maintained at a potential level at which the switching elements included in each of the bistable

circuits are turned to an ON state.

12. The driving method according to claim 11,

wherein each of the bistable circuits further includes:

a second first-node control switching element in which a second electrode is connected to the first node, and a third electrode is given the reference potential;

a second node connected to a first electrode of the second first-node control switching element; and

a second-node control switching element in which a first electrode is given the clear signal, a second electrode is connected to the second node, and a third electrode is given the reference potential.

13. The driving method according to claim 11, wherein, when the power supply is turned to the OFF state, the first scanning signal line selection potential is changed gradually with a constant gradient from a potential at a point of time when the power supply is turned to the OFF state to the ground potential.

14. The driving method according to claim 13,

wherein the power supply circuit includes a first scanning signal line selection potential generation line for generating the first scanning signal line selection potential based on a predetermined potential generated by the power supply, and a second scanning signal line selection potential generation line for generating the second scanning signal line selection potential based on the predetermined potential, the first scanning signal line selection potential generation line being connected to a first capacitor and a first resistor, the

second scanning signal line selection potential generation line being connected to a second capacitor and a second resistor, and

a discharge time constant determined by the second capacitor and the second resistor is larger than a discharge time constant determined by the first capacitor and the first resistor.

15. The driving method according to claim 11, wherein the potential of the clear signal is set at the scanning signal line non-selection potential in the first discharge step.

16. The driving method according to claim 11, wherein the electric charge discharging step further includes, as a step performed before the first discharge step, an initialization step of setting the potential of the clear signal at the second scanning signal line selection potential and setting the reference potential at the scanning signal line non-selection potential.

17. The driving method according to claim 16, wherein the potential of the clock signal is set at the scanning signal line non-selection potential in the initialization step.

18. The driving method according to claim 11, wherein each of the bistable circuits further includes an output-node control switching element in which a first electrode is given the clock signal, a second electrode is connected to the output node, and a third electrode is given the reference potential.

19. The driving method according to claim 11, wherein the switching elements included in each of the bistable circuits are thin film transistors made of an oxide semiconductor.

20. The driving method according to claim 19, wherein the oxide semiconductor is indium gallium zinc oxide (IGZO).