

ABSTRACT

The invention relates to a data processing arrangement including at least one data processing unit (2) and at least one nonvolatile memory (5) that is electrically erasable and reprogrammable, at least under the partial control of the processing unit.

The arrangement is characterized in that it includes at least one processing unit (2) and at least one nonvolatile memory (5) electrically erasable and reprogrammable at least under the partial control of the processing unit, characterized in that it includes means (8) for detecting a signal requesting reinitialization of the registers of the system, which command means (7) bringing about the inhibition of the application of at least one signal (V_{pp} , WE, EE) necessary for the programming of the nonvolatile memory (5), at least when said signal (RAZ) requesting reinitialization of the registers of the arrangement has a level (RAZ1) sufficient to activate the reinitialization.

A particularly important application of the arrangement relates to monolithic and/or autoprogrammable microprocessors.

Fig. 1

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Terms in French on drawings are translated as follows,
going by the block numbers, reading from top to bottom or left to
right as applicable, of each figure.

Fig. 1

- 6: converter
- 9: V_{CC} detector
- 8: RAZ1 detector
- 2: processing unit

Fig. 2

- 6: converter
- 8: RAZ1 detector

Fig. 3

- 6: converter
- 9: V_{CC} detector
- 8: RAZ1 detector

Fig. 4

- 6: converter
- 9: V_{CC} detector
- 8b: RAZ1 detector
- 10: RAZ2 detector

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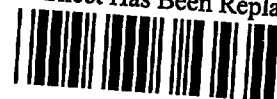


Fig. 5

6: converter
9: V_{CC} detector
13: automatic RAZ
8: RAZ detector
14: clock

Fig. 6

9: V_{CC} detector
13: automatic RAZ
8: RAZ detector
14: clock
6: converter

Fig. 7

13: automatic RAZ
8: RAZ detector
14: clock